

PCI Express Receiver Design Validation Test with the Agilent 81134A Pulse Pattern Generator/ 81250A ParBERT

Product Note





Agilent Technologies

Introduction

The digital communications deluge is the driving force for high-speed interconnects between chips, functional boards and systems. The data may be digital, but it is analog, low-voltage differential signaling (LVDS) that designers are choosing to drive these high-speed transmission lines. LVDS is proven for speed, low power, and noise control. Its cost advantages are also popular in point-to-point applications for datacom.

This product note begins with an introduction to PCI Express Receiver (RX) Design Validation needs. The different tests to be performed are described.

Technical details are given on the setup of RX Design Validation measurements, in particular noise and cross-talk measurements. This document focuses on the RX side as the tests on this side are more challenging than the ones on the transmitter (TX) side. For the TX side, it is convenient to hook up an oscilloscope to measure the signals directly. For the RX side, an indirect method is needed.

RX Design Validation Test Principle

Stimulus:



Assumption:

The response is correct if

1) the RX input received the stimulus signal correctly and

2) the subsequent stages of the DUT processed it properly.

Figure 1

Principle of Operation

Figure 1 shows the principle of operation and the central assumption used in the RX Design Validation Test. The PCI Express device under test (DUT) is initialized by a training sequence. This is a specific data sequence that stimulates a part of the DUT's functionality. When stimulated by a training sequence, the DUT will react by outputting a similar sequence. The bit pattern of the answer is predictable. However, due to the latency that the PCI Express specification allows between the stimulus (Training Sequence TS1) and the response of the DUT (Training Sequence 2), the exact timing cannot be predicted precisely. The response needs to be checked within a latency window.

This behavior can be used to characterize the RX input performance. The stimulating training sequence can be sent with nominal conditions or with superimposed stress. The stress applied to the stimulus sequence can be various levels and swing, noise added to the levels in common and differential mode or jitter to reduce the eye opening.

Design Verification/ Characterization Test Setup

The Logic Analyzer is the preferred tool to determine whether the response training sequence is correct. This instrument allows the analysis of the exact data flow and to check whether an expected data sequence was transmitted.

For the stimulating training sequence, a Pattern Generator is needed that allows data sequences to be loaded, e.g into memory. By using variable levels and timing, a sequence can be applied to the RX input with nominal levels and timing. Additionally, the swing or the pulse width can be reduced up to the point where the DUT ceases to work correctly. With the help of an additional Function Generator, the signal can be further stressed by applying noise and jitter. See the following figures for details.

The stimulus side of the RX Design Validation Test setup (Pulse Pattern Generator) is complemented by an oscilloscope (Agilent 86100A/B Infinium DCA) for signal integrity tests on the TX (response) side.

For functional testing, the stimulus signal needs to be clean and the levels/swing are set to the nominal conditions. These levels meet or exceed the minimum requirements defined in the standard. No noise or jitter is applied.

The stress measurements are performed by reducing the levels/swing below the minimum requirements of the receiver. The logic analyzer will immediately detect a false

Test Setup



Figure 2

response caused by the RX input being unable to recognise the stressed signal. Other stress applied consists of superimposed noise. This can be common mode noise or differential noise. Common mode noise is noise added to both, data and complementary data, in the same way. Differential noise, or cross-talk, is a signal added to only one of the data lines. Jitter modulation will reduce the effective eye opening time-wise. As the eye opening gets smaller, the harder it becomes for the RX input to capture the bits correctly. At a certain eye opening, the input bandwidth will be insufficient to recognise the input sequence correctly.

Functional versus Stress Test

Functional	Nominal Eye
Stress	Min/max Swing
	Noise
	Jitter

Figure 3



Figure 3b describes the RX Design Verification/Compliance Measurements as derived from the specifications of the PCI Express standard.

These Measurements are: **Receiver Voltage**

This is the functional test with the input signal levels at nominal conditions defined with the eye mask.

Jitter Outliner

This is a stress test with a jitter modulation within a jitter budget as defined at section 4.3.4. This test also can be called Jitter Tolerance Testing. **Common Mode Noise**

Common Mode Noise

This is a stress test with the same noise signal on both, the data and the complement data line. The noise magnitude is defined in section 4.4.4 of the specification.

Cross-talk

This is a stress test with noise only on one data line as defined in section 4.3.3 Delay between Data Lanes This is a stress test for PCI Express devices by 2, 4, 8, 16 that have multiple RX inputs. The stress applied is skew (delay) between the Data Lanes.

How to apply Jitter

The jitter modulation is straight-forward when using the Agilent 81133/34A Pattern Generator or the Agilent ParBERT 3.35 Gb/s generators. Both have a built-in Delay Control Input for generating jitter modulation by connecting a Function Generator. The waveform of the Function Generator defines the modulation type, the amplitude defines the degree of the eye closure.

RX Design Verification/Compliance Measurements

Description	Measurement	Equipment	Compliance
Receiver Voltage	apply Training Sequence, detect response	Pulse Pattern Generator, Logic Analyzer	RX Eye (page 214)
Jitter Outliner (Tolerance)	Receiver Voltage measurement plus modulated eye	same plus Function Generator	Jitter budget, section 4.3.4
Common Mode	Receiver Voltage measurement plus common mode noise	as above	Common Mode Noise < 100 mV, section 4.3.4
Cross-talk on Idle	Receiver Voltage measurement plus single ended noise	as above	Noise < 65 mV, section 4.3.3
Delay between Lanes (by 2 and more)	Receiver Voltage measurement with Multiple Lane stimulus	ParBERT 81250 plus as above	< 20 ns any lane per port

Figure 3b

How to apply Jitter (1)



Figure 4

Figure 5 shows three examples of jitter modulation:

- \cdot sinusoidal
- \cdot triangle
- \cdot square

The histogram displayed at the bottom of each waveform shows the jitter distribution caused by the different modulation types. A square modulation emulates deterministic jitter. For the emulation of random jitter, a modulation needs to be performed with a noise source.

How to apply Noise

Any Noise is added as AM (amplitude modulation) to the data sequence. With the help of a Function Generator this noise is e.g. generated as a sinusoidal, rectangular or random signal. The AM is achieved by connecting to the resistors normally used for the termination of the high speed data. When a modulation signal is applied to the sides of the termination resistors that normally terminate to ground, this signal adds to the data sequence at the RX input. For details on how to apply this concept in practice, see Figure 7.

How to apply Jitter (2)





Figure 5

How to apply Noise (1)



Figure 6

The Pattern Generator provides the data sequence on differential lines. To add the modulation signal, a power divider needs to be added to both signal lines. It is essential to maintain equal electrical length of both data lines between the generator output and the RX input.

The power dividers consist of three resistors to ensure proper termination in each direction. The trade-off is the amplitude loss of 50% through the divider. Therefore, in order to provide a specific swing, the Pattern Generator needs to be set to twice the required amplitude.

For common mode noise, both data lines need to be modulated with the same signal. This is achieved by means of a power divider that splits the Function Generator's noise output. This provides the noise signal on both data lines with clean isolation of the data to the complement data line. As the power is divided by two for the modulation signals, the amplitude of the driving Function Generator needs to be set 4 times higher than the desired noise floor at the RX input.

For cross-talk measurements, where the noise signal should appear on a single data line only, the modulation signal from one of the power dividers outputs in the data path is simply disconnected. It is important to terminate both open ends. Some Function Generators may not have an adequate backwards termination. In this case it is helpful to add a 3 dB attenuator between function generator and power divider. This significantly improves backwards termination.

How to apply Noise (2)



Figure 7

How to generate De-Emphasis

To verify the receiver's response to de-emphasized signals, a signal with two different voltage amplitudes within the data stream can be generated by adding the two output channels of the 81134A. While one channel is programmed to generate the 'basic' data stream, the other channel is used to adjust the voltage levels to the nominal and the de-emphasized values.

How to generate De-Emphasis (2)

As the channel addition again is achieved by using power dividers, the voltage amplitude at the pulse generator needs to be set to twice the value of the amplitude required at the DUT. Figure 9 shows a sample signal that is generated by adding the two outputs of the 81134A. To achieve these levels with differential signals, the channel addition is conducted in the following way: Channel one is set to levels in between the emphasized and the de-emphasized levels. The final levels are set to channel two. If both channels are set to their "High" level, the voltages add up to the emphasized levels. If channel two is set complementary to channel one, the substraction of the voltages results in the de-emphasized levels.

How to generate De-Emphasis



How to generate De-Emphasis (2)





Figure 9

Complimentary products for 81134A

$13/20 { m GHz}$
$7 \mathrm{GHz}$
4 GHz

For PCI Express by n (n = 2,4, 8, 16), the 81250A ParBERT offers up to 64 generators. The skew between the channels can be controlled. A variable delay between the individual data lanes is available. With the delay control input, which is available for the Pattern Generator 81134A as well as for each generator in the 81250 ParBERT, the delay can be changed dynamically over the run-time of the stimulating sequence in a range of +/-250ps.

Multiple Channels, PCI Express by 2, 4, 8, 16



Modular count of stimulus channels (1- 64)

Figure 10

Related Literature

• 81133A and 81134A 3.35 GHz Pulse Pattern Generators. Data Sheet

• Jitter Generation and Jitter Measurements with the Agilent 81134A Pulse Pattern Generator & 54855A Infiniium Oscilloscope

• ParBERT 81250 Parallel Bit Error Ratio Tester, Product Overview

• PCI Express Tools - From the Physical Layer to a Fully Operating System

• Signal Integrity Brochure

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United States: (tel) 800 829 4444

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(tel) (82 2) 2004 5004 (fax) (82 2) 2004 5115

Latin America:

(tel) (650) 752 5000

Taiwan:

(tel) 0800 047 866 (fax) 0800 286 331

Other Asia Pacific Countries:

(tel) (65) 6375 8100 (fax) (65) 6836 0252 Email: tm_asia@agilent.com

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