Dramatically accelerate in-circuit validation of systems with FPGAs

大幅提升FPGA系統的內電路驗證速度

2004年7月28、29日 新竹
Dramatically Accelerate In-Circuit Validation of FPGA-based Systems

Agilent FPGA Dynamic Probe

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Agenda

• Why in-circuit debug?
• Issues with traditional “route out” approach
• The FPGA Dynamic Probe – a new approach
• Technology walk-through/demo
• Application example
Why real-time measurements?

- Faster: several seconds in-circuit = days of simulation
- Uncovers problems difficult to simulate
  - Corner cases
  - Interaction with rest of the system
  - Signal integrity effects
- FPGAs enable rapid turns → multiple short iterations

Agenda

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1) Route nets out to FPGA pins

- 1 signal per FPGA pin; usually pin limited
- Requires design change to view new signals
- Manual management of physical and logical signal mapping to logic analyzer
- Equal time investment for each iteration

Manual Setup of Physical Connection
Single pin example

- Pin 6 of the FPGA
- Goes to pin 10 of the micro connector
- Connects to pod 3 channel 8 of the logic analyzer

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Manual Setup of Signal/Bus Names on Analyzer

- Look at schematic
- Determine which connector pin it was routed to
- Determine which logic channel is connected to that pin
- Hand type each name in LA for every signal routed to debug pins
- Signal name in FPGA

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World’s First (& only) Integrated FPGA Application

- Incremental Real Time Internal Measurements ... without:
  - Stopping FPGA
  - Changing the design
  - Modifying design timing

- Quick Logic Analysis Setup
  - FPGA pins to logic analyzer channels
  - Signal and bus names

FPGA Dynamic Probing

- Result of partnership between Agilent and Xilinx

- Awarded “Best Product of the Show” at Electronica-USA 2004 convention

- Shipping for Xilinx Virtex-II, Virtex-II Pro and Spartan-3 Series

- Compatible with all Agilent Windows XP Pro Logic Analyzers (1680/90 & 16900 Series)
FPGA Dynamic Probe

- Insert ATC2 core with Xilinx Core Inserter
- Control access to new signals via JTAG
- FPGA Dynamic Probe SW application supported by 1680/1690/16900
- JTAG
- PC Board
- Probe core output
- Parallel

Agilent Trace Core (ATC2)

- Up to 32 signal banks
- All banks have identical width (4 to 128 signals wide)
- Change signal bank selection from logic analyzer
- Output to FPGA pins for debug
- JTAG Select

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Dramatically Accelerate In-Circuit Validation of FPGA-based Systems
2X Pin Compression

Using Time Division Multiplexing

- Up to 32 signal banks
- All banks have identical width (4 to 128 signals wide)

Pin compression option:
- 2 signals/pin

Change signal bank selection from logic analyzer

ATC2
2X TDM Selection MUX

Output to FPGA pins for debug

Number of Debug Pins

<table>
<thead>
<tr>
<th>Number of Debug Pins</th>
<th>Maximum Internal Signals</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>256</td>
</tr>
<tr>
<td>8</td>
<td>512</td>
</tr>
<tr>
<td>16</td>
<td>1024</td>
</tr>
<tr>
<td>32</td>
<td>2048</td>
</tr>
<tr>
<td>128</td>
<td>8192</td>
</tr>
</tbody>
</table>

Core Options

- State Core Without Pin Compression
- State Core With Pin Compression
- Timing Core
Dramatically Accelerate In-Circuit Validation of FPGA-based Systems
When to Choose State vs Timing Cores

<table>
<thead>
<tr>
<th>State Core (90%+ of cases)</th>
<th>Timing Core (10%- of cases)</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Best for functional debug in one time domain</td>
<td>• Best for measurements across multiple time domains</td>
</tr>
<tr>
<td>• TDM for 2X pin reduction</td>
<td>• Minimal impact on design timing</td>
</tr>
<tr>
<td>• Calibration capability</td>
<td>• Measurements include skew from routing path variances</td>
</tr>
<tr>
<td>• Cycle accurate measurement</td>
<td>• Glitch detection</td>
</tr>
<tr>
<td>• Measured on each FPGA clock cycle</td>
<td>• Measured per logic analysis timing sample rate</td>
</tr>
</tbody>
</table>

System Components

• Xilinx Core Inserter
  • (Bundled with ChipScope Pro, $695 for annual license)
• Logic Analyzer
  • Agilent Windows XP Logic Analyzer (1690/1680 starting at $6995, modular 16900 system starting at $21k)
  • FPGA Dynamic Probing Software = $995 annual license, $3k perpetual (prices reflect 50% off promotion on each good through 2004)
• Xilinx JTAG Cable = $95
Dramatically Accelerate In-Circuit Validation of FPGA-based Systems

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  The FPGA Dynamic Probe – a new approach
• Technology walk through / demo
• Application example

Technology Walk Through

Xilinx Core Inserter
• Create core & put it in design
• Agilent FPGA Dynamic Probe
  • Pin and signal/bus setups
  • Core control
  • Taking measurements
Debug example – Xilinx XC2V250

Packet Communications System

Mictor Connector

Define 1st Bank to View Transmit Side

External Data IN

“Serial to Monitor” State Machine

8B/10B Encoder

Serial Packets

Serial Acks

Xilinx FPGA

External Data IN

AgilentTraceCore2

JTAG to Logic Analyzer

To Logic Analyzer Connection (16 Pins for Debug)

8

8

TID

State

Ack ID

State

Master State Machine

Bank 0

TID State

Bank 3

Data In & Out

Bank 2

Master State Machine

Bank 1

Ack ID State TID out

Micro Blaze uP

RAM

External RAM

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Dramatically Accelerate In-Circuit Validation of FPGA-based Systems
ChipScope Pro

- ILA & logic analyzer viewer
- Core Inserter
- Post-synthesis insertion
- Core Generator
- Pre-synthesis core generation

Preferred design flow:
- Timing Constraints
- Synthesis
- Insert ATC-2 Cores
- Translate (LUTs and nets)
- Static Timing Analysis
- Program FPGA
- Functional Simulation
- Design Modifications
- Design Entry
- Bitstream
- PROM
- FPGA

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Set Core Parameters

- # of debug pins
- # of signal banks
- Pin compression

Select Capture Mode

ATC2 pin location

Xilinx Core Inserter

Specify Signal Bank Grouping

Select Bank

Add signals into each desired Bank

Xilinx Core Inserter
Establish JTAG Communication Link
(Between logic analyzer application and ATC2 core)

FPGA Dynamic Probe (demo)
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Dramatically Accelerate In-Circuit Validation of FPGA-based Systems

**Pin Mapping Tab**

- Spare connector pins available for other PC board signals
- Completed FPGA pin to probe PC board routing

![Pin Mapping Diagram]

**Before - Manual Setup of Signal/Bus Names on Analyzer**

- Look at schematic
- Determine which connector pin it was routed to
- Determine which logic channel is connected to that pin
- Hand type each name in LA for every signal routed to debug pins

![Before Diagram]
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Now ... Signal Name Import

“Generic” signal names

Reads .cdc file produced by Core Inserter

All Signal Updated with FPGA Design Names

Transfers signal/bus names from design to logic analyzer

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**Select Bank to Activate**

![Diagram of Select Bank to Activate]

**Select Signal Bank Zero**

![Diagram of Select Signal Bank Zero]

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View Signals at Transmit Side

Measurement of Signals/Buses on Bank 0
Change to Measure Signals on Bank 1

Selected Bank Becomes Active and Logic Analyzer Updates Signal names from the Active Bank
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Measure Signals at Receive Side

External Data IN

“Serial to Monitor” State Machine
State TID

8B/10B Encoder

Serial Packets

Monitor

“Serial from Monitor” State Machine
State Ack ID

TID Out

Serial Acks

Master State Machine

Bank 0
Bank 3
Bank 2
Bank 1

TID State

5

3

8

RAM

Micro Blaze uP

Xilinx FPGA

Bank 0 TID State
Bank 3 Data In & Out
Bank 2 Master State Mach.
Bank 1 Ack ID State TID out

MUX

External RAM

Agilent TraceCore 2

External Data IN

JTAG to Logic Analyzer

To Logic Analyzer Connection
(16 Pins for Debug)

Measurement of Signals/Buses on Bank 1

Time correlation with external events

Bus names

Measurement of Signals/Buses on Bank 1
**Productivity Improvements**

- **Dramatic productivity improvement!**

- 1 pin $\rightarrow$ 1 signal
- Fixed probe points (design changes)
- Manually manage physical connection
- Manually enter signal & bus names in logic analyzer

- 1 pin $\rightarrow$ up to 64 signals
- Dynamic probing (without design change)
- Easy graphical description of physical connection
- Automatic synchronization of signal and bus names

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**Time Saving Benefits**

- **Dramatic productivity improvement!**

- Better internal visibility
- Save time
- Eliminates error prone & time consuming tasks

- 1 pin $\rightarrow$ up to 64 signals
- Dynamic probing (without design change)
- Easy graphical description of physical connection
- Automatic synchronization of signal and bus names

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### Worst Case Resources for Core

<table>
<thead>
<tr>
<th>Core Type</th>
<th>Total LUTs</th>
<th>Total Flops</th>
</tr>
</thead>
<tbody>
<tr>
<td>State Core without Pin Compression</td>
<td>262</td>
<td>533</td>
</tr>
<tr>
<td>State Core with 2X Pin Compression</td>
<td>462</td>
<td>880</td>
</tr>
<tr>
<td>Timing Core</td>
<td>75</td>
<td>217</td>
</tr>
</tbody>
</table>

Enter # of pins (if state core, don’t count the clock pin): 40
Enter # of signal banks (1,2,4,8,16, or 32): 8

XC2V3000 has 28,672 LUTs and Flops
Core uses up to 0.9% of LUTs, 1.9% of Flops

### Summary

- Simulation has its limitations
- FPGAs allow early in circuit validation and debug
- The FPGA Dynamic Probe can reduce validation and debug time through
  - Wide signal visibility with fixed pins
  - Probe selection without design changes
  - Automated signal mapping to logic analyzer
  - Easy correlation of internal FPGA events to rest of system
- Soft Touch Pro connector-less probing is a great new option
Other Tools From Agilent

For General FPGA Debug

- Agilent Infiniium Mixed Signal Oscilloscopes
  - 2 or 4 analog inputs
  - 1GHz analog bandwidth
  - 16 digital inputs
  - Up to 16 Mbytes MegaZoom Deep Memory
  - SoftTouch compatible

Recommended Resources

- B4655A FPGA Dynamic Probe
- Xilinx ChipScope Pro
- 1680/1690/16900 Logic Analyzers
Resource Materials

- Agilent
  - www.agilent.com/find/fpga
  - www.agilent.com/find/16900
- Demos:
  - www.agilent.com/find/logicdemos
- FAQs:
  - www.agilent.com/find/fpga_faq
- Archived Web seminar:
  www.agilent.com/find/FPGAeseminar
- Probing:
  - www.agilent.com/find/logic_analyzer_probes
- Soft Touch:
  - www.agilent.com/find/softtouch

- Xilinx: www.xilinx.com
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