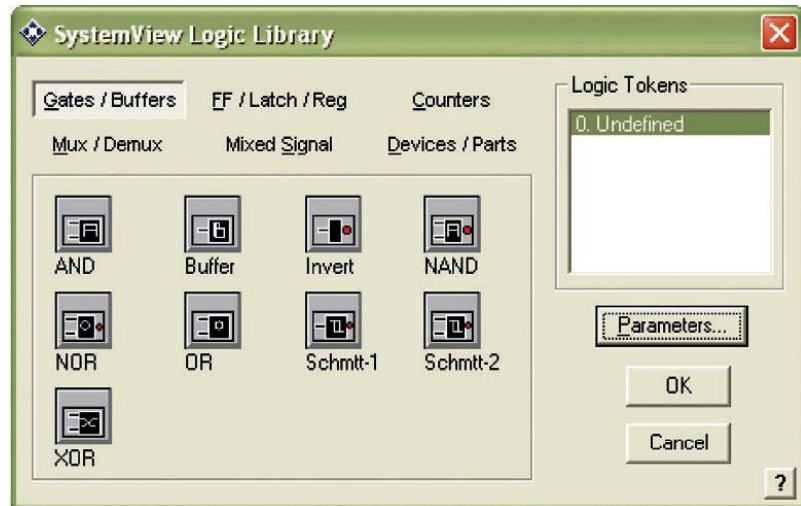


# Agilent EEsof EDA SystemVue Logic Library

## Features

- AND, NAND, OR, XOR, and NOR gates
- Buffer and inverter gates
- 1- and 2-input Schmitt trigger gates
- D-type, quad-D, and J/ K\* flip-flops
- Set/reset latch, 8-bit transparent latch
- Shift registers, counters
- PROM
- Digital phase/frequency detector
- Digital multiplexers, demultiplexers
- Analog multiplexers, demultiplexers
- One-shot (retriggerable monostable multivibrator)
- Digital comparator
- Analog comparator



The SystemVue Logic Library features logical gate operations with realistic rise and fall times. These Logic tokens can be used on a stand-alone basis to simulate systems such as a sequencer or digital sliding correlator, or can be combined to enhance the Communications, DSP, or RF/Analog libraries.

## Overview

SystemVue is a software environment for communications, DSP, and RF analog system design. The optional SystemVue Logic Library has three classifications of tokens:

**Generic Tokens** include well-known functions such as the NAND gate. These generic logic tokens can have an unlimited numbers of inputs. For example, you may use the NAND token to create a 2-input NAND gate, a 5-input NAND gate, and so on.

**7400 Tokens** simulate functions available as off-the-shelf parts. In SystemVue, "74xx" refers to a specific logic function and not to a family such as TTL or CMOS.

**Custom Tokens** implement logic functions not generally available as off-the-shelf parts, or mixed-signal functions such as an analog switch, analog comparator, 16-bit DAC, or 16-bit ADC. Logic parameters

can be independently set on each device, including logic thresholds, the amplitude and polarity of the HIGH and LOW states, and the output delay of the function. The default propagation time (output delay) is zero seconds to be consistent with the logic tokens that are in the main Operator library.

The Logic library may be used on a stand-alone basis to simulate systems such as a sequencer or digital sliding correlator, or it may be combined with the Communications, DSP, or RF/Analog libraries to enhance their capabilities. An example of this multi-library use would be the simulation of a PLL (phase-locked loop) using a MC4044 Digital Phase/Frequency Detector and the 744040 12-stage binary counter from the Logic Library, and an Op-Amp type lowpass filter from the RF/Analog Library.



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## Library Tokens

### Flip flops/latches/registers

D-type flip flop (positive edge triggered)  
 Quad D-type flip flop  
 J-NOT-K type flip flop (positive edge triggered)  
 8-Bit transparent latch with Q output  
 8-Bit parallel-in/serial-out shift register  
 8-Bit serial-in/parallel-out shift register  
 Programmable read only memory (8x8)  
 Read only memory from table (ROM-64Kx16)  
 Set/reset latch (two NAND gates, cross-coupled)

### Gates/buffers

AND gate  
 NOR gate  
 OR gate  
 XOR gate  
 NAND gate  
 Non-inverting buffer  
 Inverter (NOT)  
 2-Input Schmitt trigger NAND  
 Schmitt trigger inverter

### Multiplex/demultiplex

8-Input digital multiplexer  
 3-line to 8-line demultiplexer

### Mixed signal

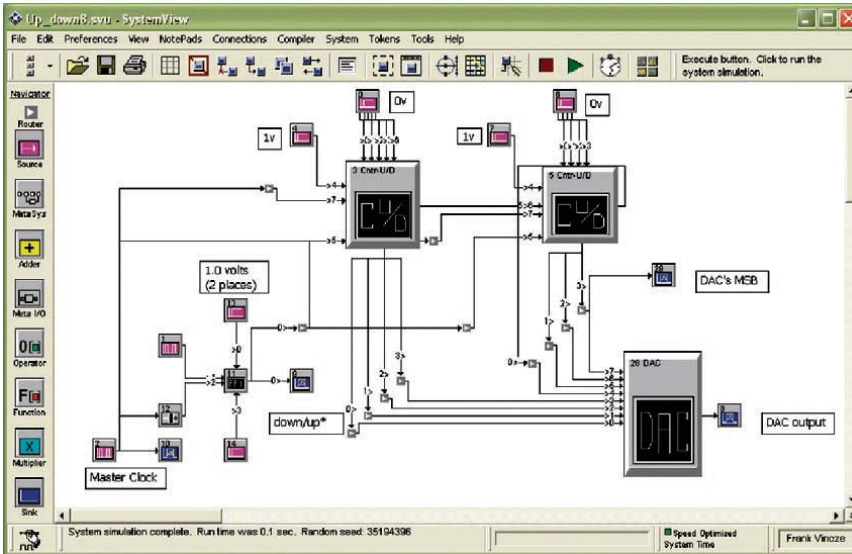
n-Bit analog to digital converter (ADC)  
 n-Bit integer to digital converter  
 n-Bit digital to analog converter (DAC)  
 Analog comparator (differential analog input, Q and Q\* output)  
 Two-channel analog multiplexer/demultiplexer (DPDT switch)  
 Two-channel analog multiplexer (SPDT switch)

### Devices/parts

8-Bit identity comparator (equality detector)  
 Retriggerable monostable multivibrator  
 Phase-frequency detector

### Counters

4-Bit synchronous presettable binary counter  
 12-Bit stage binary counter  
 4-Bit synchronous binary up/down counter, with one clock



An example of two cascaded up/down counters from the SystemVue Logic library using the ripple carry/borrow method of interconnection.

For more information on SystemVue and related products, visit:  
[www.agilent.com/find/eesof-eagleware](http://www.agilent.com/find/eesof-eagleware).

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