

Agilent E2960B Series for PCI EXPRESS® 2.0

Data Sheet Version 2.4

Fastest Time to Insight

The most integrated and comprehensive PCI Express® x1 through x16 test solution, with superior probing

P2L Gateway

Full system viewing with the extended P2L **Stimulus**

gateway

Unique logic and protocol functionality in a single solution

Tools

Thorough product testing with the x1 through x16 exerciser

Compliance test packages to speed up your test cycles

Industry's first Jammer for disruptive testing in live system

Solution Approach

Complete two in one modular and scalable solution for stimulus response



Protocol **Analyzer**

Reliable traffic capture with analyzers x1 through x16

> **Superior protocol** visualization through flexible and customizeable GUI

Array of probing solutions to meet your product needs

Table of Contents

Overview2
E2960B Key Features2
System Architecture Overview3
Typical Configurations4
PCI Express Gen 2 Ready Program5
Overview6
N5306A Analyzer8
N5322A Extended Interface Module11
N5309A Exerciser, Protocol Test Card 2.0 and Compliance Tests12
N5323A Jammer17
N4241A/2A/3A Full Size Mid-bus Probe19
N5328A Half Size Mid-bus Probe21
N4241F Flying Lead Probe23
N4241Z ZIF Flying Leads Probe25
N5315A Slot Interposer Probe27
N5316A Passive Backplane29
N5313A P2L Gateway Cable31
N5319A P2L Gateway Cable with Flag Support32
Related Products33
Related Agilent Literature33
Ordering Information34
Product Web SiteBack cover
Sales and ServiceBack cover

Overview

The E2960B Series is the industry's most complete and integrated test system with x1 through x16 protocol analyzer, exerciser, compliance test packages and an array of probing solutions to meet test needs.

- The non-intrusive analyzer provides an authentic system view with genuine and unaltered signal characteristics.
- The exerciser provides thorough testing of the link from x1 to x16, with an automated LTSSM exerciser and predefined compliance test to expedite test cycles.
- The protocol to logic gateway (P2L gateway) for correlation with the Agilent logic analyzers, enabling broad visibility into all parts of the system.
- Integrated solution for stimulus (exerciser) and response (analyzer) enables detailed observation and full understanding of the DUT's behavior.

These capabilities provide our customers with the fastest time to insight. Leaving more time for design debug, and bringing products to market quickly.

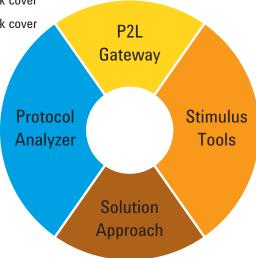


Figure 1.

E2960B Key Features

- Reliable traffic capture and analysis.
- Fastest lock times in the industry, 3 - 4 FTS lock time typical, for effective active state power management (ASPM) testing.
- Easy flow and context sensitive display for clear protocol viewing.
- Full package of post processing capabilities including flow control tracking, traffic over view and real time statistics.
- Sophisticated triggering, search, and filtering capabilities.
- Includes unique logic capabilities such as lane view, fast ASPM sync time, and trigger on ordered set.
- Comprehensive probing capabilities, including Mid-bus 2.0, Flying Lead 2.0 and slot interposer probes.
- Unique LTSSM testing using pre-configured tests.
- Innovative jammer tool to simplify error injection and disruptive tests.
- PTC 2.0, compliance tests for PCI Express Gen1 and Gen2 on the same test card.
- Upgradable hardware model, can be used for PTC 2.0 or upgraded to the compliance assured test package with 170 PCI-SIG recommended additional tests, or to full exerciser capabilities.
- Cross triggering between logic analyzer and protocol analyzer.
- Ping-pong triggering with flags is supported.
- Strong integration between exerciser and analyzer allows the analyzer to capture only the key segments of the device behavior.
- Replay traffic in the exerciser recorded with the protocol analyzer.
- Consistent use model between both stimulus and response to minimize learning curve.

System Architecture Overview



- 1 Windows® XP or Windows 7 PC host to manage and interact with the system.

 Multiple connection options for the controller:
 - 100 Mbps ethernet LAN directly from PC controller to chassis
 - USB to LAN dongle available for USB connectivity to PC
- 2 Chassis (2 slot or 4 slot available)
- 3 N5306A protocol analyzer module controlled via LAN or USB 2.0 link from the PC controller
- 4 N5316A test backplane, allows testing of end points without vendor system
- 5 N5309A exerciser module controlled via LAN or USB 2.0 link from the PC controller
- 6 N5315A slot interposer probe

Figure 2. E2960B protocol analyzer

Platform continuity	 The Agilent E2960B Series is based on the existing platform making the E2960A Chassis and probes usable again for PCle™ 2.0. The complete software; including the GUI, is the same for both series of products, so customers can protect their investment and leverage their existing know-how to start PCle 2.0 testing immediately. The E2960B Series APIs are compatible with existing E2960A (Gen 1) APIs, allowing scripts developed for Gen 1 to be reused in Gen2 testing.
Gen 2 Ready program	 E2960B hardware used for PCI Express Gen 1 testing. Later, when your organization starts PCI Express Gen 2 testing, it is a simple license update to enable the same hardware for Gen 2 testing.
Unique logic and protocol functionality in a single solution	 A fast and effective way to understand the data from the physical layer through to the transaction layer. This means instantaneous lane status information, both on the I/O module and in the GUI using the per lane LEDs. Per-lane view even prior to channel bonding completion – including 8b, 10b or K/D symbols. Two "Trigger-down-the-lane" patterns on selected lanes. Manual and automatic speed settings.
Test customization and automation with TCL or Windows DCOM	 Automates tedious testing. Repeats tests for subsequent product builds. Creates and automates your specific test procedure. Performs regression tests.



Figure 3.

From a lightweight portable system to large-scale validation environment

The E2960B Series is designed to be lightweight and portable, and take minimum space in your labs. However, if you need many analyzers or exercisers at once, the architecture is designed to support this. Multiple chassis can be connected together to form a large scale, time synchronized test system.

Typical Configurations

The E2960B Series supports two main types applications, exerciser and protocol analyzer.

The main characteristics of the exerciser application is to create stimulus to the device under test (DUT). If you are testing an add-in card, the exerciser can be programed to emulate a root-complex. If you are doing root-complex testing, then the exerciser can be programmed to emulate an end device.

The exerciser application has programmable behaviors at the

physical, data link and transaction layer, to allow you to comprehensively validate the behavior of your DUT before releasing the product. You can program the behavior of the exerciser yourself, or you can purchase the compliance assured test package from Agilent, which includes over 170 fully automated tests to validate the correct behavior of your device.

If problems are uncovered during the testing, then protocol analyzers are used to further debug and troubleshoot the issue at hand. One of the key challenges of doing debugging in PCI Express Gen 2 is access to the signals. The E2960B Series analyzers address this challenge by providing a full array of probing solutions, mid-bus probes, slot interposer probes, and flying lead probes, to meet your test needs.

The E2960B Series protocol analyzers also include sophisticated features such as state-based triggering, easyflow, context sensitive columns to help you gain insight faster.



Exerciser samp	le configuration
Test cards N5309A-E04	Exerciser and LTSSM Board x4 for PCIe 5 Gb/s
Test backplane N5316A	Test backplane
Software N5309A-EX2 N5309A-COM	Exerciser SW license exerciser and LTSSM at 5 Gb/s Exerciser SW license compliance assured test package - including over 170 additional PCI-SIG recommended compliance tests
N5309A-PTC	Exerciser SW license for PTC (free with exerciser purchase) - includes the 13 PCI-SIG required compliance tests



Analyzer sample configuration		
Chassis N5302A	2 slot chassis	
Test cards N5306A	Analyzer module for PCIe 5 Gb/s	
Software N5306A-A04	Analyzer SW license x4 for PCIe 5 Gb/s	
Probes N5315A-A04	Slot interposer x4 for PCle 5 Gb/s	

Figure 4. Analyzer and exerciser sample configurations

PCI Express Gen 2 Ready Program

As the industry starts validating PCI Express Gen 2 designs, many discussions are underway to decide whether to continue investment in test equipment for PCI Express Gen 1 or to shift the investment to Gen 2. The Gen 2 Ready program has been created to make this decision

easier. The Gen 2 Ready program is investment protection of your current test tool investments. Independent of the required lane width, x1 to x16, the Agilent E2960B Series for the PCI Express 2.0 analyzer and exerciser is now available either at 2.5 Gb/s

or 5 Gb/s. You can use the E2960B today just for Gen 1 applications, and migrate to Gen 2 testing over time. The upgrade to Gen 2 functionality is fast and easy, with a software only update — no need for exchange, or swapping out hardware.

Analyzer link	Gen2 Ready configuration	Description	Upgrade to Gen2
x1	N5306A	Analyzer module for PCle 5 Gb/s (requires 2 for x 16)	N5310U-U21
	N5306A-G01	Analyzer SW license x4 for PCIe 2.5 Gb/s	Upgrade x1 from Gen2 Ready to Gen2
	N5315A-A01	Slot interposer x1 for PCIe 5 Gb/s	
	N5302A	2-slot portable chassis	
x4	N5306A	Analyzer module for PCle 5 Gb/s (requires 2 for x 16)	N5310U-U24
	N5306A-G04	Analyzer SW license x4 for PCIe 2.5 Gb/s	Upgrade x4 from Gen2 Ready to Gen2
	N5315A-A04	Slot interposer x4 for PCIe 5 Gb/s	
	N5302A	2-slot portable chassis	
x8	N5306A	Analyzer module for PCle 5 Gb/s (requires 2 for x 16)	N5310U-U28
	N5306A-G08	Analyzer SW license x8 for PCIe 2.5 Gb/s	Upgrade x8 from Gen2 Ready to Gen2
	N5315A-A08	Slot interposer x8 for PCIe 5 Gb/s	
	N5302A	2-slot portable chassis	
x16	N5306A	Analyzer module for PCle 5 Gb/s (requires 2 for x 16)	N5310U-U26
	N5306A	Analyzer module for PCle 5 Gb/s (requires 2 for x 16)	Upgrade x16 from Gen2 Ready to Gen2
	N5306A-G16	Analyzer SW license x16 for PCIe 2.5 Gb/s	
	N5306A-G16	Analyzer SW license x16 for PCle 2.5 Gb/s	
	N5315A-A16	Slot interposer x16 for PCIe 5 Gb/s	
	N5302A	2-slot portable chassis	

Exerciser	Gen2 Ready	.	
link	configuation	Description	Upgrade to Gen2
x1	N5309A-E01	Half sized exerciser and LTSSM board x1 for PCle 5 Gb/s	N5310U-E12
	N5309A-EX1	Exerciser SW license and LTSSM for PCle 2.5 Gb/s	Upgrade from Gen2 Ready to Gen2
x4	N5309A-E04	Half sized exerciser and LTSSM board x4 for PCle 5 Gb/s	N5310U-E12
	N5309A-EX1	Exerciser SW license and LTSSM for PCle 2.5 Gb/s	Upgrade from Gen2 Ready to Gen2
x8	N5309A-E08	Half sized exerciser and LTSSM board x8 for PCle 5 Gb/s	N5310U-E12
	N5309A-EX1	Exerciser SW license and LTSSM for PCle 2.5 Gb/s	Upgrade from Gen2 Ready to Gen2
x16	N5309A-E16	Half sized exerciser and LTSSM board x16 for PCle 5 Gb/s	N5310U-E12
	N5309A-EX1	Exerciser SW license and LTSSM for PCle 2.5 Gb/s	Upgrade from Gen2 Ready to Gen2

Jammer	Gen2 Ready		
link	configuation	Description	Upgrade to Gen2
x1	N5323A-J01	Jammer module x1 for PCle 5 Gb/s	N5310U-J12
	N5323A-JM1	Jammer SW license: Jammer at 2.5 Gb/s	Upgrade from Gen2 Ready to Gen2
x4	N5323A-J04	Jammer module x4 for PCIe 5 Gb/s	N5310U-J12
	N5323A-JM1	Jammer SW license: Jammer at 2.5 Gb/s	Upgrade from Gen2 Ready to Gen2
x8	N5323A-J08	Jammer module x8 for PCIe 5 Gb/s	N5310U-J12
	N5323A-JM1	Jammer SW license: Jammer at 2.5 Gb/s	Upgrade from Gen2 Ready to Gen2

Overview

Reliable traffic capture and	System traffic is easy to understand with the x1 to x16 analyzer.
analysis	 2.5 Gb/s and 5 Gb/s PCI Express traffic is reliably captured.
	 Advanced triggering capabilities reduce the time needed to detect difficult-to-find errors.
	 Reliable data capture even exiting L0s, with the industry's fastest lock time of 3 to 5 fast training sequences (typical).
	 It is fast and easy to understand the data through context-sensitive column analysis with easy flow views.
	 SR-IOV and MR-IOV decodes to support debug and analysis even for the latest specifications from PCI-SIG.
	Full package of post processing features including:
	Flow control credit counting and graphing.
	Transaction viewer and transaction metrics.
	Real time statistics graphing and post processed performance statistics.
	Traffic overview.
Family of superior probing solutions to meet your	The protocol analyzer has a full array of probing solutions, including mid-b slot interposer, and flying lead probes, from x1 to x16.
application needs	 Mid-bus and flying lead probes are designed with low capacitive loading to minimize signal distortion.
	 The slot interposer probe combines outstanding analog repeating technology with mechanical robustness, to allow probing where signal integrity is marginal.
	Low profile mid-bus probe for access in blade server environments.
Full system viewing	Cross bus analysis is made possible using the P2L gateway.
	 Multiple protocols can be monitored at the same time (e.g., PCI Express to DDR).
	 It provides time-correlated views between the logic analyzer view and the protocol analyzer view.
	Cross triggering provided between the logic analyzer and protocol analyzer
	 Ping pong triggering between the logic analyzer and protocol analyzer through flags support.



Overview

S t i m u	Fully validate the DUT (device under test)	 The exerciser: Emulates both root complex and endpoint to allow testing of any type of DUT for PCI Express 2.0. Uses the exerciser and test backplane to test the end point without a system. Automates testing with the built-in API interface. The Jammer: Validate the DUT and software under extreme conditions by creating corner cases and injecting inline errors. Inject errors into a real system with any OS and any driver and any application. Easy to setup, the Jammer is transparent to the PCI express hierarchy. Just insert it into a working system, and start testing.
u s	Thorough link testing	 Pre-defined LTSSM tests can help validate complex and hard to test state transition of the DUT's LTSSM. Easily validate new additions to the 2.0 specifications, including dynamic lane width changes, and link negotiations.
	Compliance testing	 Over 170 compliance test scripts (as defined by the PCI-SIG) quickly test for compliance to the PCI Express 2.0 specifications at the transaction, data link layers, as well as in the configuration space. The exerciser has an easy-to-use GUI; a single click to run all tests, or subsection of test cases. Precise reports to clearly identify pass, fail, and warning results.
S o I u t i o n	Two in one solution for stimulus and response	 A single solution for stimulus (exerciser) and response (analyzer) enables a fully integrated overview, a detailed observation of the DUT's behavior, and a consistent look and feel across both the exerciser and analyzer. Integrated exerciser and analyzer allows easy record and replay; save a packet from the analyzer, and replay in the exerciser.
A p r o a c		

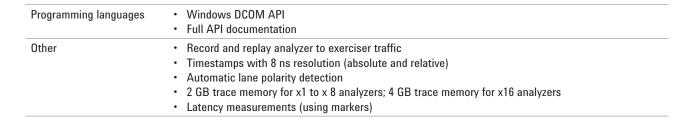
N5306A Analyzer

Features

Display	 Highly configurable GUI, based on a configurable tabular view Color customization Condensed data view using context sensitive columns "Ping-pong" view of upstream/downstream data with easy flow Easy navigation within captured trace Traffic overview (post capture) Per lane display, to show individual lane data Multiple views of the packet decode for faster debugging; record decode view, singe line decode view, payload view, lane view Expand and collapse packets in order to view/hide full packet, with errors that are highlighted Color-coded transaction types allow easy recognition of various types of traffic Multiple markers with comment functionality Display with time stamps, absolute timestamps, relative time stamps, and ability to configure any location as time zero Multiple listings with independent layout Transaction view with associated transaction metrics Ability to dynamically track link width changes Real time statistics Post processed performance statistics Flow control credit tracking counters and graphs
Trigger	 Graphical trigger setup Multi-state, multi-level trigger sequencer – Eight states – Two counters/timers – Four pattern terms – Internal, cross module arm in/out for including in trigger sequencer from another analyzer External trigger in and out Protocol error trigger Multi-directional branching Filtering (real time): – Idles – On a per-packet basis controlled by the trigger sequencer – Storage qualification Filter conditions can be defined individually for each trigger sequencer state Trigger on payload (up to 128 bits) Trigger on a per-bit user specified training sequence ordered set
Search/filter	 Fast hardware based searching and filtering Graphical search/filter setup with easy to configure drag and drop interface Search/filter on protocol errors Multiple parallel search/filter conditions Up to 6 patterns at the same time Extensive list of predefined patterns (TLP, DLLP, ordered sets, training sequences, protocol errors) User definable data patterns
Traffic capture	 Supports capturing in x1, x2, x4, x8, x16 link width with 2.5 GT/s and 5 GT/s Non-intrusive traffic capturing Captures training sequences, ordered sets, data-link-layer packets and transaction-layer packets in both directions simultaneously Supports data rates 2.5 GT/s and 5 GT/s (± 300 ppm) Error detection Disparity errors and invalid 10 b symbols in hardware LCRC, symbol, disparity, EDB, framing, idle data malformed packet check (CRC error, invalid field contents, length mismatch) in software

N5306A Analyzer

Features



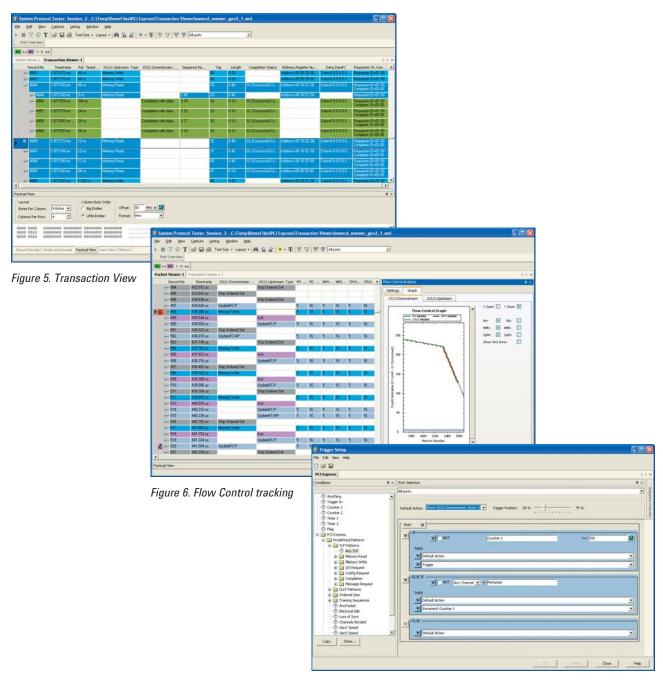


Figure 7. Trigger Setup

N5306A Analyzer Specifications

System

- The N5306A analysis module is an I/O blade that fits into a 2-slot portable chassis (N5302A) or 4-slot rackmountable chassis (N5304A).
- The software application that controls the N5306A module runs on a Windows XP or Windows 7 PC host.
- For more details regarding the chassis or PC controller, see the related products section of the data sheet.

Environment	
Temperature (AT-ETM757)	Operating: 0 °C to +55 °C Storage: -40 °C to +70 °C
Humidity (AT-ETM758)	Operating: 15 to 95% Operating soak: 90% (24 h)
Safety standards	Installation category: EN ISO/IEC 17025, IEC 61010-1/EN61010-1, II Pollution degree: 2 Environmental rating: Standard

General characteristics	
Memory	2 GB
Display	4-character LEDs display on the I/O module for status information
Status LED	16 per lane LEDs to indicate status of the individual lanes Two status LEDs to indicate module global status Grey: system is not configured Red: speed is not detected or system is not configured Yellow: system configured to speed of 2.5 Gb/s Green: system configured to speed of 5 Gb/s
Connectors	 Analyzer probe connector Intermodule connector (used to connect to the logic analyzer via the N5319A P2L gateway with flags support) Self test connector REF clock out 10 MHz clock out Sync port for P2L support



Figure 5. N5306A analyzer

N5322A Extended Interface Module Features and Specifications

System

The N5322A extended interface module should be used in conjunction with the N5306A analyzer I/O module for extended analysis capabilities.

0	40 1 150 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Status LED	16 per lane LEDs to indicate status of the individual lanes	
	Two status LEDs to indicate module global status.	
	Grey: system is not configured	
	 Red: speed is not detected or system is not configured 	
	 Yellow: system configured to speed of 2.5 Gb/s 	
	 Green: system configured to speed of 5 Gb/s 	
Connectors	Analyzer probe connector	
	Intermodule connector	
	REF clock input	
Active state power management (ASPM) capabilities	Bit lock after L0s with typical 3 to 5 fast training sequences	

Environment	
Temperature (AT-ETM757)	Operating: 0 °C to +55 °C Storage: -40 °C to +70 °C
Humidity (AT-ETM758)	Operating: 15 to 95% Operating soak: 90% (24 h)
Safety standards	Installation category: EN ISO/IEC 17025, IEC 61010-1/EN61010-1, II Pollution degree: 2 Environmental rating: Standard
Electrical characteristics Jitter tolerance	Eye width: 0.55 UI (minimum)



Figure 6. Extended interface module

N5309A: Exerciser, Protocol Test Card 2.0 and Compliance Tests Compliance Testing

General	Compliance tests run on existing N5309A exerciser hardware
	PCI Express Gen 1 and Gen 2 both supported
	Easy to use GUI
	- Integrated into N5309A exerciser GUI
	 Run single tests, or select multiple tests for sequential execution
	 Test tagging at start and end of every test. Allowing easy capture and analysis with Agilent's protocol analyzer
Test support	Two test packages available
	- E2969B PTC2
	 Supports all 13 PCI-SIG mandatory test cases
	 N5309A-COM compliance assured test package with over 170 recommended tests
	• 70 transaction layer tests
	• 40 link layer test
	66 config space tests
	• 1 electrical test

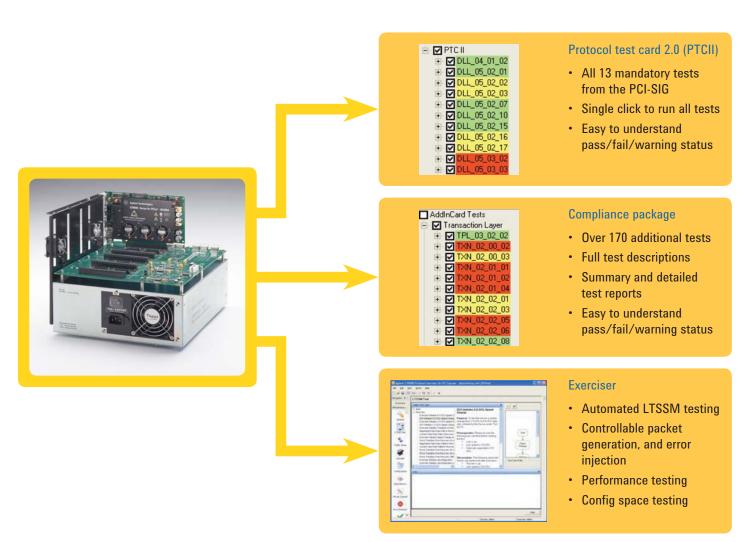


Figure 7. Exerciser and Compliance Test: one hardware, multiple applications

N5309A: Exerciser, Protocol Test Card 2.0 and Compliance Tests Exerciser Features

Physical layer	 Fully automated symbol encoding/decoding, generation, and validation of packet framing; ability to report framing errors to user Scrambling can be turned on or off by user Configurable, automatic link initialization and training: Automatic Lane Polarity Detection (RX), separate for each lane Programmable Lane Polarity Inversion (TX), separate for each lane Automatic link width negotiation; link widths x1, x4, x8, x16 supported; user can configure which widths will be negotiated during link training Programmable Tx Lane Reversal (Rx is automatic) Programmable Lane Skew: (± 7 symbols, resolution: 1 symbol time) Link Training and Status State Machine (LTSSM): Full support for states: detect, polling, configuration, recovery, L1, L0s, L0 Programmable skip rate and number of SKPs per skip OS Note concerning power management: When exiting from L0s or L1 the exerciser's receiver may not be able to receive data until the second SKP ordered set. Packets might get lost, causing a retraining of the PCI Express link.
Data link layer	 Fully implemented data link control and management state machine Automatic flow control initialization; programmable credits and flow control update rate Automated generation of data link layer packets (DLLPs): ACK/NAK, Init/Update-FC Automatic generation and checking of LCRC and sequence numbers; allows the insertion of incorrect LCRCs into TLPs for testing purposes; automatic retry function management
Transaction layer	 User software can define arbitrary sequences of transactions "Send single packet" for simple packet transmission one memory for block transactions per virtual channel Conditional start on RX pattern matcher, external trigger in and completion status Generation and receipt of packets at maximum bandwidth (stress testing); up link width x8 at 5 GT/s Infinite loop One completer queue defines the way completion packets are sent out (e.g. lengths, errors inserted, partitions, etc) Completions can be split into individual packets Up to 32 outstanding requests can be "pending" (256 in extended mode) (request without completion) Decoders (6 BARS + Expansion ROM decoder) Payload generation and reception from/into data memory



Figure 8. N5309A exerciser and LTSSM exerciser

N5309A: Exerciser, Protocol Test Card 2.0 and Compliance Tests Exerciser Features

Packet generation	 Transmit modes Send single packet Block transfer Import packet from captured analyzer trace Sent single packet Send any type of TLP, with control of all the fields Create errors on the transmitted packet Block transfer Create large transfers (read or write), with configurable request size Automatic data comparator to ensure no data corruption Performance testing to ensure maximum data rates Completion queues Program any type of completion status
Error generation and analysis	 Physical layer: Transmitter polarity inversion Transmitter lane reversal Determinant lane skew of up to 7 symbols Link width and lane sequence negotiation emulating a x1, x4, x8, x16 device Sending packets with incorrect "running disparity" TX framing errors on TLPs Data link layer: Sending packets with incorrect LCRC Systematically answers NAK instead of ACK, for retry buffer test Wrong sequence numbers Generate a free form DLLP with any bit changed Transaction layer: Arbitrary header field contents Sending "nullified TLPs" Sending "poisoned TLPs" Advertised packet length (in TLP header) is different from actual packet length (by one word) The transmitter ignores flow control credits Completion loss/delay
Configuration space	 Can emulate the configuration of different types of PCI Express devices Supports up to 6 base address registers and expansion ROM decoder Full support for PCI Header type 0 configuration space Supported capability structures: PCI power management capability structure MSI capability structure PCI Express capability structure Virtual Channel capability structure Advanced error reporting structure
Display	Explorer like tree structure to select test Display of test log in GUI Feedback of state transitions performed Timestamp in [ns] for all states Link status indications Link width x1, x4, x8, x16
Debug support	External trigger on exit from L0 Log file output of LTSSM exerciser state transitions and timestamps Automatic flow control initialization with infinite credits
Supported states	Detect Polling Configuration L0, L0s, L1 Recovery
Easy software upgrade	Ability to upgrade from PTC II license to Compliance Assured Test Package licence to full exerciser and LTSSM software licence

N5309A: Exerciser, Protocol Test Card 2.0 and Compliance Tests Specifications

System requirements

The N5309A is a standalone PCle card that can be used for the PTCII, compliance assured test package and exerciser application. The software application that controls the N5309A card runs on a Windows XP or Windows 7 PC host connected via a USB 2.0 link. For more details regarding the PC controller, see related products section of the data sheet.

Environment	
Temperature (AT-ETM757)	Operating: 0 °C to +55 °C Storage: -40 °C to +70 °C
Humidity (AT-ETM758)	Operating: 15 to 95% Operating soak: 90% (24 h)
Safety standards	Installation category: EN ISO/IEC 17025, IEC 61010-1/EN61010-1, II Pollution degree: 2 Environmental rating: Standard

General characteristics	
Power requirements	100-240 Vac
	130-160 VA 1.5 A maximum
	47 to 63 Hz
Form factor	PCI Express standard height, half size card
	Length: 168 mm (6.6 inch)
	Height: 111 mm (4.37 inch)
	Component height on top side including heat sink: 19 mm (0.75 inch)
Connectors	Front bracket:
	USB type B
	• Vin 18 V DC, 3.5 A
	 PCle analysis output, proprietary
	Top connector:
	 PCle, connector x16, only x1 lane connection
	Bottom connector:
	 PCIe, x1, x4, x8 or x16 (version dependent)
	Trigger in/out:
	LVCMOS 2.5 V, see user guide
	Vin maximum 3.0 V
	Power in:
	 ATX power connector to supply the top connector
SSC	Support for SSC
Data memory	160 kB

N5309A: Exerciser, Protocol Test Card 2.0 and Compliance Tests Specifications

Electrical characteristics	
Data in	Input levels • Minimum: 100 mV • Maximum: 1.2 V Jitter tolerance • Compliant to PCle Specification 2.0 Rev 0.9 Frequency • Minimum: 2.5 GHz -300 ppm*UI 5 GHz -300 ppm • Maximum: 2.5 GHz +300 ppm; 5 GHz +300 ppm SSC support • None
Data out	Output level Minimum: 800 mV (full swing) Typical: 1000 mV Maximum: 1.2 V De-emphasis 3.5 dB Typical: 3.5 dB De-emphasis 6 dB Typical: 6.0 dB UI interval Minimum: -300 ppm*UI Maximum: +300 ppm*UI Total jitter Typical: 0.3 UI Electrical idle Typical: 20 mV
External clock in	Level • Minimum: 800 mVdiff • Maximum: 1200 mVdiff AC coupled Frequency: 100 MHz
Reference clock in	Compliant to PCIe Specification 2.0

N5323A Jammer

Features

General features

- · Ability to configure the physical layer characteristics of the device, including skew, lane polarity, and lane ordering
- · Protocol checker included, ability to flag any protocol violations during test
- · Statistics tables and graphs, to show when errors were inserted during test
- External trigger In/Out, with the ability to trigger the analyzer and vice versa

Jamming options

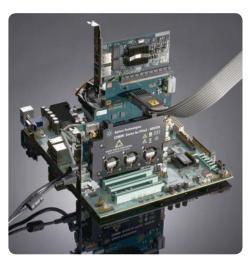
Jamming actions can occur on the physical layer, data link layer and also transaction layer. The list of actions that the jammer can perform are:

Physical layer	 Disparity error on symbols, lanes or packets
	Drop STP/END characters
	Link retrain / recovery
Data link layer	Drop specified DLLP
	Insert arbitrary DLLP
	Corrupt CRC values
	NAK incoming TLP
	Offset sequence number
Transaction layer	Delay TLP
	Drop/Insert TLP
	Replace TLP payload
	Modify TLP header

Automation test

The jammer similar to other PCI Express products from Agilent provides a complete API that allows all aspects of the jammer to be automated. This is key for implementing a regression test environment. In addition, to help you get started, there is a suite of pre-defined test cases available.

- · TCL API with full online documentation
- · Five example test scenarios scripts, part of the QuickTest framework
- Additional 25 test scripts available for purchase, part of the QuickTest framework



Test & Measurement World

BISS

BISS

AWARD WINNER

Figure 9. Jammer inserted between motherboard and add-in card

N5323A Jammer Specifications

System requirements

The N5323A is a standalone PCI Express card form factor. The software application that controls the N5323A card runs on a Windows XP or Windows 7 PC host connected via a USB 2.0 link.

Environment	
Temperature (AT-ETM757)	Operating: 0 °C to +55 °C Storage: –40 °C to +70 °C
Humidity (AT-ETM758)	Operating: 15 to 95% Operating soak: 90% (24 h)
Safety standards	Installation category: EN ISO/IEC 17025, IEC 61010-1/EN61010-1, II Pollution degree: 2 Environmental rating: Standard

General characteristics					
Power requirements	100-240 Vac 130-160 VA 1.5 A 47 to 63 Hz	maximum			
Form factor	PCI Express half Component heigh		gth: 168 mm (6.6 incl luding heat sink: 19 i	,	mm (7.1 inch)
Connectors	Front bracket USB type B Vin 18 V DC, 3.5 A PCle analysis output, proprietary	Top connector PCIe, connector x16, maximum x8 lane connection	Bottom connector • PCle x1, x4 or x8 (version dependent)	Trigger in/out LVCMOS 3.3 V, see user guide Vin maximum 4.6 V	Power in ATX power connector to supply the top connector
SSC	Supported				
Data memory	128 kB				

Electrical characteristics						
Data in	Input levels • Minimum: 100 mV • Maximum: 1.2 V	litter tolerar Compliant Specificat Rev 0.9	t to PCle	Frequency • Minimum: 2.5 GHz ±3 5 GHz ±30 • Maximum: 2.5 GHz +3 5 GHz +3	0 ppm 300 ppm;	SSC support None
Data out	Output level Minimum: 800 mV (full swing) Typical: 1000 mV Maximum: 1.2 V		De-emphasis 3.5 dB • Typical: 3.5 dB		De-emphasis 6 dB • Typical: 6.0 dB	
	UI interval • Minimum: –300 ppm*UI		• Typical: 0.3 UI		• Typical: 20 mV	
	Maximum: +300 ppm*U		. , p		. , , , ,	
External clock in	Minimum level: 800 mVdiff Maximum level: 1200 mVdiff AC coupled Frequency: 100 MHz					
Reference clock in	Compliant to PCIe Specific	cation 2.0				

N4241A/2A/3A Full Size Mid-bus Probe

Features

The Agilent mid-bus 2.0 Series of probes using soft touch technology, are specially designed to provide support for up to 16-channel probing and give insight to the system without influencing it.

General

- Three types of mid-bus probes; straight (N4241A), swizzled x16 (N4242A), split x4 (N4243A)
- · Mid-bus interposers available for all link width and link types
- 5 ft cable length for flexible setup between analyzer and test system
- Each mid-bus probe ships with five retention modules, and extras can be ordered with E2960B-RET-05



Figure 10. N4241A/2A/3A mid-bus probe



Figure 11. Mid-bus probe head



Figure 12. Mid-bus interposer

N4241A/2A/3A Full Size Mid-bus Probe Specifications

See mid-bus probe manual for a more detailed description.

Environment	
Temperature (AT-ETM757)	Operating: 0 °C to +40 °C Storage: -40 °C to +70 °C
Humidity (AT-ETM758)	Operating: 15 to 95% Operating soak: 90% (24 h)
Safety standards	Installation category: EN ISO/IEC 17025, IEC 61010-1/EN61010-1, II Pollution degree: 2 Environmental rating: Standard
Airflow	140 linear feet per minute for a single probe with no heat source within 1 inch distance 200 linear feet per minute for 2 probes placed side to side with minimum spacing
General characteristics	
Probe tip	Width : 3.6 cm (1.40 inch) Depth : 1.5 cm (0.60 inch) Height : 6.7 cm (2.62 inch) Weight: 0.75 kg (1.65 lbs)
Probe cable	Length : 1.5 m (59.06 inch) Weight : 0.75 kg (1.65 lbs)
Electrical characteristics	
Absolute maximum ratings	Amplitude data signal: 2 V _{ppdiff} Amplitude ref. CLK: 5 V _{ppdiff}
Jitter tolerance	Eye width: 0.6 UI (minimum) Trace length transmitter: 9 inch (maximum for worst case scenario)
Capacitive loading	150 fF
Data signals	Frequency • Minimum: 2.5 GHz —300 ppm 5 GHz —300 ppm • Maximum: 2.5 GHz +300 ppm 5 GHz +300 ppm Eye opening minimum: 60 mV (eye width of 0.6 UI) Maximum input amplitude: 1600 mV _{ppdiff} (eye width of 0.85 UI)
Ref. CLK*	Amplitude • Minimum: 800 mV ppdiff • Maximum: 2000 mV ppdiff DC offset • Minimum: 0 mV • Maximum: 500 mV Frequency • Minimum: 100 MHz -300 ppm • Maximum: 100 MHz +300 ppm SSC • Minimum: -0.5% • Maximum: 0%

N5328A Half Size Mid-bus Probe

Features

The half size mid-bus probe 2.0 supports up to 8 channels (x4 bi-directional), and is especially designed for mobile or embedded applications where space is constrained. With a smaller footprint, this probe allows for easier routing and board layout compared to the full size mid-bus probe.

General

- 5 ft cable length for flexible setup between analyzer and test system
- Each mid-bus ships with five retention modules, extras can be ordered N5328A-RET-05



Figure 13. N5328A half size mid-bus probe



Figure 14. Half size mid-bus probe head

N5328A Half Size Mid-bus Probe Specifications

See probe manual for a more detailed description.

Environment	
Temperature (AT-ETM757)	Operating: 0 °C to +40 °C
	Storage: -40 °C to +70 °C
Humidity (AT-ETM758)	Operating: 15 to 95%
	Operating soak: 90% (24 h)
Safety standards	Installation category: EN ISO/IEC 17025, IEC 61010-1/EN61010-1, II
	Pollution degree: 2
	Environmental rating: Standard
Airflow	140 linear feet per minute for a single probe with no heat source within 1 inch distance 200 linear feet per minute for 2 probes placed side to side with minimum spacing
General characteristics	
Probe tip	Width: 2.3 cm (0.91 inch)
	Depth : 1.5 cm (0.60 inch)
	Height: 6.4 cm (2.53 inch)
Probe cable	Length : 1.5 m (59.06 inch)
	Weight: 0.75 kg (1.65 lbs)
Electrical characteristics	
Absolute maximum ratings	Amplitude data signal: 2 V_{ppdiff} Amplitude ref. CLK: 5 V_{ppdiff}
Jitter tolerance	Eye width: 0.6 UI (minimum)
	Trace length transmitter: 9 inch (maximum for worst case scenario)
Capacitive loading	150 fF
Data signals	Frequency
	 Minimum: 2.5 GHz —300 ppm 5 GHz —300 ppm
	• Maximum: 2.5 GHz +300 ppm 5 GHz +300 ppm
	Eye opening minimum: 60 mV (eye width of 0.6 UI)
	Maximum input amplitude: 1600 mV _{ppdiff} (eye width of 0.85 UI)
Ref. CLK*	Amplitude
	• Minimum: 800 mV _{ppdiff}
	• Maximum: 2000 mV ppdiff
	DC offset
	• Minimum: 0 mV
	Maximum: 500 mV Froquency
	Frequency • Minimum: 100 MHz -300 ppm
	• Maximum: 100 MHz +300 ppm
	SSC
	• Minimum: –0.5%
	• Maximum: 0%

N4241F Flying Lead Probe

Features

, ,	ad probe 2.0 is designed to expose hard-to-reach signals for mobile and embedded systems, allowing nk at 5 Gb/s speeds without a designed-in connector.
General	 Each probe can monitor upto a x8 PCI Express link, and two probes can be combined for x16 links 5 ft cable length for flexible setup between analyzer and test system
Probe tip	 Socketed probe tip allows easy and reliable connection to resistors Amplification done outside of probe tip to ensure minimum size, and minimize thermal concerns

N4241F Flying Lead Probe Specifications

See flying lead probe manual for a more detailed description.

Environment	
Temperature (AT-ETM757)	Operating: 0 °C to +40 °C Storage: –40 °C to +70 °C
Humidity (AT-ETM758)	Operating: 15 to 95% Operating soak: 90% (24 h)
Safety standards	Installation category: EN ISO/IEC 17025, IEC 61010-1/EN61010-1, II Pollution degree: 2 Environmental rating: Standard
Airflow	140 linear feet per minute for a single probe with no heat source within 1 inch distance 200 linear feet per minute for 2 probes placed side to side with minimum spacing



Figure 15. Flying lead probe

N4241F Flying Lead Probe Specifications

General characteristics	
Probe cable	Length: 1.5 m (59.06 inch) Weight: 0.75 kg (1.65 lbs)
Probe tip characteristics	Socketed differential tip Dimensions • Flying leads length: 15 cm (5.91 inch) • Tip width: 4.71 mm • Tip length: 3.33 mm

Electrical characteristics	
Absolute maximum ratings	Amplitude data signal: 2 V_{ppdiff} Amplitude ref. CLK: 5 V_{ppdiff}
Jitter tolerance	Eye width: 0.65 UI (minimum) Trace length transmitter: 9 inch (maximum for worst case scenario)
Capacitive loading	200 fF
Data signals Note: These measurements are only valid when using Agilent-supplied resistors (E5381-82101).	Frequency • Minimum: 2.5 GHz –300 ppm 5 GHz –300 ppm • Maximum: 2.5 GHz +300 ppm 5 GHz +300 ppm Eye opening minimum: 75 mV (eye width of 0.65 UI) Maximum input amplitude: 1600 mV _{podiff} (eye width of 0.85 UI)
Ref. CLK	Amplitude • Minimum: 800 mV _{ppdiff} • Maximum: 2000 mV _{ppdiff} DC offset • Minimum: 0 mV • Maximum: 500 mV Frequency • Minimum: 100 MHz —300 ppm • Maximum: 100 MHz +300 ppm SSC • Minimum: -0.5% • Maximum: 0%

N4241Z ZIF Flying Leads Probe

Features

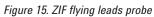
General	 The Agilent ZIF flying leads probe is designed with reliable signals and ease of probing access in mind, allowing access to the PCIe link at 5 Gb/s speeds without a designed in connector.
	 Also, by leveraging the Agilent infiniimax ZIF probe tip, it allows designers to use the same probe points for both physical layer Oscilloscope measurements well as logical/protocol measurements. Over 6 ft cable length for flexible setup between analyzer and test system
Probe tip	 Easy to connect and disconnect zero insertion force (ZIF) differential tip, to protect probe head and ensure many reuses Both N5426A and N5451A ZIF tips supported, to ensure maximum flexibility Amplification done outside of probe tip to ensure minimum size, and minimize thermal concerns

N4241Z Flying Lead Probe Specifications

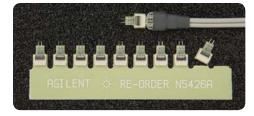
See flying lead probe manual for a more detailed description.

Environment	
Temperature (AT-ETM757)	Operating: 0 °C to +40 °C Storage: -40 °C to +70 °C
Humidity (AT-ETM758)	Operating: 15 to 95% Operating soak: 90% (24 h)
Safety standards	Installation category: EN ISO/IEC 17025, IEC 61010-1/EN61010-1, II Pollution degree: 2 Environmental rating: Standard
Airflow	140 linear feet per minute for a single probe with no heat source within 1 inch distance 200 linear feet per minute for 2 probes placed side to side with minimum spacing









N4241Z ZIF Flying Leads Probe Specifications

General characteristics	
Probe cable	Analyzer cable length: 1.5 m (59.06 inch) Weight: 0.75 kg (1.65 lbs)
Probe tip characteristics	Zero Insertion Force (ZIF) differential tip Dimensions • Flying leads length : 21 cm (8.27 inch) • Tip width : 5.54mm (0.218 inch) • Tip length : 10.5 mm (0.413 inch)

Electrical characteristics	
Absolute maximum ratings	Amplitude data signal: 2 V_{ppdiff} Amplitude ref. CLK: 5 V_{ppdiff}
Jitter tolerance	Eye width: 0.65 UI (minimum) Trace length transmitter: 9 inch (maximum for worst case scenario)
Capacitive loading	≤ 250 fF
Data signals Note: These measurements are only valid when using Agilent- supplied ZIF tip N5426A or N5451A	Frequency • Minimum: 2.5 GHz -300 ppm 5 GHz -300 ppm • Maximum: 2.5 GHz +300 ppm 5 GHz +300 ppm Eye opening minimum: 75 mV (eye width of 0.65 UI) Maximum input amplitude: 1600 mV _{podiff} (eye width of 0.85 UI)
Ref. CLK	Amplitude • Minimum: 800 mV _{ppdiff} • Maximum: 2000 mV _{ppdiff} DC offset • Minimum: 0 mV • Maximum: 500 mV Frequency • Minimum: 100 MHz —300 ppm • Maximum: 100 MHz +300 ppm SSC • Minimum: -0.5% • Maximum: 0%

N5315A Slot Interposer Probe Features

Interposer • Analog repeating slot interposer • Physical link width x1 x4 x8 x16

- Electrical Idle conditions are propagated by the slot interposer
- · Mechanical stabilization for the device under test
- Cable holders to prevent them from laying on top of DUT or backplane
- Mechanical Stabilization with backplane to ensure firm PCle slot connection
- Power management capabilities (15-35 FTS)



Figure 16. N5315A slot interposer probe

N5315A Slot Interposer Probe Specifications

Environment	
Temperature (AT-ETM757)	Operating: 0 °C to +55 °C Storage: 40 °C to +70 °C
Humidity (AT-ETM758)	Operating: 15 to 95% Operating soak: 90% (24 h)
Safety standards	Installation category: EN ISO/IEC 17025, IEC 61010-1/EN61010-1, II Pollution degree: 2 Environmental rating: Standard

General characteristics	s
Display	4-character LED display status
LED	Two status LEDs
Power requirements	100-240 Vac 130-160 VA 1.5 A maximum 47 to 63 Hz
Form factor	Length: 195.8 mm (7.71 inch) Height: 169.5 mm (6.67 inch)
Probe cable length	1.0 m (39.37 inch)
Connector	Front bracket: Vin 18 V DC, 3 A Top connector: PCle, connector x16 Bottom connector: PCle, x1, x4, x8 or x16 (version dependent)

Electrical characteristics	
Absolute maximum ratings	Amplitude data signal: 2 V ppdiff Amplitude ref. CLK: 5 V ppdiff
Jitter tolerance	Eye width: 0.6 UI (minimum) Trace length transmitter: 9 inch (maximum for worst case scenario)
DUT path	Added jitter: below 0.1U Output voltage level: 100 to 110% of the input signal Delay: 1200 psec Lane-to-lane skew: below 30 psec
External clock level	Minimum: 800 mV diff Maximum: 2000 mV diff AC coupled frequency: 100 MHz

N5316A Passive Backplane

Features

General	Provides power and clock to DUT Test fixture for add-in card testing with exerciser
Power	 Separate power on/off for fast reset in tests Power reset AUX (stand by) power for add-in card available if required Per bus power switch
Link width	All link widths are supported
Clocks	Clock generation with/without SSC Input for external clock Clock output (e.g. for scope measurements) Supports different mid-bus probes N4241A/2A/3A Reset/power button
Connectors	 Bus 1 One pair of x16 PCle connectors Two x8 mid-bus probe retention modules with bidirectional footprint supporting N4242A (x16), N4241A (x1, x4, x8), N4243A (dual x4) Bus 2 One x16 PCle connector with loop back Bus 3 One pair of x16 PCle connectors Two x8 mid-bus probe retention modules with unidirectional footprint supporting two N4241A (x1, x4, x8, x16)



Figure 17. Passive backplane

N5316A Passive Backplane Specifications

Environment		
Temperature (AT-ETM757)	Operating: 0 °C to +55 °C Storage: –40 °C to +70 °C	
Humidity (AT-ETM758)	Operating: 15 to 95%	
Safety standards	Installation category: EN ISO/IEC 17025, IEC 61010-1/EN61010-1, II Pollution degree: 2 Environmental rating: Standard	

Power requirements	100-240 Vac
•	10/6A
	47 to 63 Hz
Connectors	5x PCI Express x16 physical connector
	Five mid-bus probe retainers to hold N4241A/2A/3A mid-bus probes
	DUT power connector
Dimensions	Length: 30.5 cm
	Width: 24.5 cm
	Height: 13.5 cm excluding rear cover
	Weight: approximately 5 kg

Electrical characteristics	
Slot supply voltages	Maximum power rating • +12 V/5.5 A per PCI slot • +3.3 V/3.0 A per PCI slot
Connectors	Power out connector Disk drive power connector 12 V 5.5 A maximum 5 V 3 A maximum
Clocks	SMA external clock input • 800 mVpp AC coupled onboard SMA clock output • Terminate into 50 0hm • Level: typically 800 mVpp Reference clock at PCI connectors • According PCI Express Specification 2.0 Rev 0.9 • Frequency 100 MHz ± 300 ppm SSC supported • 30 KHz triangle waveform is used with 0.5% down-spread

N5313A P2L Gateway Cable Specifications

General	 Make the Agilent logic analyzer and E2960B PCI Express protocol analyzer one complete tool
	 Full view of interaction between busses monitored by the logic analyzer and the PCI Express bus
GUI	 Time correlated views between the logic analyzer and protocol analyzer Shared markers between both instruments
Triggering	Cross triggering between the logic analyzer and protocol analyzer
Connectors	 Connects to the PCI Express module 3 BNC connects to the 16900 logic analyzer module

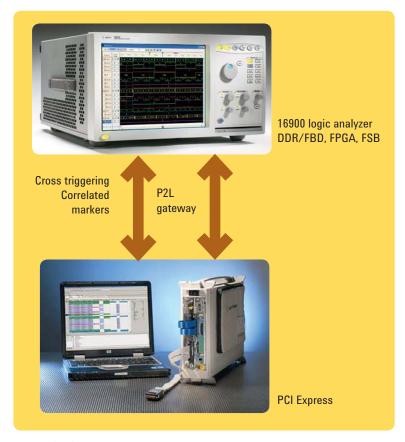


Figure 18. PCI Express to logic correlated system



Figure 19. N5313 P2L gateway cable



Figure 20. P2L system viewing

N5319A P2L Gateway Cable with Flag Support Specifications

General	 Make the Agilent logic analyzer and E2960B PCI Express protocol analyzer one complete tool
	 Full view of interaction between busses monitored by the logic analyzer and the PCI Express bus
GUI	 Time correlated views between the logic analyzer and protocol analyzer Shared markers between both instruments
Triggering	 Cross triggering between the logic analyzer and protocol analyzer Ping pong triggering between logic analyzer and protocol analyzer through flag support. Four flags supported
Connectors	 Connects to the PCI Express protocol analyzer Connects to the 16900 logic analyzer module

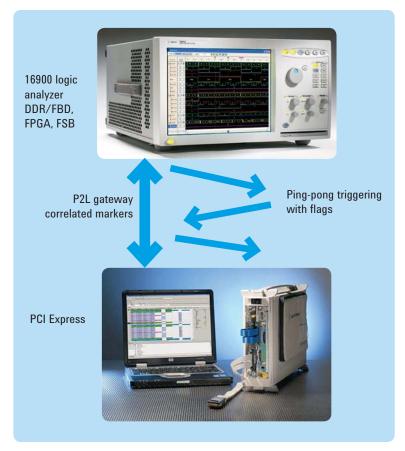


Figure 21. PCI Express



Figure 22. N5319A P2L gateway cable with flag support



Figure 23. P2L system viewing

Related Products N5302A (2 Slot) or N5304A (4 Slot) Chassis

Environment	
Temperature (AT-ETM757)	Operating: 0 °C to +55 °C Storage: -40 °C to +70 °C
Humidity (AT-ETM758)	Operating: 15 to 95% Operating soak: 90% (24 h)
Safety standards	Installation category: EN ISO/IEC 17025, IEC 61010-1/EN61010-1, II Pollution degree: 2 Environmental rating: Standard

General characteristics	3	
Power requirements	100-120 Vac 200-250 Vac 550 VA maximum 47 to 63 Hz	

Physical characteris	tics
2-slot chassis	Width: 30 cm (11.81 in) Depth: 49.0 cm (19.29 in) Height: 11 cm (4.33 in) Weight (empty): 5.1 kg (112 lbs)
4-slot chassis	Width: 45.4 cm (17.87 in); mounts in EIA-standard 48.3 cm (19 in) rack Depth: 49.0 cm (19.29 in) Height: 2U - 8.89 cm (3.5 in) Weight (empty): 5.1 kg (112 lbs)

Connectors	
MDI	RJ-45; 100 Mb/s ethernet (to PC controller)
MDI-X	RJ-45; 100 Mb/s ethernet (to next chassis)
AT hard drive power	Connector on probe board (uses 12 V only)
External trigger in	Female BNC; trigger input from external device
External trigger out	Female BNC; trigger output from external device

Related Agilent Literature

Publication title	Pub number
The Agilent Test Portfolio for PCI Express 2.0 Brochure	5989-5594EN
Agilent E2960B Series for PCI Express 2.0 x1 through x16 Gen 2 Ready Program Photo card	5989-6395EN
Agilent E2969B Protocol Test Card for PCI Express 2.0 Photo card	5989-7594EN
Agilent E2969A Protocol Test Card for PCI Express Photo card	5989-9520EN
Agilent PCI Express Jammer Brochure	5990-3222EN
PCI Express Probes for Agilent E2960B PCI Express Analysis Systems Brochure	5990-4123EN
Agilent Digital Test Console PCI Express 3.0 Data Sheet	5990-5018EN

Ordering Information Protocol Analyzer

Hardware	Description
N5306A	Analyzer module for PCIe 5 Gb/s
N5322A	Extended interface module for PCIe 5 Gb/s

	Description
N5306A-A01	Analyzer SW license x1 for PCIe 5 Gb/s
N5306A-A04	Analyzer SW license x4 for PCIe 5 Gb/s
N5306A-A08	Analyzer SW license x8 for PCIe 5 Gb/s
N5306A-A16	Analyzer SW license x16 for PCIe 5 Gb/s
N5306A-G01	Gen2 Ready analyzer SW license x1 for PCle 2.5 Gb/s
N5306A-G04	Gen2 Ready analyzer SW license x4 for PCle 2.5 Gb/s
N5306A-G08	Gen2 Ready analyzer SW license x8 for PCle 2.5 Gb/s
N5306A-G16	Gen2 Ready analyzer SW license x16 for PCIe 2.5 Gb/s
	N5306A-A04 N5306A-A08 N5306A-A16 N5306A-G01 N5306A-G04 N5306A-G08

ectional x8 for PCle 5 Gb/s ed x16 for PCle 5 Gb/s
ed x16 for PCle 5 Gb/s
it x4 for PCle 5 Gb/s
ectional x8 for PCle 5 Gb/s
Gb/s link width x1
Gb/s link width x4
Gb/s link width x8
Gb/s link width x16
PCIe 2.5 Gb/s for N4241A
robe board
robe board
robe board
nid-bus probe for PCI-Express
ctional x8 for PCle 2.5 Gb/s
ctional x8 for PCIe 2.5 Gb/s
ole set for PCI Express 2.5 Gb/s
able (connect Gen1 probes to Gen2 systems)

Accessories		Description
	N5302A	2-slot portable chassis
	N5304A	4-slot chassis
	E2960B-LAN	USB to LAN adapter for chassis to controller connectivity
	E2960B-RET-05	Retention modules for mid-bus probe 2.0 - 5 pcs
	E2960B-RET-50	Retention modules for mid-bus probe 2.0 - 50 pcs
Logic analyzer to protocol analyzer correlation accessories	N5313A	P2L gateway cable to connect 16900A to E2960B analyzer
	N5319A	P2L gateway cable with flags to connect 16900A to E2960B analyzer

Ordering Information Exerciser

Hardware	Description
N5309A-E01	Half size exerciser and LTSSM module x1 for PCle 5 Gb/s
N5309A-E04	Half size exerciser and LTSSM module x4 for PCle 5 Gb/s
N5309A-E08	Half size exerciser and LTSSM module x8 for PCle 5 Gb/s
N5309A-E16	Half size exerciser and LTSSM module x16 for PCle 5 Gb/s

Software		Description
Gen2 exerciser software	N5309A-EX2	Exerciser SW license: exerciser and LTSSM at 5 Gb/s
Gen2 Ready exerciser software	N5309A-EX1	Gen2 Ready exerciser SW license: exerciser and LTSSM at 2.5 Gb/s
Compliance tests N53	N5309A-PTC	Exerciser SW license: protocol test cards software (included with exerciser purchase)
	N5309A-COM	Exerciser SW license: compliance assured test package (over 170 pre-defined tests)

Accessories		Description
	N5316A	Test backplane for PCle2

Protocol Test Cards		Description
PTC1	E2969A	Protocol test card for PCI Express Gen 1 (includes software and hardware)
PTC2	E2969B	Protocol test card for PCI Express Gen 2 (includes software and hardware)

Jammer

Harware		Description
	N5323A-J01	Jammer module x1 for PCIe 5Gb/s
	N5323A-J04	Jammer module x4 for PCIe 5Gb/s
	N5323A-J08	Jammer module x8 for PCIe 5Gb/s

Software		Description
	N5323A-JM1	Gen2 Ready Jammer SW license: Jammer at 2.5 Gb/s
	N5323A-JM2	Jammer SW license: Jammer at 5Gb/s
	N5323A-SCR	Jammer SW license: Jammer scripts

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Revised: June 8, 2011

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