Agilent U1062A

Acqiris High-Speed PXI Digitizers

DC152: 10-bit, 2 ch, up to 2 GHz, 2-4 GS/s
DC122: 10-bit, 1 ch, 2 GHz, 4 GS/s

Agilent Technologies

Main Features

- **Dual- and single-channel 10-bit digitizers with up to 4 GS/s sampling rate**

- **Choice of fully-featured mezzanine front end, with internal calibration and input protection, offering 50Ω or 1 MΩ input impedance, with up to 2 GHz analog bandwidth**

- **Large 512 kSample acquisition memories expandable to 64 or 512 MSample (optional)**

- **Multi-module synchronization with auto-synchronous bus system for distribution of trigger and clock signal**

- **Device drivers for Windows®, VxWorks, LabViewRT, and Linux, with application code examples for MATLAB®, C/C++, Visual Basic, LabVIEW, and LabWindows/CVI**

Acqiris High-Speed Digitizers

The proprietary ADC chipsets in Agilent Technologies Acqiris high-speed digitizers are designed for the specific purpose of optimizing high-speed ADC performance. The analog front-end technology provides the signal conditioning, amplification, and interleaving functions essential to achieving high-speed data acquisition at GS/s rates. The digital data handling components provide vital clock and synchronization signals, to capture and memorize acquired data with maximum data throughput. Together these ASICS make low-power, high-fidelity data acquisition much more accessible and provide maximum data throughput to the host PC or processor to reduce the time and cost of measurement.

The Acqiris product line provides a range of high-speed digitizer cards[1] with 8-, 10-, and 12-bit resolution, wide bandwidths, and large acquisition memory. These products, in PCI, PXI, cPCI, and VME formats, are used in research, and in ATE and OEM applications in industries such as biotechnology, semiconductors, aerospace, physics, and astronomy.

1) 500 MS/s, 1 GS/s, 2 GS/s, 4 GS/s and 8 GS/s high-speed digitizer cards.

High-Resolution High Sample Rate Signal Acquisition

Agilent Acqiris high-speed PXI digitizers (U1062A) significantly increase data acquisition and testing rates, achieving an impressive single-channel sampling rate of up to 4 GS/s. The sampling rate of these digitizers, in combination with an input bandwidth of up to 2 GHz, make them ideal for high-speed applications such as telecommunications, ATE, and semiconductor testing, where test time should be limited only by the speed limits of the device under test (DUT). These high-precision, high-speed digitizers become the optimized data conversion component in synthetic instrumentation systems, for the replacement of standard digital multimeters, oscilloscopes, power meters, and frequency counters in RF and microwave test systems.

The DC152, with up to 2 GHz of bandwidth, provides synchronous sampling of 2 GS/s on both input channels – in single-channel applications this doubles to 4 GS/s. The single-channel DC122 offers sampling rates of up to 4 GS/s.

These digitizers are compliant with both the PXI and CompactPCI standards, and combine ultra-fast sampling and wide analog bandwidths with standard 512 ksample acquisition memories and optional 512 Msample acquisition memories [2].

Multiple Front-End Options

As with other Acqiris products, the entire front-end is mounted on a removable mezzanine card. In the event of accidental damage, or as relays fatigue over time, replacement is fast and efficient. The U1062A single- or dual-channel front-end mezzanines feature internal calibration and a choice of BNC or SMA connectors.

The 50 Ω input stage is fully protected against overvoltage signals. The programmable front-end electronics are used to provide a complete set of input voltage ranges, from 50 mV to 5 V full scale (in a 1, 2, 5 sequence) with variable voltage offset. With a bandwidth of 2 GHz, the digitizers provide optimized amplifier response. Flatness, overshoot, and accuracy are optimized to ensure precise high-frequency measurements.

The dual-channel switchable 50 Ω/1 MΩ input stage (for U1062A-002 only) offers the same input protection and programmable front-end electronics. With It features input voltage ranges, from 50 mV to 50 V full scale (in a 1, 2, 5 sequence) with variable voltage offset, and a bandwidth of 1.4 GHz into 50 Ω and > 300 MHz (typ.) into 1 MΩ.

Front-end option	Impedance	Bandwidth	Full scale range
50 Ω (U1062A-F50 and U1062A-2F5)	50 Ω	2 GHz	50 mV, 100 mV, 200 mV, 500mV, 1 V, 2 V, and 5 V
50 Ω / 1 MΩ (U1062-2FZ)	50 Ω	1.4 GHz	50 mV, 100 mV, 200 mV, 500mV, 1 V, 2 V, and 5 V
	1 MΩ	>300 MHz (typ.)	50 mV, 100 mV, 200 mV, 500mV, 1 V, 2 V, 5 V ,10 V, 20 V, and 50 V

2) Shared between input channels of the DC152.

Extended Functionality

Multi GHz bandwidth front-end

The front-end mezzanines include a proprietary front-end amplifier chip. This integrated circuit includes a programmable gain amplifier (PGA) with on-chip filtering and trigger circuitry. It provides pre-ADC signal conditioning and amplification, essential for high performance high-speed data conversion systems. The filter section, which is useful for signal noise reduction, allows 2-pole Bessel bandwidth limiting at 700 MHz and 200 MHz.

Trigger mezzanine with Ctrl I/O

Ctrl I/O

The trigger mezzanine also includes the proprietary front-end amplifier chip. The trigger processing circuit embedded in the package includes
  • Dual comparators for window triggering mode
• On-chip DACs for threshold adjustment
• Additional filters for LF and HF reject trigger coupling
• A prescaler to allow an HF divide-by-four mode

The trigger mezzanine has a standard 50 Ω terminated BNC or SMA connector and the Ctrl I/O connectors. These four front-panel MMCX connectors provide access for an external clock or 10 MHz reference signal, a trigger output, and two additional I/O digital control lines (I/O A and B) for monitoring or modifying the digitizer's status and configuration or extracting a 10 MHz clock signal.

Auto-synchronous bus system

AS bus 2

If more than two synchronous data acquisition channels are required, several digitizers can be combined using the second generation high-bandwidth auto-synchronous bus system (AS bus 2). The system provides superior synchro-nization to the standard 10-MHz PXI reference clock. AS bus 2 connects up to three U1062A modules.

PXI Compliance for Modular Instrumentation

The U1062A digitizer is PXI compliant. Designed to benefit from fast data interfaces, the products can be integrated with other test and automation modules in both PXI and CompactPCI chassis.

The PXI format offers high performance in a small, rugged package. It is an ideal deployment platform for many automated test systems. A wide array of complementary PXI products are currently available, including multimeters, waveform generators, and switch multiplexers.

Figure 1: High-speed U1062A-002 PXI digitizer

Fast data throughput with large memory

The memory and acquisition controller component is a digital CMOS integrated circuit. A high-speed data demultiplexer with on-board memory it is designed for the capture of 10-bit digital data at speeds up to 2 GS/s. It includes large internal static RAM, high clock frequencies, and is able to accept and generate LVDS levels [3] for fast I/O signals.

The two IC's on the digitizer each allow storage of the input data stream to a self-addressed, 10-bit, 256 ksample internal memory. The digitizer has provision for a 512 Msample external memory expansion. This acquisition memory is divided between the active input channels.

Precise channel interleaving

The cross point switch chip is a matrix of analog multiplexers. It includes a calibration input, essential for the accurate timing calibration of several interleaved ADCs, and allows offset matching with four dedicated on-chip, 8-bit DACs.
The interleaving of multiple ADCs is essential for high-speed data conversion systems. The process increases the effective sample rate in high-speed digitizer systems by acquiring the same signal on two or more ADCs in parallel and out of phase. These acquired signals are then reordered and recombined, by the memory and acquisition controller, to reconstruct the signal waveform.

Reference clock and synchronization

The integrated circuit that handles the ADC clock distribution circuit also includes trigger functions that facilitate high-performance triggering. The chip is used with the memory and acquisition controller for interleaving 2 high-speed ADCs to achieve unmatched high-speed data acquisition.

Easy Software Integration

Agilent's high-speed Acqiris digitizers are supplied with software drivers for Windows, Linux, LabVIEW RT, and VxWorks, and application code examples for MATLAB, C/C++, VisualBasic, LabVIEW, and LabWindows/CVI. These code examples provide digitizer set up and basic acquisition functionality, and are easily modified, so that the card can be quickly integrated into a measurement system.
The flexibility of the driver means that, with minimum software adjustments, any Acqiris digitizer can be swapped out, replaced, or upgraded with the latest high-speed Acqiris digitizer.

3) Low-voltage differential signal, with a range of 100 mV to 600 mV.

Acqiris High-Speed PXI Digitizers

Model DC152

Dual-channel, 10-bit, 2 GHz, 2-4 GS/s

Model DC122

Single-channel, 10-bit, up to 2 GHz, 4 GS/s

Signal input 50Ω (-2F5 and -F50 Front-end option)

Channels
U1062A-001: Single at 4 GS/s
U1062A-002: Dual at 2 GS/s, Single at 4 GS/s

Bandwidth (-3 dB)
DC to 2 GHz

Full scale (FS)
50 mV to 5 V

Offset range
± 2 V for 50 to 500 mV FS
± 5 V for 1 to 5 V FS

Bandwidth limit filters
700 MHz, 200 MHz and 20 MHz

Maximum input voltage
± 5 V DC

Coupling
DC, AC (32 Hz LF limit, 50 Ω)

Impedance
50 Ω ± 1% at DC

Connectors
BNC or SMA, gold plated

SFDR (typ.)
60 dB at 10.5 MHz
36 dB at 951 MHz

SNR (Full BW, 2 GS/s)
> 32 dB at 50 mV FS
> 36 dB at 100 mV FS
> 38 dB at 1 V FS
> 39 dB at 200 mV, 2 V, 5 V FS

DC accuracy
± 2.5% FS at 50 mV FS
± 2% FS at ≥ 100 mV FS

Effective bits (at 2 GS/s)
> 6.8 at 10.7 MHz, 20 MHz BWL
> 6.5 at 99.5 MHz, 200 MHz BWL
> 6.3 at 407 MHz, 700 MHz BWL
> 4.8 at 910 MHz, full BW (all sampling rates)

High-impedance input: 50 Ω/1 MΩ (-2FZ front-end option)

Channels
U1062A-001: not supported
U1062A-002: Dual at 2 GS/s, Single at 4 GS/s

Bandwidth (-3 dB)
50 Ω: DC to 1400 MHz
1 MΩ: DC to >300 MHz (typ.)

Full scale (FS)
50 Ω: 50 mV to 5 V
1 MΩ: 50 mV to 50 V

Offset range
50 Ω: ± 2 V for 50 to 500 mV FS
50 Ω: ± 5 V for 1 to 5 V FS
1 MΩ: ± 2 V for 50 to 500 mV FS
1 MΩ: ± 20 V for 1 to 5 V FS
1 MΩ: ± 200 V for 10 to 50 V FS

Bandwidth limit filters
50 Ω: 700 MHz, 200 MHz, 20 MHz
1 MΩ: 20 MHz, 200 MHz at ≤ 5 V FS
1 MΩ: 20 MHz at > 5 V FS

Maximum input voltage
50 Ω: ±5 V DC
1 MΩ: ±300 V DC

Impedance
50 Ω ± 1.0 % at DC
1 MΩ ± 1.0 % at DC // 18 ± 3 pF

Coupling
DC, AC

SFDR (typ. at 2 GS/s, 50 Ω)
62 dB at 10.9 MHz
44 dB at 400 MHz

SNR (50 Ω and 1 MΩ)
> 36 dB at 50 mV FS
> 38 dB at ≥ 100 mV FS

DC accuracy
± 2.5% FS at 50 mV FS
± 2% FS at ≥ 100 mV FS

Effective bits (at 2 GS/s)
50 Ω: > 6.8 at 10.7 MHz, 200 MHz BWL
1 MΩ: > 6.5 at 10.7 MHz, 200 MHz BWL
50 Ω: > 6.0 at 99.5 MHz, 700 MHz BWL
50 Ω: > 5.0 at 407 MHz, 700 MHz BWL

Digital conversion

Sample rate
10 MS/s to 2 GS/s in 1, 2, 2.5, 5 sequence and 4 GS/s

Resolution
10 bits (1:1024)

Integral nonlinearity (typ.)
< ± 0.3% FS (typ.) at 1.8 MHz

Differential nonlinearity (typ.)
< 2 LSB (typ.)

Acquisition memory
DC152: 256 kSample/channel
DC122: 512 kSample

Maximum optional memory
DC152: 256 MSample/channel
DC122: 512 MSample

Time base

Clock accuracy
Better than ± 2 ppm

Sampling jitter
1.2 ps RMS (typ.) for 10 µs with internal clock and reference

Acquisition modes
Single shot, Start-on-trigger, Sequence mode (1 to 1000 segments with standard memory, dead time 350 ns at 2 GS/s, **16,000** segments with memory **-M64** option, 1.8 µs dead time at 2 GS/s, **125,000** segments with **-512** memory option, 1.8 µs dead time at 2 GS/s)

Trigger time interpolator
15 ps resolution

Internal and external trigger

Internal trigger input

Trigger frequency range
DC to 1 GHz for positive, negative,
window or pattern trigger,
DC to 2 GHz in HF mode
Threshold adjust range: FS of channel
Amplitude range: > 15% FS

External trigger input
Impedance: 50 Ω ± 1%
Trigger frequency range:
DC to 1 GHz for positive, negative,
window or pattern trigger,
DC to 2 GHz in HF mode
Full Scale: 0.5, 1, 2, 5 V
Threshold Adjust Range: ± FS/2
Maximum input voltage: ± 5 V DC
Amplitude range: >15% FS

Coupling
DC, AC LF reject (50 Hz), HF reject
(50 kHz)

Modes
Edge, positive and negative
HF: divide by 4
Spike Stretcher
Window In/Out
Pattern

Pre-trigger
Adjustable to 100% of horizontal full
scale

Post-trigger
Adjustable up to 2^{35} -1 sample

Control I/O

I/O A & B signals
TTL and CMOS compatible (3.3 V)

Ctrl I/O A & B input
Trigger enable

Ctrl I/O A & B output
10 MHz reference clock
Acquisition skipping to next segment
Acquisition active
Trigger ready

CLK IN input
200 MHz to 2 GHz
> 500 mV pk-pk into 50 Ω
± 5 DC max voltage

CLK IN ext. clock/ref threshold
Variable between -3 V and +3 V

CLK IN ext. reference frequency
10 MHz ± 0.3 %

TRG OUT output level
Adjustable in range ± 2.5 V (no load)
Amplitude ±0.8 V (no load), ± 15 mA max

TRG OUT rise/fall time
2.5 ns into 50 Ω

General

Host computer and operating system
PC running Microsoft Windows 7,
Windows Vista, Windows XP,
Wind River VxWorks,
National Instruments LabVIEW RT,
or Linux.
The following 64 bits operating systems are
also supported: XP64, Vista64, 7 64, Linux.
PowerPC systems running Wind River
VxWorks.
For more information on which specific
processors and operating system versions
are supported, please contact us.

Transfer speed
High-speed PCI bus transfers data at
sustained rates to host computer:
Up to 100 Mbytes/s for 32-bit/33 MHz
operation

Power consumption
< 35 W without memory option
< 44 W with memory option

Current requirements (max.)[4]
Without memory option:
 +12 V   0.12 A
+5 V4.0 A
+3.3 V   3.9 A
-12 V   0.015 A

With memory option:
+12 V   0.12 A

+5 V4.0 A
+3.3 V   6.8 A
-12 V   0.015 A

Front-Panel LEDs indicate digitizer status
Green: ready for trigger
Yellow: module identification
Red: trigger

Warranty
1 year

Environmental and physical

Operating temperature
0° to 40°C

Required airflow
> 2 m/s in situ

Relative humidity
5 to 95% (non-condensing)

Safety
Complies with EN61010-1

EMC immunity
Complies with EN61326-1 Industrial
Environment

EMC emissions
Complies with EN61326-1 Class A for
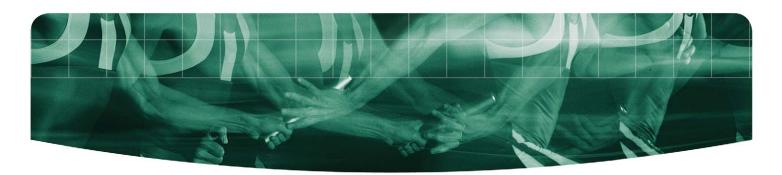radiated emissions

Dimensions
3U PXI/CompactPCI standard
100 mm x 160 mm x 20 mm

Front panel complies with IEEE1101.10
Certification and Compliance

4) U1062A all ADCs sampling at 2 GS/s.

Contacts

Agilent Acqiris Product Information

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Asia-Pacific	**61 3 9210 2890**
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Additional Agilent Contact Information

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Belgium	32 (0) 2 404 93 40
Denmark	45 70 13 15 15
Finland	358 (0) 10 855 2100
France	0825 010 700*
	*0.125 €/minute
Germany	49 (0) 7031 464 6333
Ireland	1890 924 204
Israel	972-3-9288-504/544
Italy	39 02 92 60 8484
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Other European Countries:
www.agilent.com/find/contactus

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Ordering Information

Model	Description
U1062A	Acqiris DC152 and DC122 high-speed 10-bit PXI digitizer
U1062A-001	Single-channel, 4 GS/s, 512 kSample, DC122
U1062A-002	Dual-channel, 2-4 GS/s, 256-512 kSample, DC152
U1062A-F50	Single channel 50 ohm, 2 GHz front-end
U1062A-2F5	Dual channel 50 ohm, 2 GHz front-end
U1062A-2FZ	Dual channel 50 ohm/1 Mohm, 1 GHz/300 MHz front-end
U1062A-512	512 MSample acquisition memory
U1062A-M64	64 MSample acquisition memory

Accessories

U1093A-AS5	AS bus 2 connector
U1062A-UK6	Calibration Certificate and Cal Data

www.agilent.com

For more information on Acqiris product line, sales
or services, see our website at:
www.agilent.com/find/acqiris
www.agilent.com/find/u1062a

Product specifications and descriptions in this document
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