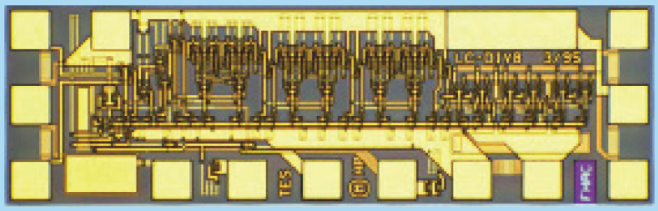
Agilent HMMC-3028
DC–12 GHz High Efficiency GaAs HBT MMIC Divide-by-8 Prescaler
1GC1-8008

Data Sheet

Description

The HMMC-3028 GaAs HBT MMIC prescaler offers DC to 12 GHz frequency translation for use in communications and EW systems incorporating high-frequency PLL oscillator circuits and signal-path down conversion applications. The prescaler provides a large input power sensitivity window and low phase noise. In addition to the features listed above, the device offers an input disable contact pad to eliminate any self-oscillation condition.



Chip size:	1330 x 440 µm (52.4 x 17.3 mils)
Chip size tolerance:	± 10 µm (± 0.4 mils)
Chip thickness:	127 ± 15 µm (5.0 ± 0.6 mils)
Pad dimensions:	70 x 70 µm (2.8 x 2.8 mils)

Features

- Wide frequency range:
  0.2 to 12 GHz
- High input power sensitivity:
  On-chip pre- and post-amps
  –20 to +10 dBm (1-8 GHz)
  –15 to +10 dBm (8-10 GHz)
  –10 to +5 dBm (10-12 GHz)
- Dual-mode P_{out}: (chip form)
  0 dBm (0.5 V_{p-p}) @ 44 mA
  –6.0 dBm (0.25 V_{p-p}) @ 34 mA
- Low phase noise:
  –153 dBc/Hz @ 100 kHz offset
- (+) or (–) single supply bias operation
- Wide bias supply range:
  4.5 to 6.5 volt operating range
- Differential I/0 with on-chip 50 Ω matching

Absolute maximum ratings[1]

(@ T_A = 25 °C, unless otherwise indicated)

Symbol	Parameters/conditions	Min.	Max.	Units
V_{CC}	Bias supply voltage		+7	Volts
V_{EE}	Bias supply voltage	–7		Volts
$V_{CC} – V_{EE}$	Bias supply delta	0	+7	Volts
$V_{Disable}$	Pre-amp disable voltage	V_{EE}	V_{CC}	Volts
V_{Logic}	Logic threshold voltage	V_{CC} –1.5	V_{CC} –1.2	Volts
$P_{in(CW)}$	CW RF input power		+10	dBm
V_{RFin}	DC input voltage (@ RF_{in} or $\overline{RF}_{in}$ ports)		V_{CC} ± 0.5	Volts
T_{BS}[2]	Backside operating temperature	–40	+85	°C
T_{st}	Storage temperature	–65	+165	°C
T_{max}	Maximum assembly temperature (60 seconds max.)		310	°C

1. *Operation in excess of any parameter limit (except T_{BS}) may cause permanent damage to the device.*
2. *MTTF > 1 x 10^6 hours @ T_{BS} ≤ 85 °C. Operation in excess of maximum operating temperature (T_{BS}) will degrade MTTF.*

DC Specifications/Physical Properties

(T_A = 25 °C, $V_{CC} - V_{EE}$ = 5.0 volts, unless otherwise listed)

Symbol	Parameters/conditions	Typ.	Min.	Max.	Units
$V_{CC} - V_{EE}$	Operating bias supply difference[1]	5.0	4.5	6.5	Volts
$\|I_{CC}\|$ or $\|I_{EE}\|$	Bias supply current (**HIGH** output power configuration:[2] $V_{PwrSel} = V_{EE}$)	44	37	51	mA
	Bias supply current (**LOW** output power configuration: V_{PwrSel} = open)	34	29	39	mA
$V_{RFin(q)}$ $V_{RFout(q)}$	Quiescent DC voltage appearing at all RF ports	V_{CC}			Volts
V_{Logic}	Nominal ECL logic level (V_{Logic} contact self-bias voltage, generated on-chip)	V_{CC} –1.32	V_{CC} –1.45	V_{CC} –1.25	Volts

1. Prescaler will operate over full specified supply voltage range, V_{CC} or V_{EE} not to exceed limits specified in absolute maximum ratings section.

2. High output power configuration: P_{out} = 0 dBm (V_{out} = 0.5 V_{p-p}). Low output power configuration: P_{out} = –6.0 dBm (V_{out} = 0.25 V_{p-p})

RF Specifications

(T_A = 25 °C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/conditions	Typ.	Min.	Max.	Units
$f_{in(max)}$	Maximum input frequency of operation	14	12		GHz
$f_{in(min)}$	Minimum input frequency of operation[1] (P_{in} = –10 dBm)	0.2		0.5	GHz
$f_{Self\text{-}Osc}$	Output self-oscillation frequency[2]	1.7			GHz
P_{in}	@ DC, (square-wave input)	> –25	–15	+10	dBm
	@ f_{in} = 500 MHz, (sine-wave input)	> –20	–15	+10	dBm
	f_{in} = 1 to 8 GHz	> –20	–15	+10	dBm
	f_{in} = 8 to 10 GHz	> –15	–10	+5	dBm
	f_{in} = 10 to 12 GHz	> –10	–5	–1	dBm
RL	Small-signal input/output return loss (@ f_{in} < 12 GHz)	15			dB
S_{12}	Small-signal reverse isolation (@ f_{in} < 12 GHz)	30			dB
Φ_N	SSB phase noise (@ P_{in} = 0 dBm, 100 kHz offset from a f_{out} = 1.2 GHz carrier	–153			dBc/Hz
Jitter	Input signal time variation @ zero-crossing (f_{in} = 10 GHz, P_{in} = –10 dBm)	1			ps
T_r or T_f	Output edge speed (10% to 90% rise/fall time)	70			ps

1. For sine-wave inpout signal. Prescaler will operate down to D.C. for square-wave input signal. Minimum divide frequency limited by input slew-rate.

2. Prescaler may exhibit this output signal under bias in the absence of an RF input signal. This condition may be eliminated by use of the pre-amp disable ($V_{Disable}$) feature, or the differential input de-biasing technique.

RF Specifications, continued

(T_A = 25 °C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/conditions	High output power operating mode[1] Typ.	Min.	Max.	Units
P_{out}	@ f_{out} < 1 GHz	0	–2.0		dBm
	@ f_{out} = 1.25 GHz	0	–2.0		dBm
	@ f_{out} = 1.5 GHz	–0.25	–2.25		dBm
$\lvert V_{out(p-p)} \rvert$	@ f_{out} < 1 GHz	0.5	0.39		Volts
	@ f_{out} = 1.25 GHz	0.5	0.39		Volts
	@ f_{out} = 1.5 GHz	0.48	0.38		Volts
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 10 GHz, unused RF_{out} or $\overline{RF}_{out}$ **unterminated**)	–61			dBm
	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 10 GHz, both RF_{out} and $\overline{RF}_{out}$ **terminated**)	–81			dBm
$P_{feedthru}$	Power-level of f_{in} appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 12 GHz, P_{in} = 0 dBm, referred to $P_{in}(f_{in})$)	–30			dBc
H_2	Second harmonic distortion output level (@ f_{out} = 1.5 GHz, referred to $P_{out}(f_{out})$)	–30			dBc

Symbol	Parameters/conditions	Low output power operating mode[2] Typ.	Min.	Max.	Units
P_{out}	@ f_{out} < 1 GHz	–6.0	–8.0		dBm
	@ f_{out} = 1.25 GHz	–6.0	–8.0		dBm
	@ f_{out} = 1.5 GHz	–6.25	–8.25		dBm
$\lvert V_{out(p-p)} \rvert$	@ f_{out} < 1 GHz,	0.25	0.20		Volts
	@ f_{out} = 1.25 GHz	0.25	0.20		Volts
	@ f_{out} = 1.5 GHz	0.24	0.19		Volts
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 10 GHz, unused RF_{out} or $\overline{RF}_{out}$ **unterminated**)	–71			dBm
	f_{out} power level appearing at RF_{in} or $\overline{RF}_{in}$ (@ f_{in} = 10 GHz, both RF_{out} and $\overline{RF}_{out}$ **terminated**)	–91			dBm
$P_{feedthru}$	Power-level of f_{in} appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 12 GHz, P_{in} = 0 dBm, referred to $P_{in}(f_{in})$)	–30			dBc
H_2	Second harmonic distortion output level (@ f_{out} = 1.5 GHz, referred to $P_{out}(f_{out})$)	–35			dBc

1. *$V_{PwrSel} = V_{EE}$*
2. *V_{PwrSel} = open circuit*

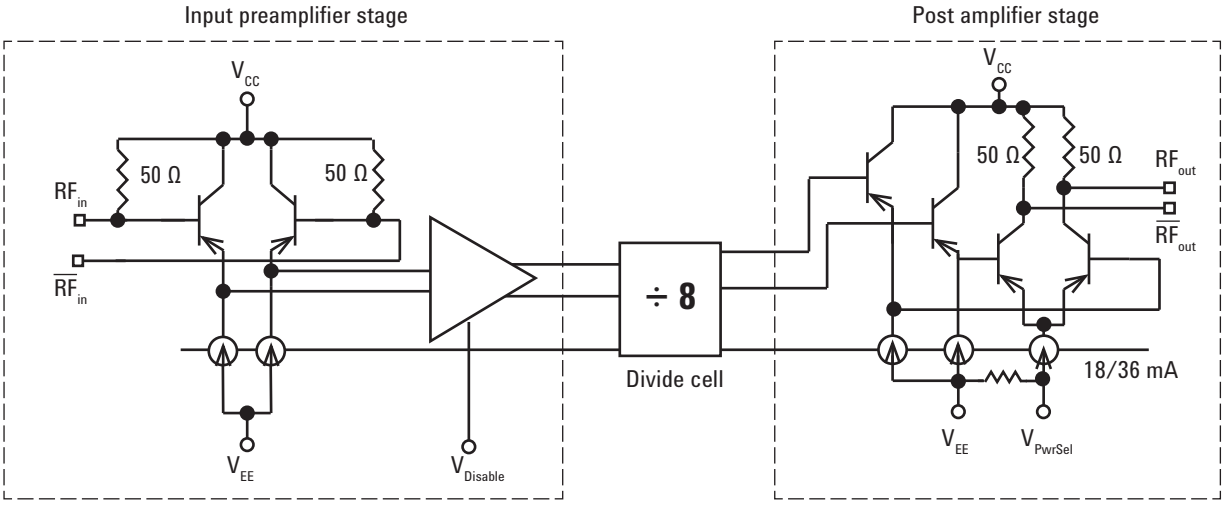


Figure 1. Simplified schematic

Applications

The HMMC-3028 is designed for use in high frequency communications, microwave instrumentation, and EW radar systems where low phase-noise PLL control circuitry or broadband frequency translation is required.

Operation

The device is designed to operate when driven with either a single-ended or differential sinusoidal input signal over a 200 MHz to 12 GHz bandwidth. Below 200 MHz the prescaler input is "slew-rate" limited, requiring fast rising and falling edge speeds to properly divide. The device will operate at frequencies down to DC when driven with a square-wave.

The device may be biased from either a single positive or single negative supply bias. The backside of the device is not DC connected to any DC bias point on the device.

For positive supply operation V_{CC} is nominally biased at any voltage in the +4.5 to +6.5 volt range with V_{EE} (or V_{EE} & V_{PwrSel}) grounded. For negative bias operation V_{CC} is typically grounded and a negative voltage between –4.5 to –6.5 volts is applied to V_{EE} (or V_{EE} & V_{PwrSel}).

Several features are designed into this prescaler:

1. Dual-output power feature

Bonding both V_{EE} and V_{PwrSel} pads to either ground (positive bias mode) or the negative supply (negative bias mode), will deliver ~0 dBm (0.5 V_{p-p}) at the RF output port while drawing ~40 mA supply current. Eliminating the V_{PwrSel} connection results in reduced output power and voltage swing, –6.0 dBm (0.25 V_{p-p}) but at a reduced current draw of ~30 mA resulting in less overall power dissipation. (Note: V_{EE} must ALWAYS be bonded and V_{PwrSel} must NEVER be biased to any potential other than V_{EE} or open-circuited.)

2. V_{Logic} ECL contact pad

Under normal conditions no connection or external bias is required to this pad and it is self-biased to the on-chip ECL logic threshold voltage (V_{CC} –1.35 V). The user can provide an external bias to this pad (1.5 to 1.2 volts less than V_{CC}) to force the prescaler to operate at a system generated logic threshold voltage.

3. Input disable feature

If an RF signal with sufficient signal-to-noise ratio is present at the RF input, the prescaler will operate and provide a divided output equal to the input frequency divided by the divide modulus. Under certain "ideal" conditions where the input is well matched at the right input frequency, the device may "self-oscillate," especially under small signal input powers or with only noise present at the input. This "self-oscillation" will produce a undesired output signal also known as a false trigger. By applying an external bias to the input disable contact pad (more positive than V_{CC} –1.35 V), the input preamplifier stage is locked into either logic "*high*" or logic "*low*" preventing frequency division and any self-oscillation frequency which may be present.

4. Input DC offset

Another method used to prevent false triggers or self-oscillation conditions is to apply a 20 to 100 mV DC offset voltage between the RF_{in} and $\overline{RF}_{in}$ ports. This prevents noise or spurious low level signals from triggering the divider.

Adding a 10 KΩ resistor between the unused RF input to a contact point at the V_{EE} potential will result in an offset of ≈25 mV between the RF inputs. Note however, that the input sensitivity will be reduced slightly due to the presence of this offset.

Assembly Techniques

Figure 3 shows the chip assembly diagram for single-ended I/O operation through 12 GHz for either positive or negative bias supply operation. In either case the supply contact to the chip must be capacitively bypassed to provide good input sensitivity and low input power feedthrough. Independent of the bias applied to the device, the backside of the chip should always be connected to both a good RF ground plane and a good thermal heat sinking region on the mounting surface.

All RF ports are DC connected on-chip to the V_{CC} contact through on-chip 50 Ω resistors. Under any bias conditions where V_{CC} is not DC grounded, the RF ports should be AC coupled via series capacitors mounted on the thin-film substrate at each RF port. Only under bias conditions where V_{CC} is DC grounded (as is typical for negative bias supply operation) may the RF ports be direct coupled to adjacent circuitry or in some cases, such as level shifting to subsequent stages. In the latter case the device backside may be "floated" and bias applied as the difference between V_{CC} and V_{EE}.

All bonds between the device and this bypass capacitor should be as short as possible to limit the inductance. For operation at frequencies below 1 GHz, a large value capacitor must be added to provide proper RF bypassing.

Due to on-chip 50 Ω matching resistors at all four RF ports, no external termination is required on any unused RF port. However, improved "Spitback" performance (~20 dB) and input sensitivity can be achieved by terminating the unused RF_{out} port to V_{CC} through 50 Ω (positive supply) or to ground via a 50 Ω termination (negative supply operation).

GaAs MMICs are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly.

MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

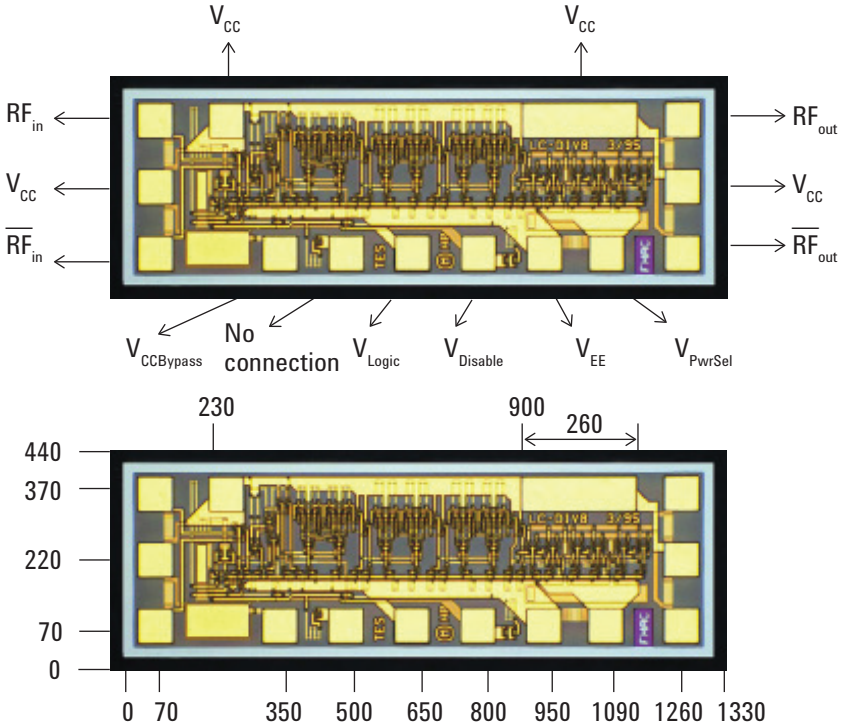
GaAs MMIC ESD, Die Attach and Bonding Guidelines, Application Note (5991-3484EN) provides basic information on these subjects.

Optional DC operating values/logic levels

(T_A = 25 °C)

Function	Symbol	Conditions	Min. (volts/mA)	Typical (volts/mA)	Max. (volts/mA)
Logic threshold[1]	V_{Logic}		V_{CC} –1.5	V_{CC} –1.35	V_{CC} –1.2
Input disable	$V_{Disable(High)}$ [Disable]		V_{Logic} +0.25	V_{Logic}	V_{CC}
Input disable	$V_{Disable(Low)}$ [Enable]		V_{EE}	V_{Logic}	V_{Logic} –0.25
Input disable	$I_{Disable}$	$V_D > V_{EE}$ +3	($V_{Disable}$ –V_{EE} –3)/500	($V_{Disable}$ –V_{EE} –3)/500	($V_{Disable}$–V_{EE} –3)/500
Input disable	$I_{Disable}$	$V_D < V_{EE}$ +3	0	0	0

1. Acceptable voltage range when applied from external source.

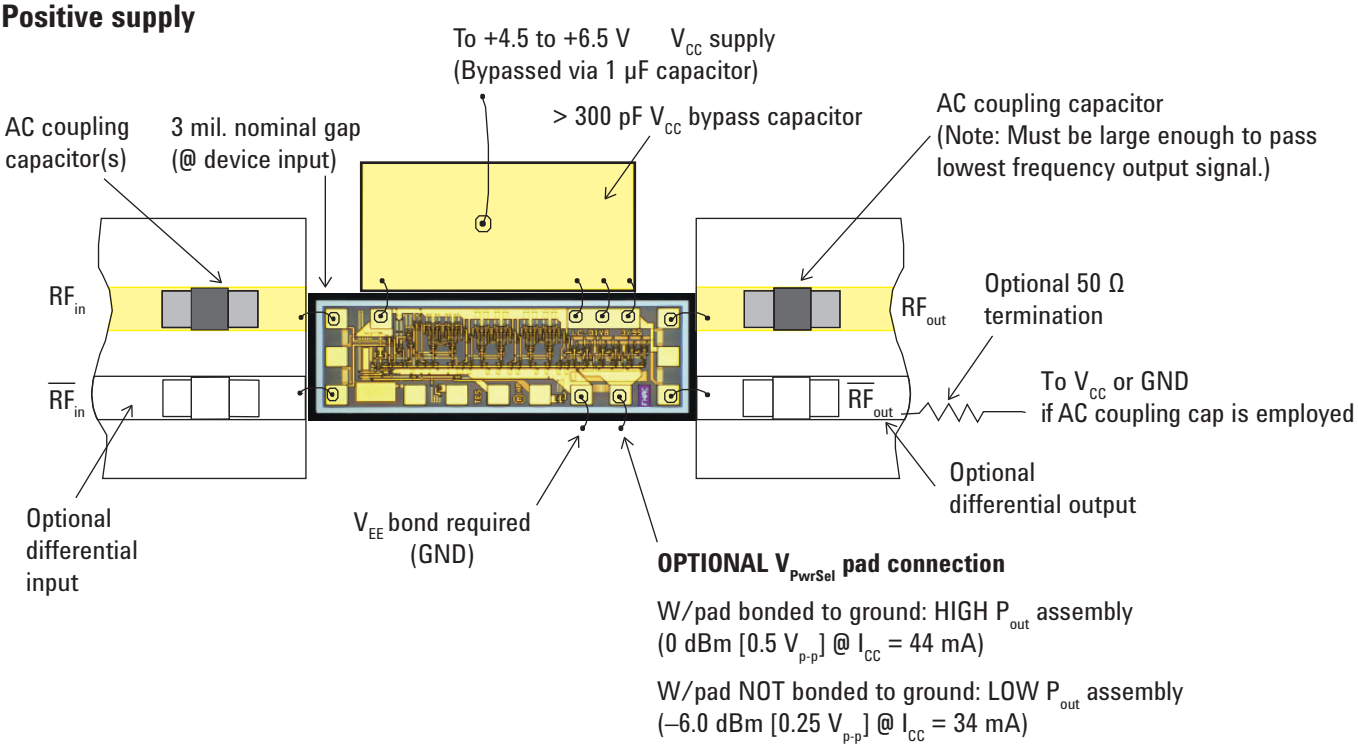


Notes:

- *All dimensions in microns.*
- *All pad dim: 70 x 70 mm (except where noted).*
- *Tolerances: ± 10 mm*
- *Chip thickness: 127 ± 15 mm*

Figure 2. Pad locations and chip dimensions

Positive supply



Negative supply

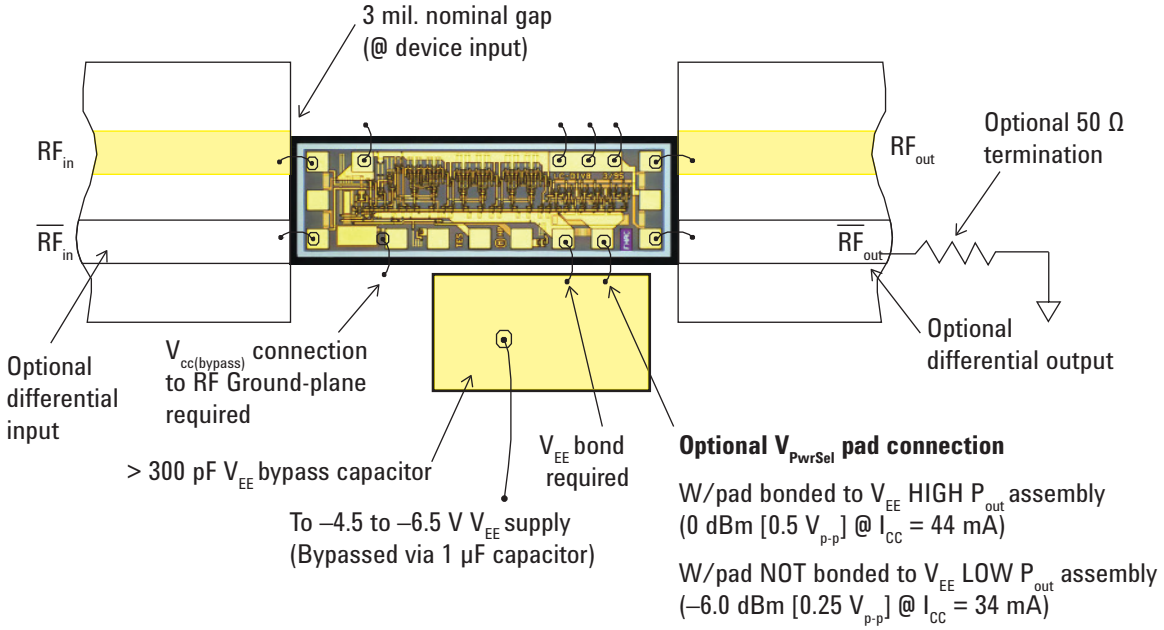


Figure 3. Assembly diagrams

Supplemental Data

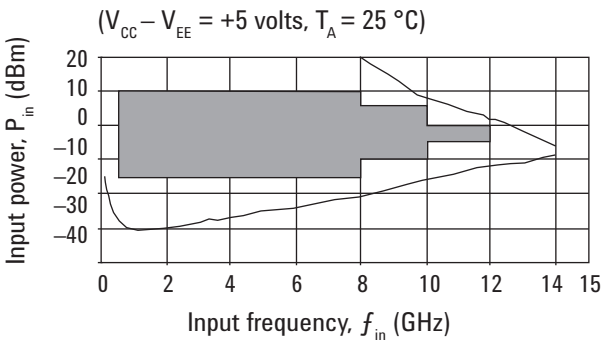


Figure 4. Typical input sensitivity window

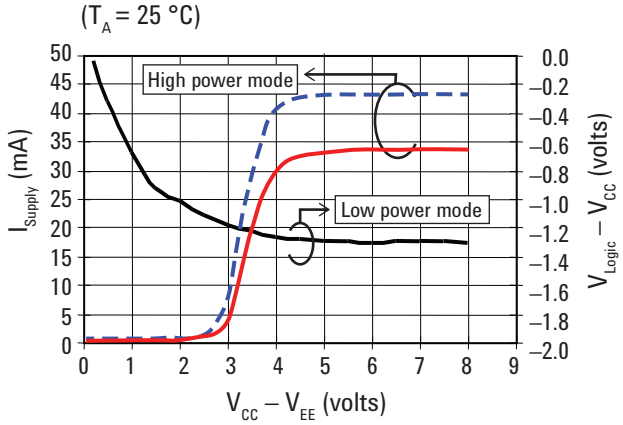


Figure 5. Typical supply current & V_{Logic} vs. supply voltage

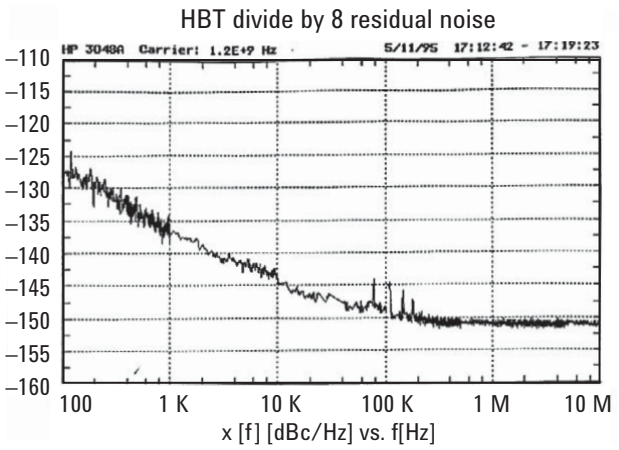


Figure 6. Typical phase noise performance

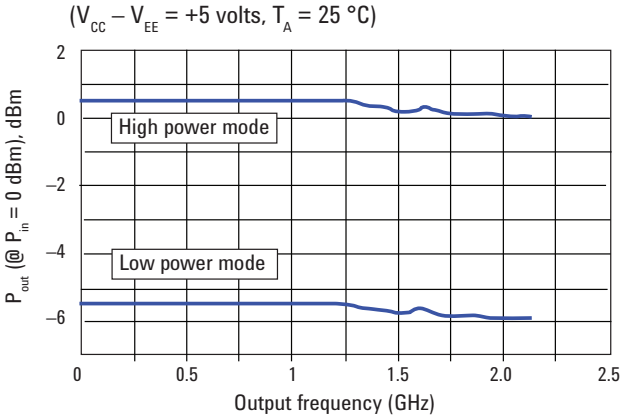


Figure 7. Typical output power vs. output frequency, f_{out} (GHz)

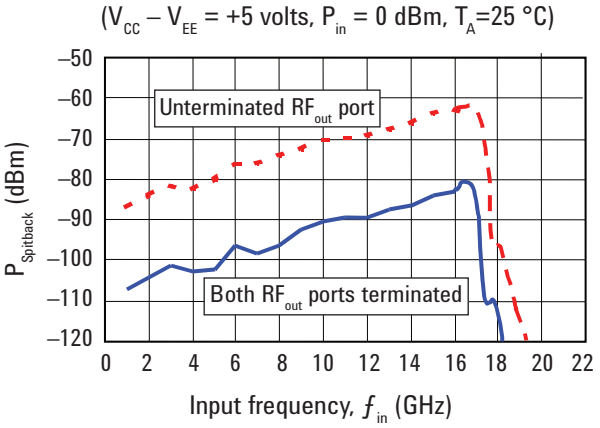


Figure 8. Typical "spitback" power P (f_{out}) appearing at RF input port

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