Agilent

Inphi Corporation Delivers Memory Interface Chip for DDR3-1600 Using Advanced Design System

Customer Success Story

Customer:

Inphi Corporation designs chips that deliver high performance and excellent signal integrity for processing high-speed data in demanding communication and computing systems.

Challenge:

Achieve 1.6G bps/pin with a single-ended connection across low cost RDIMM connectors and over FR4 board.

Solution:

Agilent's ADS Signal Integrity Designer tools fully explore the design and deliver robust signal integrity.

Results:

Accurate simulations save rework and chip spins, saving millions of dollars in lost revenue and in added design and photomask costs.

The accuracy of Advanced Design System saved Inphi re-spins when designing this DDR3 memory interface chip.

"*We have used many different simulation tools and find that ADS has unique advantages. It is the only tool we have employed simultaneously for device modeling to more than 100 GHz, multi-chip designs for telecom ICs, and system analysis for computer memory modules.*
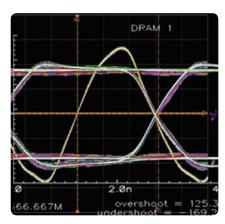
Its library of components is extensive and vetted by years of experience in the MMIC world – but unlike special-ized RF/microwave tools, ADS allows us to simulate mixed-signal ICs in time and frequency domains and trust the results at any data rate.

We have had many experiences where a traditional "SPICE" tool was used in the distributed-circuit arena and produced nonphysical results – ones that raise more questions than the simulation was intended to solve – and we turned to ADS to resolve the issue."

Ramanan Thiagarajah
Product Line Manager, Inphi Corporation

Inphi
Think fast.

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Simulation vs. measurement at register.

We asked Ramanan Thiagarajah, a product line manager at Inphi Corporation, about using Agilent EEsof EDA's Advanced Design System (ADS) Signal Integrity Designer tools to design their Registering Clock Driver for DDR3 RDIMMs.

Your Company:
What types of products do you develop? For what applications?

Inphi is a leading provider of memory interface chips. I'm product line manager for the Memory Interface Logic product line. The chip itself contains a PLL, decode logic and buffer logic running at 1.6 Gbps/pin in a 176 BGA package. Our products are used inside a DDR3-1600 RDIMM by our direct customers, the DRAM manufacturers. Our chip acts as an interface between the host controller, typically a microprocessor from Intel or AMD, and the DRAM chips inside the module. In turn, the modules are used inside high-end servers for the Internet and other data communications and data processing systems.

How do you work with other companies up and down the supply chain?

We work closely with the JEDEC consortium to define the RDIMM topology standards and layout, but there is always some variation between each vendor's implementation of what we call the raw cards that we have to accommodate. We get models of the host controller from the vendor, but, to protect their IP, these models are usually not very detailed, so we have to elaborate the model ourselves. On the DRAM side we have very detailed models. The channel between our chips and host controller crosses the raw card, the connector, and the motherboard. The channel design is controlled by the server manufacturer and it varies from system to system. We use S-parameter models to model a wide range of channel configurations.

Your Challenges:
What technical and business challenges do you face now and in the near future?

As memory speed and density increases, and you want to increase the number of slots per channel, signal integrity is the biggest technical challenge. We have to meet system performance — usually measured by the eye diagram opening — even under the tight constraint of low cost components and material. We're still using the low cost connectors from the DDR1 days, when frequencies were much lower. We don't have the luxury of exotic board materials like Duroid or Rogers. We can only use FR4, a higher-end FR4 maybe, but still basically FR4. So, the channel is impaired with HF attenuation, impedance variation, reflections, and ISI. Terminations are critical. We don't have the luxury of differential signaling either: DDR3 is single-ended. In these densely packed circuits, crosstalk is a big issue. Speeds are increasing from 1.6 Gbps/pin in DDR3 to 1.86, and 2.13 gigs in DDR3+ and 3.2 Gbps/pin in DDR4.

Our broad business challenges are time to market and the need to meet design and unit cost targets.

Your Solution:
How do you use ADS to solve these challenges?

We have used ADS for five or six years on several generations of products. The tool helps us evaluate and analyze various channel scenarios and allows us to identify and modify critical design parameters. We just completed one recently on stub resistances. We can explore the design space see the effect on the link-level metrics, such as the eye opening relative to the mask on the eye diagram. It gives us insight into which parameter is most critical and shows what range of values is suitable for the best eye opening. We get increased accuracy by measuring our current high-speed driver and feeding the S-parameters back into the tool to refine the model accuracy for the next generation.

Having the two links gives great flexibility because engineers who work mainly in Cadence Virtuoso can access the Agilent simulator, and those who work mainly in ADS can access the Cadence netlist via Dynamic Link.
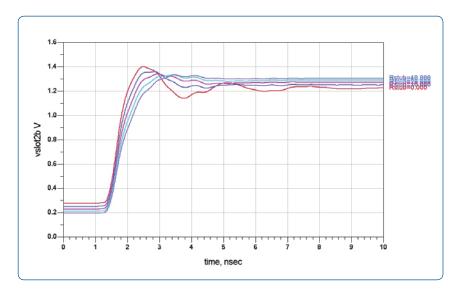
How does the Advanced Design System help you, and how does it compare to other tools you've used?

We have used many different simulation tools and find that ADS has unique advantages. It is the only tool we have used simultaneously for device modeling to more than 100 GHz, multi-chip designs for telecom ICs, and system analysis for computer memory modules.
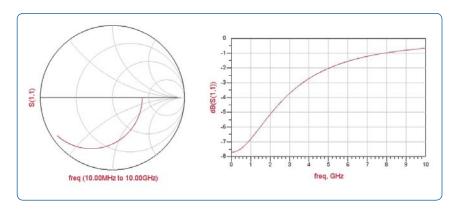
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Your Results:
Can you share any measurable benefits compared to alternate solutions?

We selected ADS because its accuracy saves us re-spins. For example, we're shipping the existing DDR2 family in high volume — millions of units per month of product — so you can see why any delay due to re-spins is very costly. The cost of a re-spin can be hundreds of thousands of dollars, but the opportunity cost of the delay — five to six weeks or more — is even more painful in terms of lost revenue—millions of dollars.

Effect of R_{stub} value during a write event.

Impedance/R_L looking into the controller from the motherboard.

Products Used

- E8988L ADS High Speed Analog Designer Premier
- W1112L GoldenGate Design & Verify
- E8970 RFIC Dynamic Link to Cadence

Web Resources

For more information about designing for signal integrity with Agilent EEsof EDA and Advanced Design System, visit our Website:
www.agilent.com/find/signal-integrity

For more information about other Agilent test and measurement products for signal integrity, go to:
www.agilent.com/find/si

For more information about InPhi, visit:
www.inphi-corp.com

To request an evaluation of Agilent's Signal Integrity solutions, visit:
www.agilent.com/find/eesof-si-demo-software-request

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