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Overview on 1.6-mW LC-tuned VCO Design for 2.4GHz in 0.18-um RF CMOS Technology

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Design of a 1.6-mW LC-tuned VCO for 2.4GHz applications in 0.18-um RF CMOS technology

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Abstract

A 2.4GHz fully integrated voltage-controlled oscillator has been designed in a 0.18-um RF CMOS process. Using only 1.2mA of current from a 1.3V power supply, the circuit shows a measured single-sideband phase noise of -117dBc/Hz at 1.0MHz offset frequency. The VCO can produce a GFSK-modulated output by adding a pair of small varactors in parallel to the resonance tank. The design of this VCO using the Agilent ADS harmonic balance and Momentum simulators will be described. The simulation results showing very good agreement with measurements will also be discussed.

1. Introduction

As CMOS process scaling goes further, CMOS realizations of transceiver front-ends become more and more attractive compared to bipolar solutions, also when considering power consumption. As market forces now drive total current consumption for wireless transceivers below 10mA, strict power constraints are imposed on all modules, including the VCO. It is therefore the task of the designer to design the most power-efficient VCO while fulfilling the phase-noise specification.

Several VCOs for 2.4GHz and above have already been presented ([4]-[9]), but for many of these designs the most important goal has been to minimize phase noise rather than minimizing power consumption.

This paper describes the design of a very low-power monolithic VCO intended for use in a 2.4GHz GFSK transmitter employing open-loop PLL direct VCO modulation. Other practical aspects of the design will be emphasized rather than deep theoretical treatments of phase noise, which has been covered in detail for this kind of oscillators in [1] and [2].

2. Specification

As this VCO is intended for use in an open-loop PLL modulation scheme (see Fig. 1), several requirements may be more strict compared to closed-loop operation. This is especially true for phase noise, as the noise is no longer shaped by the PLL when the loop is opened. In addition, meeting the modulation index stability requirements may present a challenge.

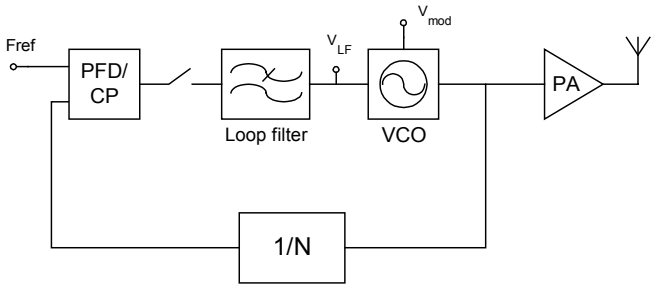


Figure 1 Simplified PLL modulator diagram showing reference frequency and modulating signal inputs

Phase Noise

For the application at hand, simulations show that adjacent channel transmitted power is not the limiting factor when it comes to phase noise. It is thus the modulated wave's signal-to-noise ratio (SNR) that sets the specification for oscillator phase noise. When modulating the VCO, the instantaneous output frequency will be the superposition of the modulation and the oscillator's internal noise signal, and the resulting average signal-to-noise ratio becomes

$$SNR \approx \frac{(\Delta f)^2/2}{\int_{f_1}^{f_2} f_m^{\,2} L(f_m)\,df_m}, \qquad (1)$$

assuming an IF equivalent noise bandwidth $B=2{\cdot}f_2$ in an imaginary noise free receiver. The choice of the lower integration bound f_1 is dependent on packet length in the transmission protocol. It is here assumed that noise at periods exceeding ten times the packet length do not contribute to the SNR. For the specification at hand [3], the maximum packet length is five slots, or 3.125 ms so f_1=32Hz.

It is worth mentioning that since CMOS oscillators exhibit substantial flicker noise, and since (in this case) the PLL is open during modulation, flicker noise will have quite a large

effect on total SNR, while it has only a marginal effect on the transmitted spectrum. To illustrate this point, Eq. 1 can be rearranged to plot SNR level curves in the f_{flk}-L(1MHz) plane, where f_{flk} is the value of the frequency offset f_m for which the up-converted flicker noise equals the up-converted white noise. It can be seen from the figure that if, for instance, a flicker noise knee of f_{flk}=100kHz is achievable and the desired SNR is 30dB, the "white" phase noise at 1.0MHz will have to be around -115.5dBc/Hz, while -112.5dBc/Hz would be sufficient if no flicker noise was present. Still, for a relaxed specification such as Bluetooth we realize that one can tolerate quite high noise levels without sacrificing system performance. This, in turn, motivates an oscillator design where low phase noise is traded for low power.

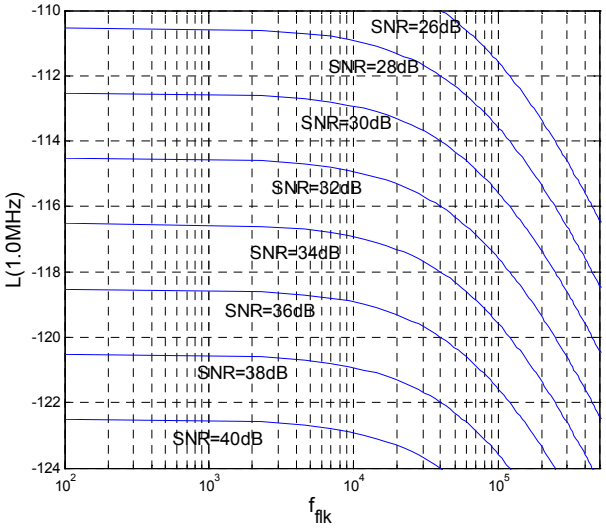


Figure 2 Curves of constant SNR assuming a noise bandwidth B=2.0MHz anda peak deviation of Δf=150KHz

Frequency Deviation

The frequency deviation stability specification normally requires some sort of process compensation when the VCO is used for direct frequency modulation. This is a severe problem when modulation is performed by adding a voltage signal at the PLL loop filter node, as the large VCO tuning range is usually exploited for process compensating the center frequency of the VCO. This means that the VCO gain with respect to modulation (K_{MOD}) varies a lot over process, since the loop filter voltage may take on different values depending on other tank capacitance variations. In our case, however, the modulation is applied at another node with predefined, optimum bias conditions such that the nonlinear main varactor capacitance vs. voltage characteristic has no effect on deviation.

Now, deviation will still be somewhat dependent on the total capacitance in the tank. Assuming the inductance has little or no process variation, it can be shown that the deviation will only be dependent on channel number and the modulation varactor's capacitance variations itself. The inductor's parasitic capacitances will certainly vary a lot over process, but this will be compensated for by the tuning of the loop filter voltage until the correct channel frequency is reached. The dependence of deviation upon channel number, or equivalently, oscillation frequency is:

$$\begin{aligned}\Delta f &= \frac{1}{2\pi\sqrt{LC}} - \frac{1}{2\pi\sqrt{L(C+C_{\mathrm{mod}})}} \\ &= f_0\left[1 - \frac{1}{\sqrt{1+C_{\mathrm{mod}}/C}}\right] = f_0\left[1 - \frac{1}{\sqrt{1+C_{\mathrm{mod}}L(2\pi f_0)^2}}\right] \\ &\approx 2\pi^2 f_0^3 C_{\mathrm{mod}} L\end{aligned} \qquad (2)$$

where the necessary additional capacitance C_{mod} is needed to create a deviation of Δf from center frequency f_0. This known relationship can thus be compensated for by using a programmable gain at the VCO modulation input, leaving the modulation varactor itself as the only source for variation in frequency deviation.

3. Design

As both low flicker-noise up-conversion and low power consumption are crucial in the application at hand, the well-known topology of Fig. 3 is adopted.

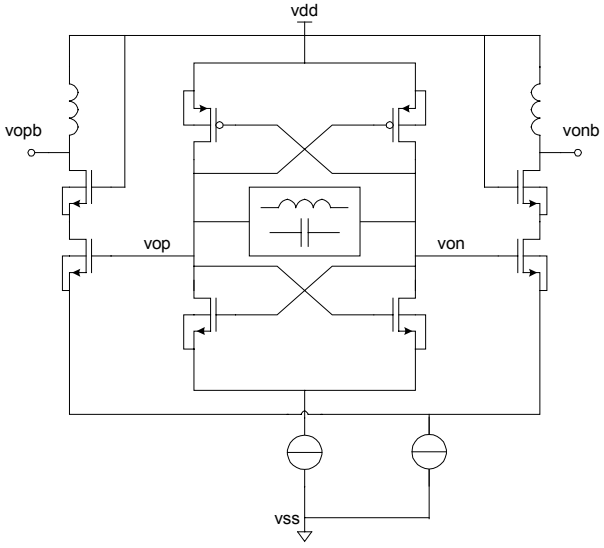


Figure 3 VCO core and output buffer

Resonance Tank

The resonance tank is shown in Fig. 4. It contains a 2.0nH planar, rectangular spiral inductor, a pair of MOS n-type varactors, a pair of plain MiM capacitors and two pairs (only one pair shown) of switched MiM capacitors to compensate for process variations. As the varactors have higher losses than MiM capacitors, the maximum size of the varactors is limited for phase noise reasons. This will, in turn, limit the VCO gain and therefore the maximum tuning range, but it will also reduce the oscillator's sensitivity to injected noise from other circuit components. At last, the tank also contains an extra set of very small varactors, suitable for analog FSK modulation. These should be so small that the noise from the pulse shaping filters do not affect carrier phase noise, but large enough so that their nonlinear C-V characteristic does not create intolerable spectral regrowth for the desired peak deviation.

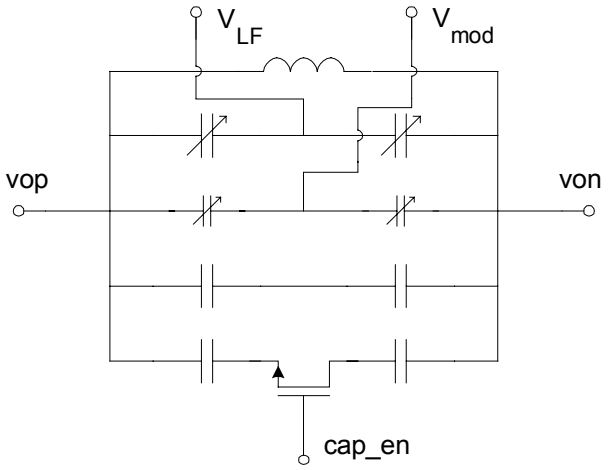


Figure 4 Resonance tank showing control (V_{LF}) and modulation (V_{mod}) inputs

Output buffer

As the oscillator frequency always will be subject to frequency pulling as power amplifier load impedance changes, it would be a good idea to use buffering with the maximum reverse isolation. As the oscillator is going to be capacitively loaded by a power amplifier, an inductively tuned differential cascode amplifier is used in this design. The simulated voltage gain is about 1dB using 0.4mA of current.

4. Experimental Results

The VCO was fabricated in a 6-metal-layer 0.18μm CMOS process with extra thick top metallization. A section of the chip micrograph is shown in Fig. 5. The oscillator core occupies less than 0.15mm^2 die area. The VCO output is sent through a -10dBm power amplifier before it goes off-chip for measurement.

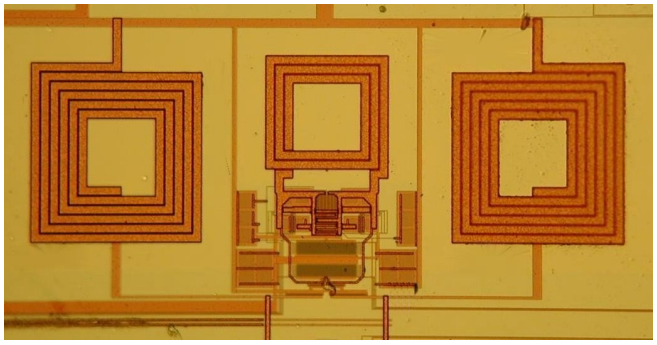


Figure 5 Section of die photo showing VCO (middle) and output buffer (bottom and sides)

Phase Noise

Phase noise was measured using the analog phase demodulation feature of an HP 89410 spectrum analyzer with RF extension. The measured spectrum can be seen in Fig. 6. Note that the instrument demodulates double-sideband, and that the single-sideband phase noise $L(f_m)$ may be obtained by subtracting 3dB from Fig. 6. The apparent flat part of the spectrum below 3kHz is due to the fact that the instrument operates with a resolution bandwidth of RBW=3kHz. This relatively high RBW means that the instrument is operating relatively close to its noise floor when measuring at 1.0MHz offset frequency. The measured flicker noise knee, f_{flk}, is about 150kHz for this design.

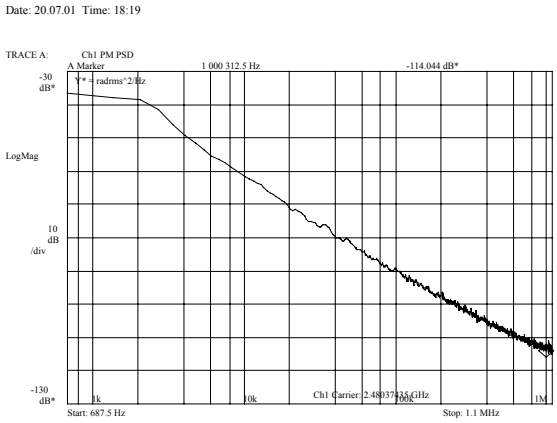


Figure 6 Measured Double-Sideband demodulated phase noise

If one is trying to quantify the "quality" of an oscillator, simply looking at the phase noise at one specific offset frequency is not enough. To be able to compare the oscillator phase noise to previously published designs, we

may use the PFN (*power-frequency-normalized*) figure of merit defined in [4],

$$PFN = 10\log\left[\frac{kT}{P_{\sup}}\left(\frac{f_0}{f_m}\right)^2\right] - L(f_m) \qquad (3)$$

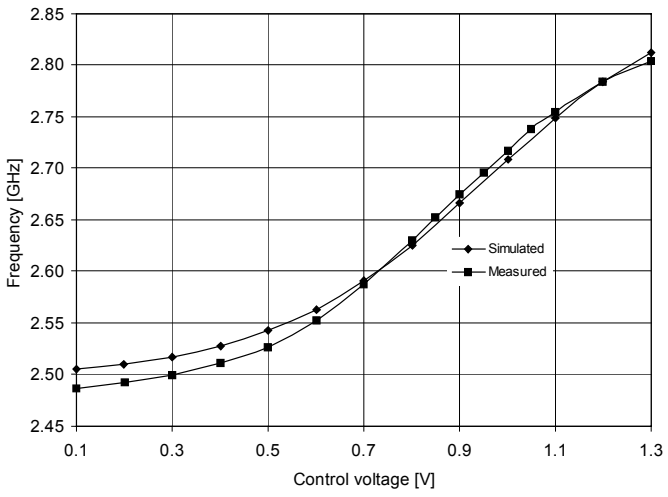
where $L(f_m)$ is expressed in dBc/Hz and a larger PFN corresponds to a better oscillator. This equation takes into account the physical phenomena that rule phase noise in oscillators, namely that phase noise is proportional both to the inverse of the dissipated power in the resonance tank and to the square of the f_0/f_m ratio. PFN for some previously published designs are shown in Table I. All designs are single-stage oscillators in CMOS technology except for [5], which is a quadrature LC-ring type of oscillator.

Table 1 Summary of CMOS oscillator properties

Ref	P_{sup} [mW]	f_0 [GHz]	f_m [MHz]	$L\{f_m\}$	PFN
Tiebout [5]	20.0	1.80	3.0	-143.0	11.7
This Work	1.56	2.48	1.0	-117.0	9.0
Hajimiri [1]	6.0	1.80	0.6	-121.0	8.8
De Ranter [6]	10.5	17.4	1.0	-108.0	8.6
Wang [7]	13.0	50.0	1.0	-99.0	7.8
Hegazi [8]	9.1	2.20	15.0	-148.0	7.3
Ham [4]	10.0	1.91	0.6	-121.0	7.1
De Muer [9]	34.2	2.00	0.6	-125.1	6.2

Tuning Range

The oscillator's tuning characteristic is shown in Fig.~5b. The frequency offset compared to the desired frequency range of 2.40-2.48GHz is due to poor accuracy of the inductor model at the time of design. Later simulations



using a field solver for the inductor show a 1.1 % accuracy for oscillator center frequency. The maximum gain occurs around 0.9V and is equal to K_{VCO}=440 MHz/V.

Figure 7 Measured and simulated tuning characteristic

Modulation Response

A digital synthesizer was used to create a Gaussian-filtered, random data signal with a bit rate of 1Mbit/s and BT=0.5. The $0.4V_{pp}$ voltage waveform was applied to the modulation input of the VCO, and the output spectrum and eye diagram can be examined in Fig. 8. The output spectrum is measured using max hold and RBW=100kHz.

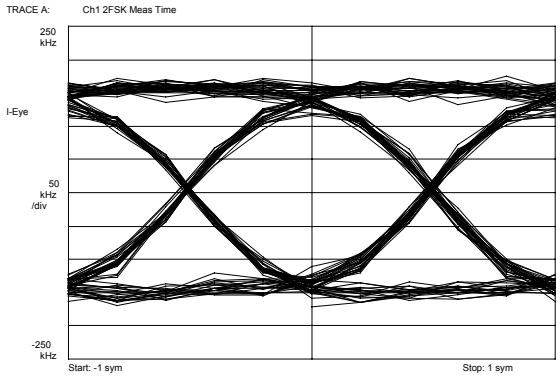


Figure 8 Measured modulation performance of the VCO: Eye diagram

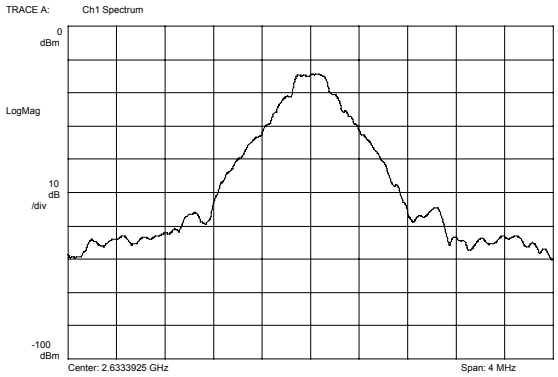


Figure 9 Measured modulation performance of the VCO: Output power spectrum

5. Conclusion

A 2.5GHz voltage-controlled oscillator has been designed in a 0.18-µm RF CMOS process. Using only 1.2mA of current from a 1.3V power supply, the circuit shows a measured single-sideband phase noise of -117dBc/Hz at 1.0MHz offset frequency.

When phase noise is normalized to power and frequency, the VCO shows excellent performance compared to other

recently reported designs. The VCO is also prepared for open-loop PLL GFSK modulation by adding an extra pair of small MOS varactors in parallel to the resonance tank. It is argued that this approach eliminates most of the process variation in frequency deviation. The modulation characteristics show excellent performance and Bluetooth compatibility.

Acknowledgements

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