

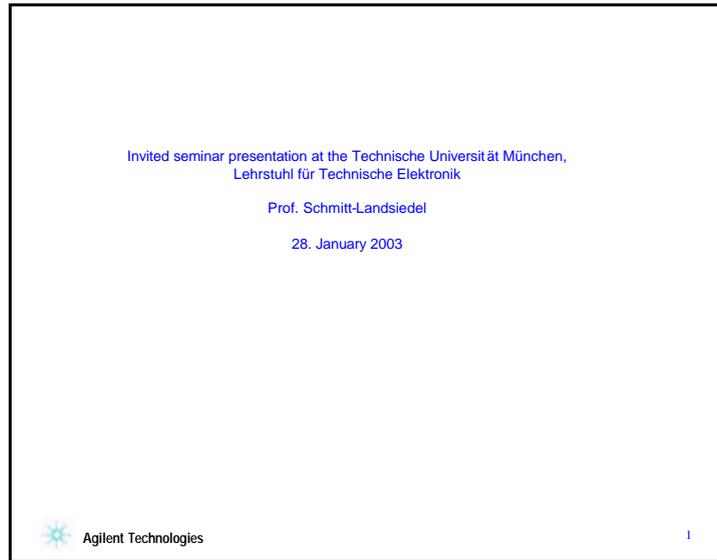


## Agilent EEsof EDA

### Presentation on DC and AC Characterization of Semiconductors

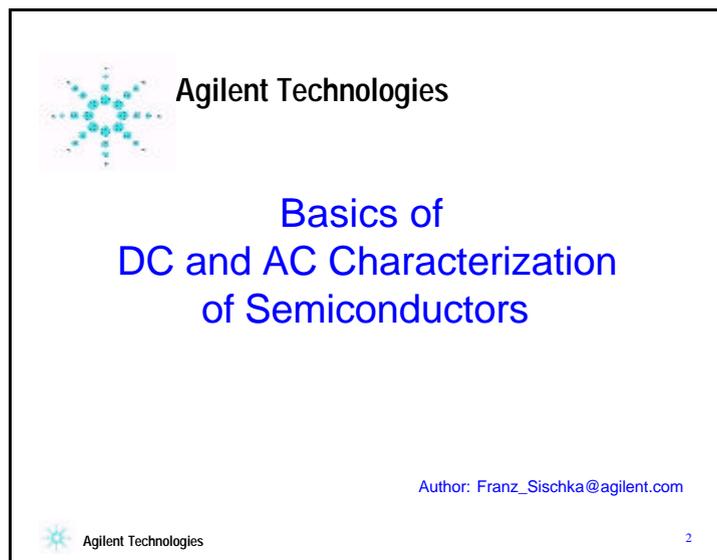
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Note: in the handouts, please find the notes *below* the corresponding slides.

Slide 2



The trend to higher integration and higher transmission speed challenges modeling engineers to develop accurate device models up to the Gigahertz range. An absolute prerequisite for achieving this goal are reliable measurements, which have to be checked for data consistency and plausibility.

This is especially true for radio-frequency (RF, >100MHz) and microwave (GHz) measurements, and also for checking and verifying the applied de-embedding techniques. If there are (hidden) problems with the measurement data, RF characterizations can become quite time consuming, with a lot of guesswork and ad-hoc judgments, and, basically, frustrating and not correct.

If, however, the underlying measurements are flawless and consistent, and provided the applied the models are understood well, RF characterization and device modeling becomes very effective and provides accurate design kits which will satisfy the chip designer's main goal: right the first time.

[Basics of DC and AC Characterization of Semiconductors](#)

Contents

- Basics of device measurement and modeling techniques from DC to RF
- Special aspects of network analyzer calibration
- De-embedding and required dummy structures

While the characterization of electronic components in the DC domain is relatively simple and only requires a Voltmeter and an Ampèremeter, the frequency performance of the device is affected by magnitude dependence and phase shift of the currents and voltages.

Furthermore, nonlinearities will lead to a spectrum of frequencies, although the device is only stimulated with a single, sinusoidal frequency.

Last not least, inevitable capacitive and inductive parasitics, with values close to those of the very device under test (DUT), will contribute to the measurements and degrade the measured performance of the 'inner' DUT.

In this presentation, we will go step by step through the individual characterization issues and develop measurement strategies which will provide the base of accurate device characterizations.

## Slide 4

[Basics of DC and AC Characterization of Semiconductors](#)

Contents

- Basics of device measurement and modeling techniques from DC to RF
- Special aspects of network analyzer calibration
- De-embedding and required dummy structures

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Let's begin with the basics of measurement techniques and device modeling from DC to RF.

## Slide 5





E5270A 8 Slot modular mainframe.

Associated modules:

- E5280A = HPSMU Module (2 slot) 10 fA ... 1A, 2uV .. 200V
- E5281A = MPSMU Module (1 slot) 10fA ... 200mA, 2 uV ..100V

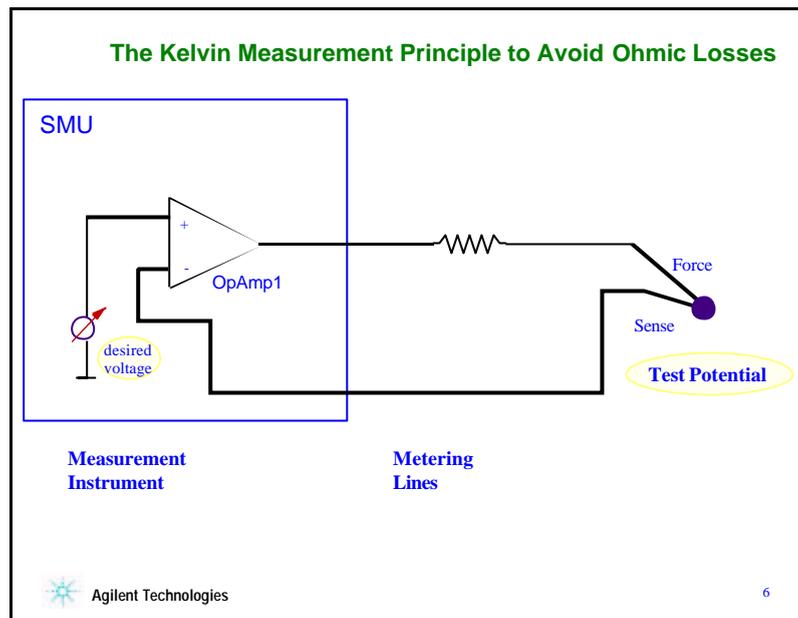
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Large signal modeling of a nonlinear component always begins with the characterization of its DC performance.

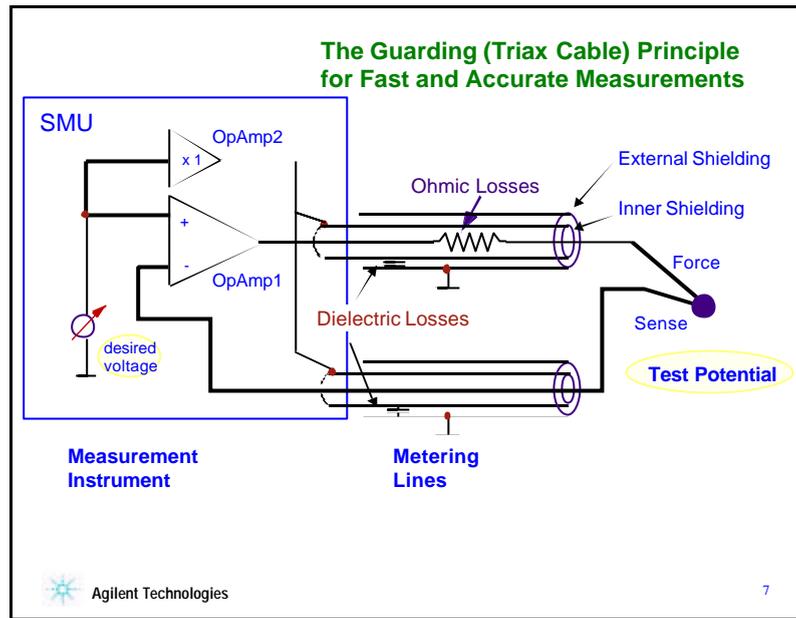
Instead of power supplies, precision DC parametric analyzers with source-monitor-unit (SMU) plugins are applied. They offer current ranges from fempto-Ampère ( $1E-15$ ) to several Ampères, and voltage potentials from micro-Volt to hundreds of Volts. This allows to fully characterize the DUT (device under test) in all four I-V quadrants. I.e. forward and reverse currents and voltages, are measured with the same SMU unit.

Usually, in case of a transistor, all 4 terminals (including substrate) are connected to individual SMUs in order to avoid recabling during the forward and reverse measurements.

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SMUs apply a Kelvin measurement to avoid parasitic series resistances. This measurement procedure, also known as the four-wire method, consists of a stimulating line (Force) with a second one in parallel (Sense) for every pin of the DUT. The slide above illustrates this. Ohmic losses on the Force line are eliminated by the operational amplifier (OpAmp1) in voltage follower mode. This means this OpAmp1 output will exhibit a somewhat higher voltage than the desired test voltage at the DUT, because the test current generates some ohmic losses along the Force line. The Sense line, connected to the minus input of the OpAmp1, assures that the DUT is biased with exactly the desired test voltage.



While the Kelvin method compensates the DC errors, it does not cover dynamic DC measurement problems. For example, to avoid external electro-magnetic influences, both the Force and Sense cables are shielded. But such cable shieldings exhibit parasitic capacitances. Due to charging problems, these capacitances will affect the measurement speed and accuracy of our Kelvin measurement.

As a simple example: assume we want to measure the reverse characteristics of a semiconductor diode. This means we need measure very low currents. Before the voltage steps to e.g. -20 V, the quiescent voltage at the diode is zero. That is, the cable capacitors are not charged. When the negative voltage step occurs, these capacitances have to be charged, and the required current is provided by the OpAmp1. This could lead to either a mis-measurement (DUT current plus charging current) or a delay in the triggering of the actual current measurement (by some intelligent firmware in our measurement).

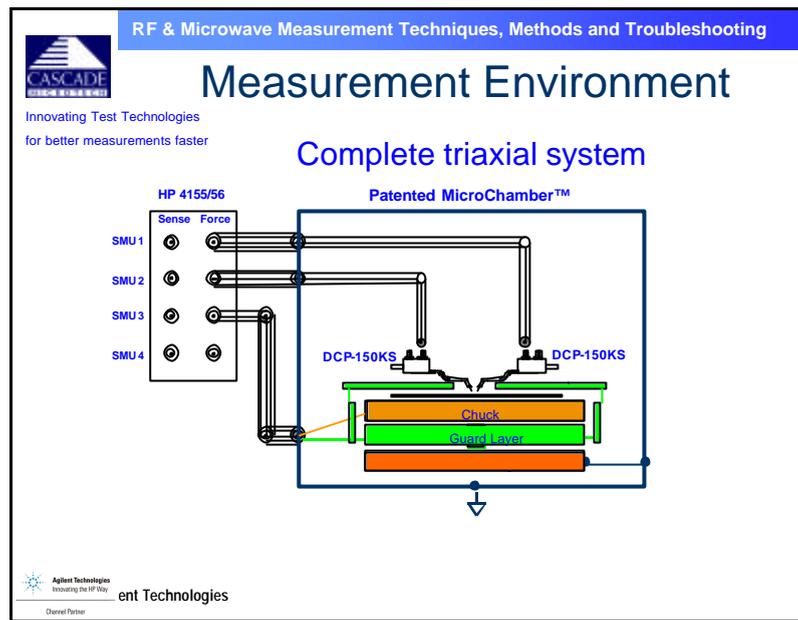
To solve this problem, an extra inner shielding is applied between the hot metering lines and the outer cable shielding, called 'Guard'. This extra shielding is connected to a separate, second OpAmp2 which follows exactly the value of the desired test voltage. Now it is this auxiliary OpAmp2 which supplies the charging current for the test cables, while the main OpAmp1 can start current measurements without being affected by this charging problem. That is, the inner measurement loop does not see the charging problem any more.

Of course the point where Force and Sense are tied together must be as close as possible to the DUT. In case they aren't connected, an internal 10kOhm resistor at the output of the SMU acts as the Kelvin point. Another important fact is that the Guard contact should *never* be connected to Force or Sense. Otherwise, the inner loop OpAmp1 of the SMU would measure the DUT current *plus* the charging current of the auxiliary, second OpAmp2!

Calibration:

In order to maintain the DC measurement accuracy, SMUs perform periodically an auto-calibration. This means that the SMU disconnects its outputs from the DUT, measures possible offset voltages and currents and corrects it. This type of calibration does not require any action from the user.

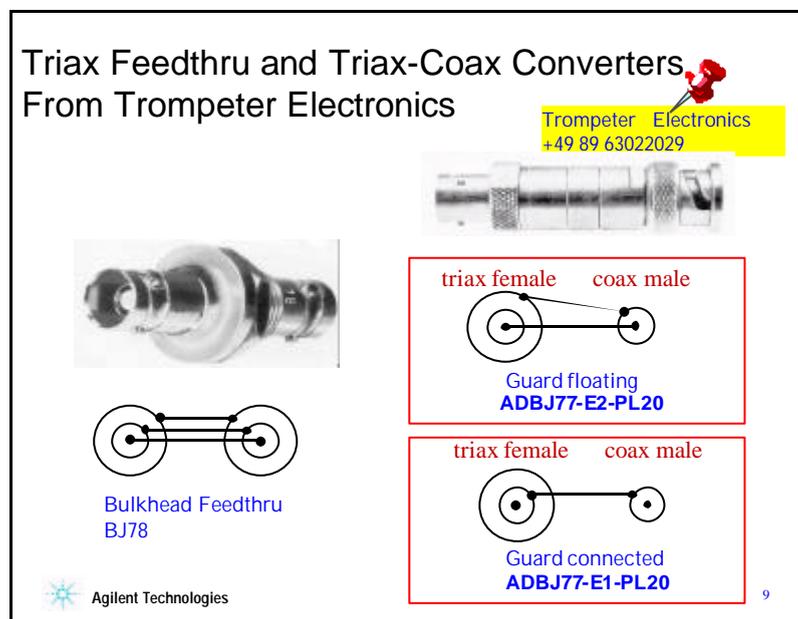
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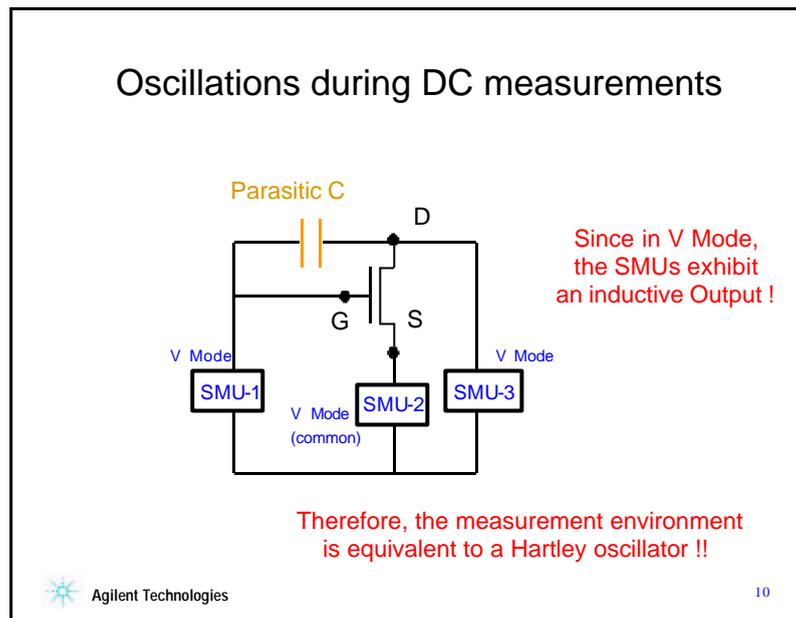
Typical on-wafer IV measurement setups require probes and chuck bias. A careful shielding completely surrounds the wafer with guard.

(slide with courtesy from Cascade Microtech)

Slide 9



When connecting the Triax connectors, and particularly when applying an adapter, make sure the Guard is left open and floating !



Under certain circumstances, SMUs may oscillate.

Superbeta, wide- bandwidth bipolar transistors are especially susceptible to oscillation. But also GaAs transistors.

Oscillation can become a problem when using older DC probe needles. A common way to avoid such oscillations is using HF probes (Ground-Signal-Ground GSG probes), or the newer shielded DC needles.

If you have to live with your DC needles, and when oscillations occur, here some ideas on causes for such oscillations:

#### 1) SMU Induced oscillations

These oscillations occur when an inductive load is connected to the SMU's output. The SMU has often an inductive load because the output impedance of the SMU is inductive during V-Mode operation and usually several SMUs are indirectly connected together through the DUT.

#### 2) Oscillation due to strays

The measurement system including the DUT, stray capacitance and residual inductance of the connection cables, switching matrix, probe card and/or test fixture can be recognized as an oscillation circuit.

The oscillation detector of SMU may not detect this type of oscillation. This is understandable when thinking of the SMU output as a low-pass filter, while the oscillation frequency may be in the 100MHz ... to several GHz range. Also, if –like in most cases- the oscillation is located at the DUT, the SMU itself cannot do anything to prevent this oscillations, since the cables are long compared to the oscillation wavelength.

As a general rule: the oscillation has to be avoided where it happens.

Related to the example of the slide above, we should be aware of the total circuit: The SMUs connected to the MOSFET's gate and drain are operating in the V-Mode. Since SMUs typically appear to be inductive in V-mode, this makes this configuration equivalent to a Hartley oscillator !

The SMU may oscillate if an unusually large inductance is connected to it. This could occur if the DUT is a superbeta transistor (big hFE) and the SMU connected to the emitter is set to one of the low current ranges.

For more details on conditions for oscillations, refer to the application note 356 -1 (publication number Agilent 5950-2954)

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### Methods to eliminate oscillations

- Ferrite beads placed as close as possible to the DUT to prevent high frequency oscillations ([Part Number 9170-0029](#))
- Keep cables as short as possible
  - Use High quality cable (low cable inductance)
- In some cases, more than 1 Ferrite Bead may be required!

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There are some effective methods to eliminate oscillations.

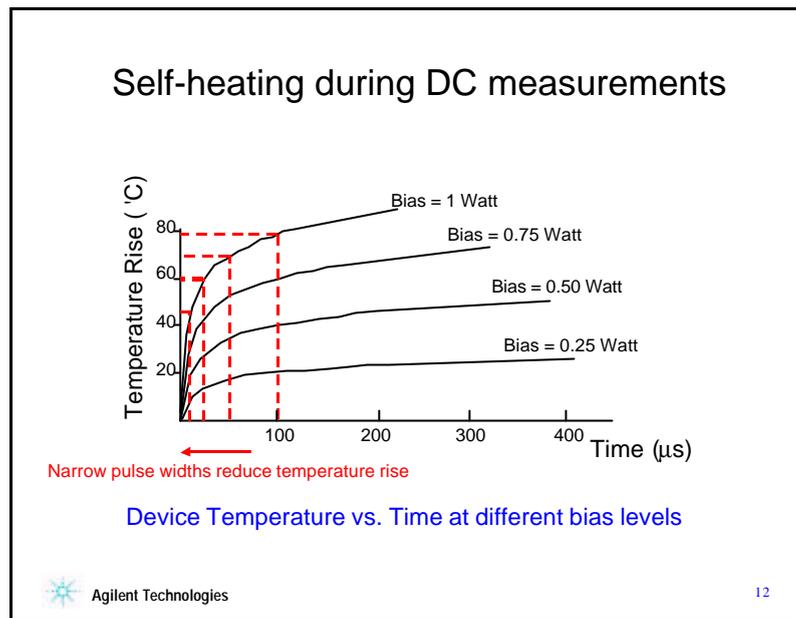
For FETs, add resistive ferrite beads as close as possible to the gate.

For bipolar transistors, add resistive ferrite beads as close as possible to the base or emitter.

Keep cables as short as possible. Long cables cause oscillation because of their large inductance.

In some cases, it is necessary to use more than one ferrite beads (Agilent Part Number 9170-0029).

>>> Or, apply shielded DC probes, even better apply RF probes.

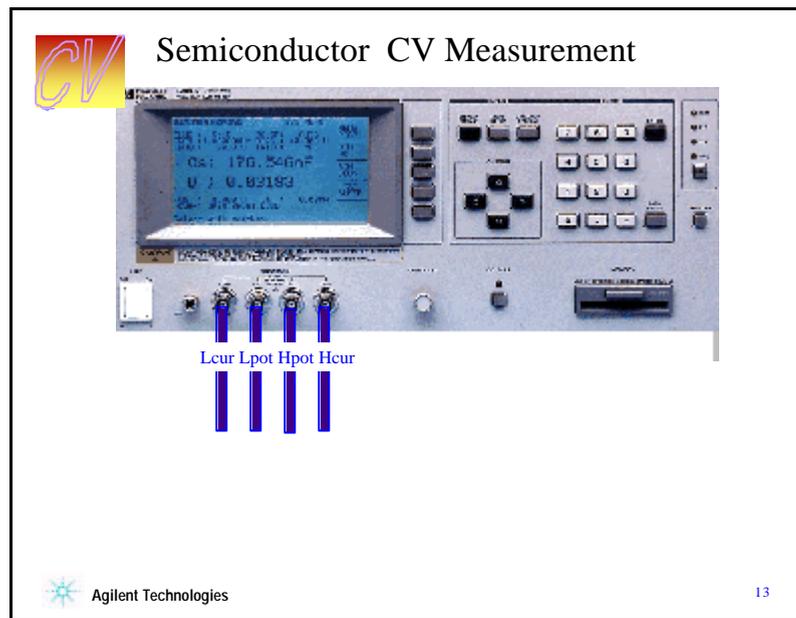


Self-heating can become a severe problem with device characterization, because the measurement results depends on the measurement speed!

This can be verified when e.g. measuring a Gummel plot for a bipolar transistor, once sweeping from low to high voltages different measurement speeds, and then sweeping from high to low voltages. Calculate beta out of your different measurements. If self-heating occurred, you will get as many beta curves as you have performed measurements!

The plot in the slide above gives the chip temperature increase of a packaged transistor as a function of the pulse width and the applied bias power. The pulse period is 1s. As can be seen, self-heating can only be avoided when applying very short, pulsed measurements, below 1 $\mu$ s pulse width. Such pulsed measurement systems, also included pulsed S-parameter measurements, are commercially available.

However, such systems are quite complex and expensive. Therefore, if you have to live with self-heating, make sure your device suffers always from the same self-heating. This means in general, apply the slowest measurement speed for you're your DC measurements, since your biased network measurements will be slow as well, and self-heating will definitively occur there !



As discussed in the previous chapter, the DC voltages and currents can be measured directly. The calibration is periodically auto-executed by the instrument.

After such a DC characterization, modeling engineers usually perform a so-called CV (capacitance versus voltage) measurement in order to characterize the device capacitances at a standard frequency of 1MHz. This frequency is high enough to allow a resolution down to a few fempto-Ampere (provided shielded probes are applied for e.g. on-wafer measurements), yet still low enough to neglect second order parasitics like resistors in series with the capacitors, or like inductances.

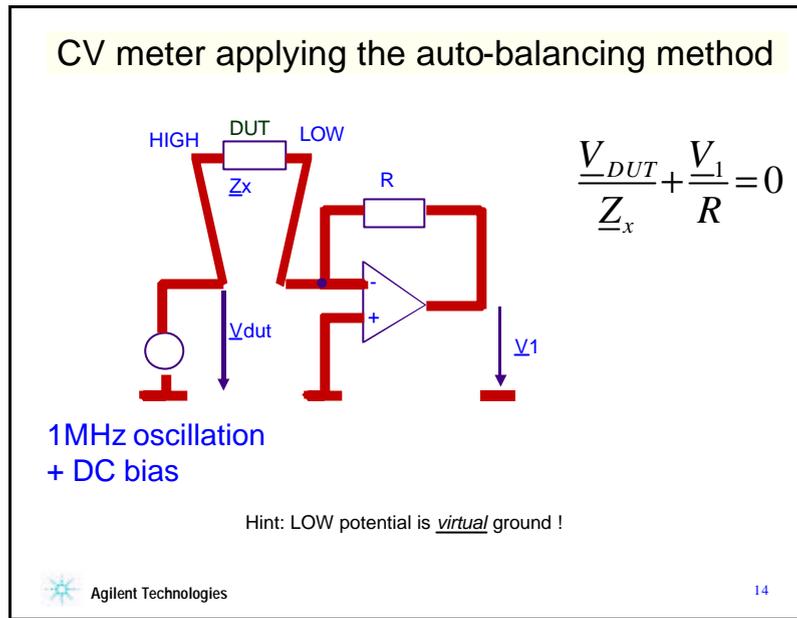
For such CV measurements, the DC-bias is swept, a test frequency (1MHz) is applied to the DUT, and the instrument calculates the capacitance between the 2 pins of the DUT from the magnitude and phase of the device voltage and current. This means, an impedance meter interprete the measurement result *always* with respect to a user-specified schematic: either a capacitor in series with a resistors, or both in parallel. This explains, why capacitances and resistor values may vary with frequency when measured with such a device. In other words, these frequency-variations are due to a too simplistic analysis model behind the measurement. A better way is therefore to measure the capacitances with network analyzers. In this case, it is up to the user to interpret the measurement result (S-parameters).

#### CV Measurements - Calibration considerations

Test cables and fixtures contribute and affect the device characterization. For CV measurements, the calibration consists of disconnecting the DUT, assuming an *ideal* OPEN condition and measuring the cables and their OPEN parasitics (CV-Meter calibration). After that, the corresponding capacitance is automatically subtracted from the DUT measurement by the CV meter.

Note: If we are interested in the inner DUT's CV curves, i.e. without its surrounding test pads capacitances, we need to connect to an OPEN dummy structure during CV meter calibration instead of simply leaving the cables unconnected. Such an OPEN dummy consists of all connection pads, lines to the DUT etc, but *without* the inner DUT itself.

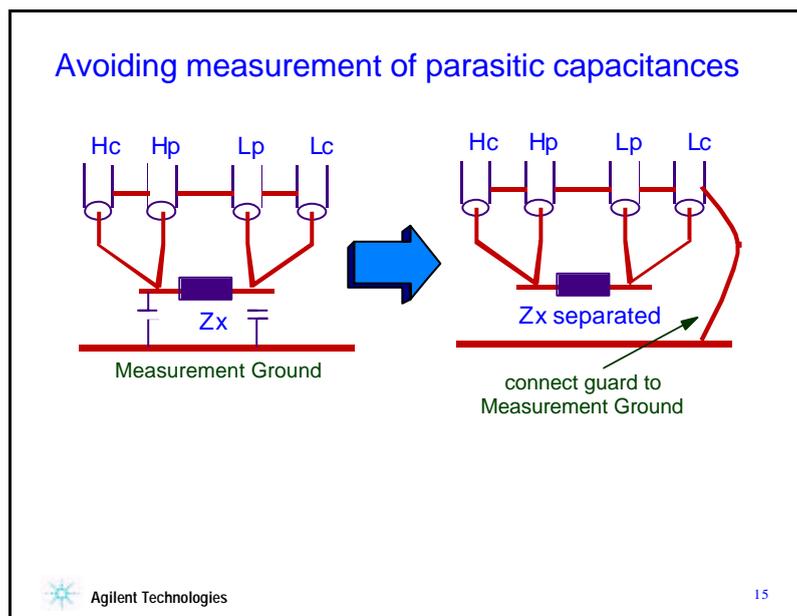
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For CV meters, the measurement principle is typically a so-called auto-balancing method. The slide above depicts the simplified measurement scheme.

The DUT is inserted in the feedback loop of an operational amplifier, and the system is stimulated with a 1MHz sinusoidal signal plus a DC bias. The feedback resistor R is precisely known, and the complex voltages V1 and Vdut are measured. From the formula given above in the slide, the capacitance of the DUT can be calculated, assuming an equivalent schematic of either a resistor in series with the capacitor, or, commonly for modeling, a capacitor in parallel with a resistor (which is the bias-dependent diode resistance for example).

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A so-called four-wire method is used for CV measurements. Similarly to the DC Kelvin measurement procedure (Force and Sense), both the low and high pin have to be tied together at the location of the DUT during CV measurements.

In the auto-balancing impedance measurement method, the shieldings of these four wires (which are not instrument chassis ground!) are connected to the virtual ground of the instrument's OpAmp. This eliminates any influences caused by the cables. Including this potential into the measurement setup allows the elimination of further stray capacitances. Like sketched above, it is possible to eliminate stray capacitances against ground (measurement plate).

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**Shielded Measurement of CGD**

With the auto-balancing method, connecting the Source to the cable shielding potential, isolates the effect of CGD, since both CGS and CDS are automatically excluded from the measurement result

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When characterizing the capacitances of transistors, the open 3rd transistor terminal should be connected to the shielding potential, eliminating the effect of the unwanted capacitors.

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**AttoGuard™ Enhanced CV Measurements**

- FemtoGuard surrounds the chuck at shield ground
- Patented AttoGuard above the chuck at shield ground
- Creates a virtual double-shielded Faraday enclosure
  - 10 atto Farad CV measurement resolution
  - Zero CV meter only one time

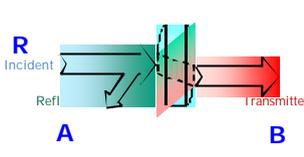
Cascade Microtech  
Innovating Test Technologies for better measurements faster

Agilent Technologies  
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The two shields insure equal potential everywhere inside the waferprober MicroChamber regardless of chuck locations.  
(slide with courtesy from Cascade Microtech)

## S-Parameters

### From Y-, Z-, and H-Parameters to S-Parameters




NOTE: on some older NWAs, you can see the 3 RF cables for the Reflected signal, signal A and signal B!

Like Y-, Z-, H-Parameters, S-Parameters belong to linear circuit theory. This means, matrix conversions etc. Are only applicable for linear operation of the device !


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While the CV measurement is considered as a specific two-pin test condition, the situation changes for frequencies above 100MHz. The device is now operated under its originally intended environment conditions: DC bias is applied to all the pins, and an additional small-signal RF excitation is applied. Now, the sinusoidal currents and voltages at *all* pins of the DUT are to be measured, *with magnitude and phase*.

A natural choice for such characterizations would be Z-, Y- or H-parameters from linear two-port theory. These two-port parameters can be used to completely describe the electrical behavior of our device (or network), including any source and load conditions. For such parameters, we have to measure the voltage or current as a function of frequency and bias at the ports of the device.

At high frequencies, however, it is very hard to measure voltage and current at the device ports. One cannot simply connect a voltmeter or current probe and get accurate measurements due to the impedance of the probes themselves. Additionally, there is a difficulty to place the probes at the desired positions. Furthermore we have to apply either (AC-wise) OPEN or SHORT circuits as part of the Z-, Y- or H-parameter measurement. Active devices may oscillate or self-destruct with such terminations.

To avoid these problems, twoports are described by S-parameters.

**IMPORTANT NOTE:**

like Y, Z, H parameters, S-Parameters are *linear* and belong to *linear circuit theory*. I.e. they represent the *small-signal behavior* of a device at a certain bias point, and for a certain frequency. Therefore, when measuring them, it must be assured that the *linear device operation* is maintained. As a consequence, linear S-parameters are independent of the applied RF signal power. Since twoport theory is restricted to linear circuit theory, matrix conversions (S to Y, S to Z etc. for de-embedding) are only applicable for linear operation of the device !

**Definition of S-parameters**  
 Referring to the spectacles examples from above, i.e. power-wise, the S-parameters are defined as:

$$\begin{pmatrix} |b_1|^2 \\ |b_2|^2 \end{pmatrix} = \begin{pmatrix} |S_{11}|^2 & |S_{12}|^2 \\ |S_{21}|^2 & |S_{22}|^2 \end{pmatrix} * \begin{pmatrix} |a_1|^2 \\ |a_2|^2 \end{pmatrix}$$

with

- $|a_i|^2$  power towards the two-port gate
- $|b_i|^2$  power away from the two-port gate

and

- $|S_{11}|^2$  power reflected from port1
- $|S_{12}|^2$  power transmitted from port1 to port2
- $|S_{21}|^2$  power transmitted from port2 to port1
- $|S_{22}|^2$  power reflected from port2

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**S-Parameters and Characteristic Impedance Z0**

Power Domain	$ a_1 ^2$		Voltage Domain	$a_1$
Starting with power	normalized to $Z_0$	gives normalized amplitudes for voltage and current		
$P = v * i$	$= \frac{v * v}{Z_0}$	$\longrightarrow$	$\sqrt{P} = \frac{V}{\sqrt{Z_0}}$	$= i * \sqrt{Z_0}$

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This means that S-parameters relate traveling waves (power) to a two-port's (DUT) reflection and transmission behavior. Since the two-port is imbedded in a characteristic impedance of  $Z_0$ , and since we apply linear circuit theory (!), these 'waves' can be interpreted in terms of normalized voltage or current amplitudes.

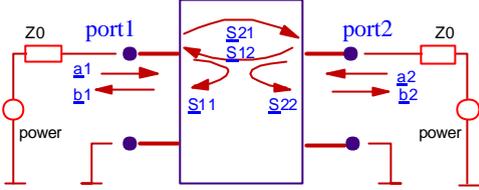
Note: think of the spectacles again: also here, the lens is imbedded on both sides with the same 'characteristic impedance', i.e. air !

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Because of the characteristic impedance, we can convert the power towards the two-port into a normalized voltage amplitude of

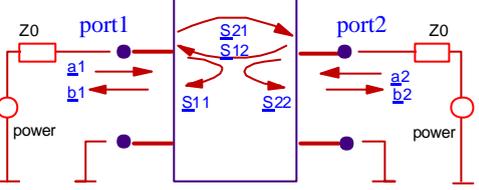
$$a_i = \frac{v_{\text{towards\_twoport}}}{\sqrt{Z_0}}$$

and the power away from the two-port can be interpreted in terms of voltages like

$$b_i = \frac{v_{\text{away\_from\_twoport}}}{\sqrt{Z_0}}$$


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Looking at the S-parameter coefficients individually, we have:

$$S_{11} = \frac{b_1}{a_1} = \frac{v_{\text{reflected at port 1}}}{v_{\text{towards port 1}}} \quad \left/ \quad \underline{a_2} = 0 \right.$$

$$S_{21} = \frac{b_2}{a_1} = \frac{v_{\text{out of port 2}}}{v_{\text{towards port 1}}} \quad \left/ \quad \underline{a_2} = 0 \right.$$

$$S_{12} = \frac{b_1}{a_2} = \frac{v_{\text{out of port 1}}}{v_{\text{towards port 2}}} \quad \left/ \quad \underline{a_1} = 0 \right.$$

$$S_{22} = \frac{b_2}{a_2} = \frac{v_{\text{reflected at port 2}}}{v_{\text{towards port 2}}} \quad \left/ \quad \underline{a_1} = 0 \right.$$

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S11 and S21 are determined by measuring the magnitude and phase of the incident, reflected and transmitted signals when the output is terminated with a perfect Z0 load. This condition guarantees that a2 is zero. S11 is equivalent to the input complex reflection coefficient or impedance of the DUT, and S21 is the forward complex transmission coefficient.

Likewise, by placing the source at port 2 and terminating port 1 in a perfect load (making a1 zero), S22 and S12 measurements can be made. S22 is equivalent to the output complex reflection coefficient or output impedance of the DUT, and S12 is the reverse complex transmission coefficient.

The accuracy of S-parameter measurements depends greatly on how good a termination we apply to the port not being stimulated. Anything other than a perfect load will result in a1 or a2 not being zero (which violates the definition for S-parameters).

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### Interpreting S-parameters

**S11 and S22**

value	interpretation
-1	all voltage amplitudes towards the twoport are inverted and reflected (0 Ω)
0	impedance matching, no reflections at all (50 Ω)
+1	voltage amplitudes are reflected (infinite Ω)

**S21 and S12**

magnitude	interpretation
0	no signal transmission at all
0 ... +1	input signal is damped in the Z0 environment
+1	unity gain signal transmission in the Z0 environment
> +1	input signal is amplified in the Z0 environment

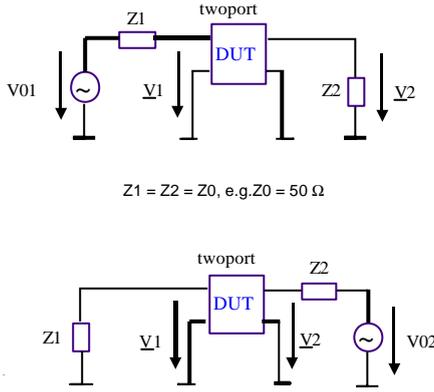

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The magnitude of S11 and S22 is always less than 1. Otherwise, it would represent a negative ohmic impedance value.

The magnitude of S21 (transfer characteristics) respectively S12 (reverse) can exceed the value of 1 in the case of active amplification. Furthermore, S21 and S12 can be positive and negative. If they are negative, there is a phase shift. Example: S21 of a transistor starts usually at about  $S_{21} = -2 \dots -20$ . This means signal amplification within the Z0 environment *and* 180° phase shift.

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### Calculating S-Parameters From Voltages



$$S_{11} = 2 * \frac{V_1}{V_{01}} - 1$$

$$S_{21} = 2 * \frac{V_2}{V_{01}}$$

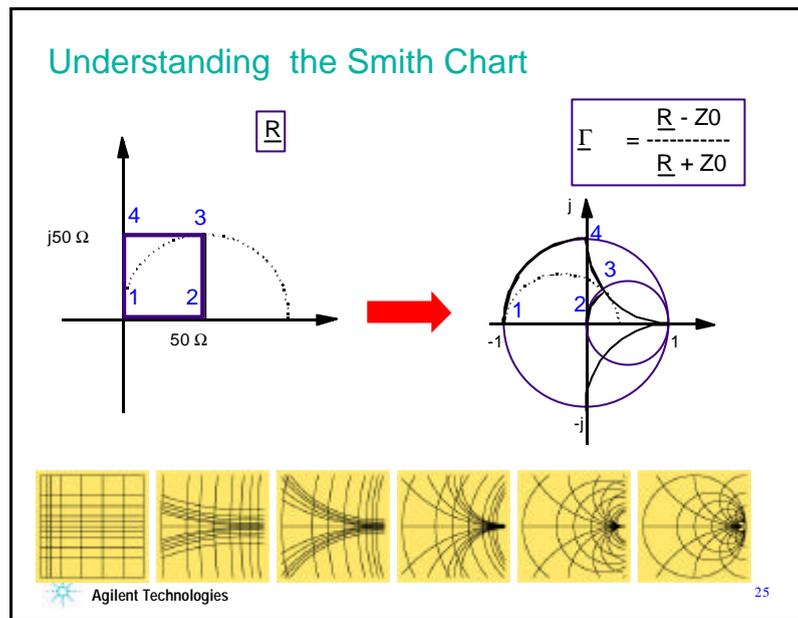
$$S_{12} = 2 * \frac{V_1}{V_{02}}$$

$$S_{22} = 2 * \frac{V_2}{V_{02}} - 1$$

Z1 = Z2 = Z0, e.g. Z0 = 50 Ω


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The slide above presents a method to calculate S-parameters from complex voltages. The DUT is imbedded in an characteristic impedance environment. Provided the required complex forward and reverse voltages  $V_1, V_{01}, V_2, V_{02}$  can be obtained (from measurements or simulations), we can calculate the S-parameters from the equations given above.



What makes  $S_{xx}$ -parameters especially interesting for modeling, is that  $S_{11}$  and  $S_{22}$  can be interpreted as complex input or output resistances of the two-port. That's why they are usually plotted in a Smith chart.

NOTE: do not forget that *included* in  $S_{xx}$  is the termination at the opposite side of the two-port, usually  $Z_0$  !!

The Smith chart is a transformation of the complex impedance plane  $\underline{R}$  into the complex reflection coefficient  $\underline{\Gamma}$  (rho), following the formula given above.

This means that the right half of the complex impedance plane  $\underline{R}$  is transformed into a circle in the  $\underline{\Gamma}$ -domain. The circle radius is '1'.

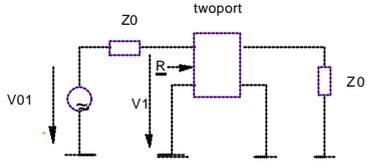
In order to get more familiar with interpreting the Smith chart, let's consider a square with the corners  $(0/0)\Omega$ ,  $(50/0)\Omega$ ,  $(50/j50)\Omega$  and  $(0/j50)\Omega$  in the complex impedance plane  $\underline{R}$  and its equivalent in the Smith chart with  $Z_0=50\Omega$ . Watch the angle-preserving property of this transform (rectangles stay rectangles close to their origins). Also watch how the positive and negative imaginary axis of the  $\underline{R}$  plane is transformed into the Smith chart domain ( $\underline{\Gamma}$ ), and where  $(50/j50)\Omega$  is located in the Smith chart. Also verify that the center of the Smith chart represents  $Z_0$ , i.e. for  $Z_0 = 50\Omega$ , the center of the Smith chart is  $(50/j0)\Omega$ .

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### WHY A SMITH CHART FOR THE Sxx-PARAMETERS ??

The voltage-related equation for the S11 parameter is  $S_{11} = 2 \cdot \frac{v_1}{v_{01}} - 1$  (1)

where  $v_1$  is the complex voltage at port 1 and  $v_{01}$  the stimulating AC source voltage (which is typically normalized to '1'). The corresponding circuit schematic is:



Under the assumption that  $R$  is the complex input resistance at port 1 and  $Z_0$  is the system impedance, we get applying the resistive divider formula for equation (1) from above:

$$S_{11} = 2 \cdot \frac{R}{R+Z_0} - 1 = \frac{R-Z_0}{R+Z_0}$$

And this is the reflection coefficient  $\Gamma$  from the Smith Chart definition !!

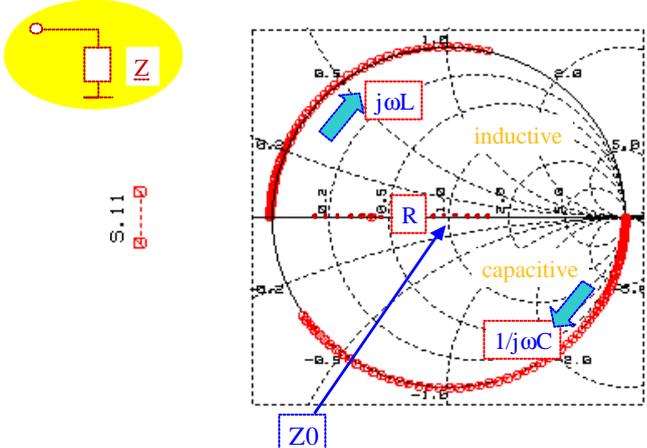
Or, solved for the complex impedance  $R$ :  $R = Z_0 \cdot \frac{1+\Gamma}{1-\Gamma} = Z_0 \cdot \frac{1+S_{11}}{1-S_{11}}$

This explains how we can get the complex input/output resistance of a two-port directly from S11 or S22, if we plot these S-parameters in a Smith chart.

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### Interpreting S11 and S22 (Sxx)



The diagram illustrates the relationship between a circuit and its representation on a Smith chart. On the left, a circuit with a voltage source and an impedance  $Z$  is shown. On the right, the Smith chart is plotted, showing the real axis (resistive), inductive region (above), and capacitive region (below). A point  $Z_0$  is marked on the real axis. The chart also shows the reflection coefficient  $S_{11}$  and the input impedance  $R$ .

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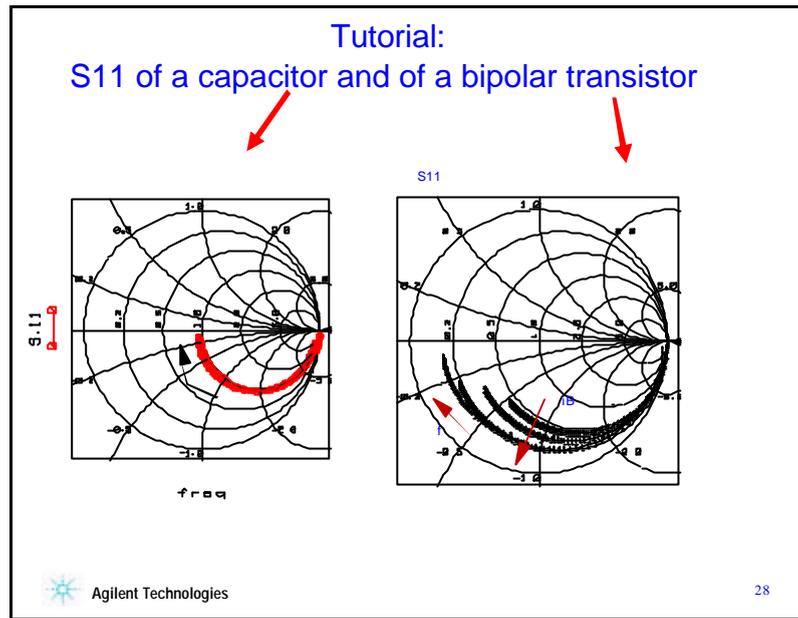
Rules for Smith charts for NWA measurements:

Sxx on the real axis represent ohmic resistors

Sxx above the real axis represent inductive impedances

Sxx below the real axis represent capacitive impedances

Sxx curves in the Smith chart turn clock-wise with increasing frequency (because in the  $R$  plane, all curves turn clock-wise too !).

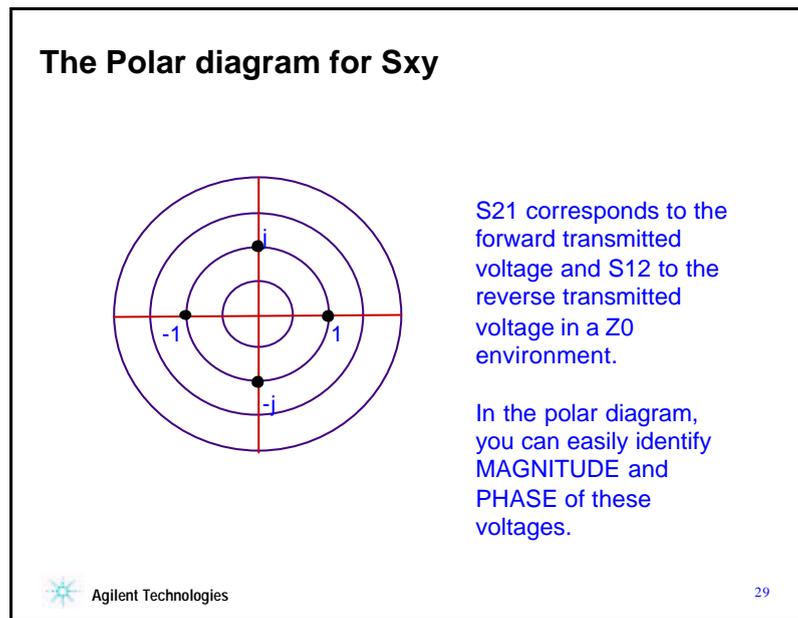


As an example for interpreting Smith charts, the left plot shows the S11 curve of a capacitor located between the two ports of the network analyzer (NWA). The capacitor represents an OPEN for DC, thus  $S_{11} = 1 = \infty * Z_0$ . For highest frequencies, it behaves like a SHORT, and we see the  $50 \Omega$  of the opposite port2 (!). The transition between the DC point and infinite frequency follows a circle, and the increasing frequency turns the curve again clockwise.

The right plot in the slide above shows the S11 plot of a bipolar transistor. In this case, the locus curve starts with  $S_{11} \approx 1$  at low frequencies corresponding to  $R_{BB'} + R_{diode} + (1+\beta) * R_E$ . For increasing frequencies, the curves then turn into the lower half-plane of the Smith chart, the capacitive region. Here, the CBE shorts  $R_{diode}$ , and  $\beta$  becomes smaller with frequency. For infinite frequency, when the capacitors represent ideal shorts, and  $\beta \rightarrow 0$ , the end point of S11 lies on the middle axis, i.e. the input impedance is completely ohmic, representing  $R_{BB'} + R_E$ . Since  $R_{BB'}$  is bias dependent, and decreasing with increasing  $i_B$ , the end points of the curves represent this bias-dependency.

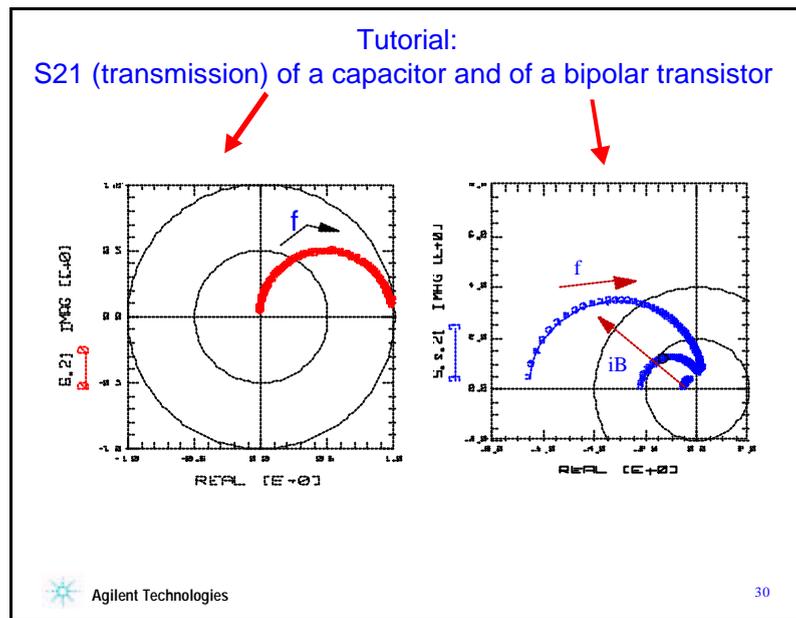
NOTE:

Keep in mind: For increasing frequency, the Sxx locus curves turn always clockwise!



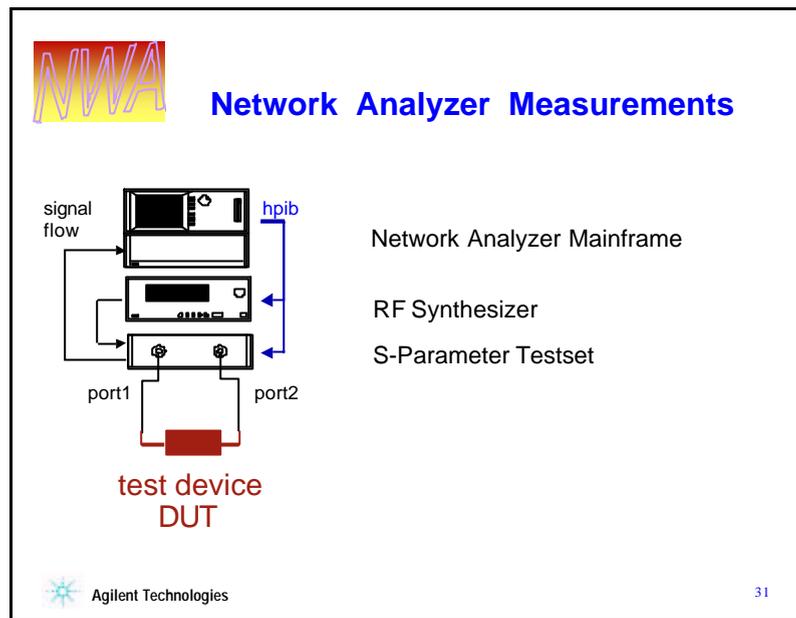
The S21 parameter represents the power transmission from port 1 to port 2, if the two-port device is inserted into a matching network with characteristic impedance  $Z_0$  of e.g.  $50 \Omega$ . This means, if no signal is transmitted, then  $S_{21}=0$  (located in the center of the polar plot). If the signal is transmitted, then  $MAG(S_{21})>0$ . The magnitude of the S21 curve will be below '1' for damping between the port 1 and port 2, and above '1' for amplification. If the phase is inverted (transistors !), we are basically in the left half-plane of the polar plot ( $REAL[S_{21}]<0$ ).

Like with the Smith chart, all S21 and S12 curves *turn clock-wise with increasing frequency*.



As a tutorial example, the capacitor on the left, exhibits no power transmission for lowest frequencies, but an ideal short ( $S_{21}=1$ ) for highest frequencies. Thus, the locus curve for  $S_{21}$  represents a circle from infinite to  $0 \Omega$ .

The right plot from above shows the  $S_{21}$  plot of a bipolar transistor between port 1 and port 2. The trace starts with  $\text{REAL}(S_{21}) < -1$  at low frequencies (voltage amplification in a  $50 \Omega$  system, plus phase inversion), and then tends towards  $S_{21} = 0$  for highest frequencies (no voltage transmission, the transistor capacitances short all voltage transmission). Since the current amplification  $\beta$  is bias depending, the start point of the  $S_{21}$  curve at lowest frequencies reflects this  $\beta(iB)$  dependency: more  $\beta$  for higher  $iB$ , i.e. more amplification magnitude with  $S_{21}$  for higher  $iB$  too.



After the introduction to the S-parameters, it is time to consider how to measure them. A network analyzer (NWA), also sometimes abbreviated by VNA (vector network analyzer), is applied. This instrument measures S-parameter vectors, i.e. the magnitude and phase, of all four S-parameters of a two-port. This 'full two-port measurement' capability is important, because only in this case are we able to convert the measured S-parameters to Y- and Z-parameters etc., what is a requirement for de-embedding etc.

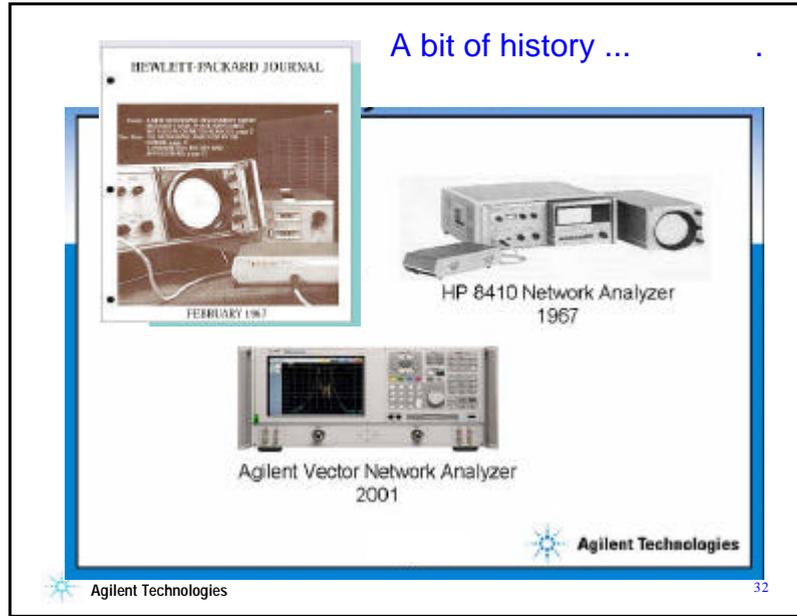
When applying network analyzers for S-parameter measurements, it is important to remember that we measure

- linear* circuit performance
- and circuit performance for a given frequency (fundamental frequency), ignoring harmonics.

On the other hand, network analyzers can also be applied to specific non-linear measurements, e.g. sweeping the RF power, measuring the transfer characteristics and evaluating for example the 1dB compression point of amplifiers. In this case, however, signal distortion happens and harmonic frequencies show up. In our case, when measuring linear S-parameters with the NWA, always the *base* or *fundamental* frequency and is measured, and harmonics should not occur. Otherwise, they would be ignored !!

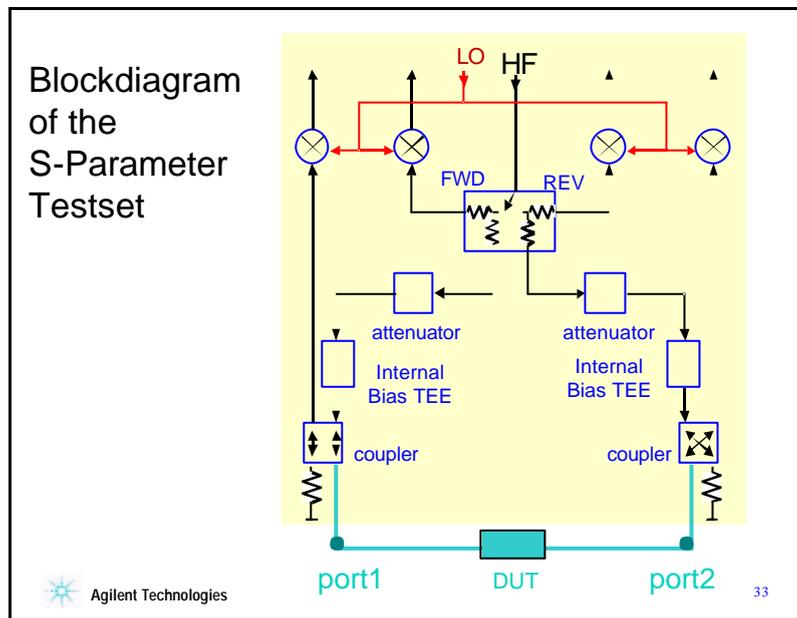
Therefore, if we are interested in the modeling of device nonlinearities, we should rather apply a spectrum analyzer after the conventional DC-CV-NWA modeling, and use harmonic balance simulation (e.g. Agilent's ADS) to model the RF-power dependent spectrum. Alternatively, one of the currently introduced commercial Nonlinear NWAs (Agilent N4463A Large Signal Network Analyzer) can be applied as well. Such instruments measure both, the magnitude and phase of the transmitted and reflected, fundamental and harmonics frequencies.

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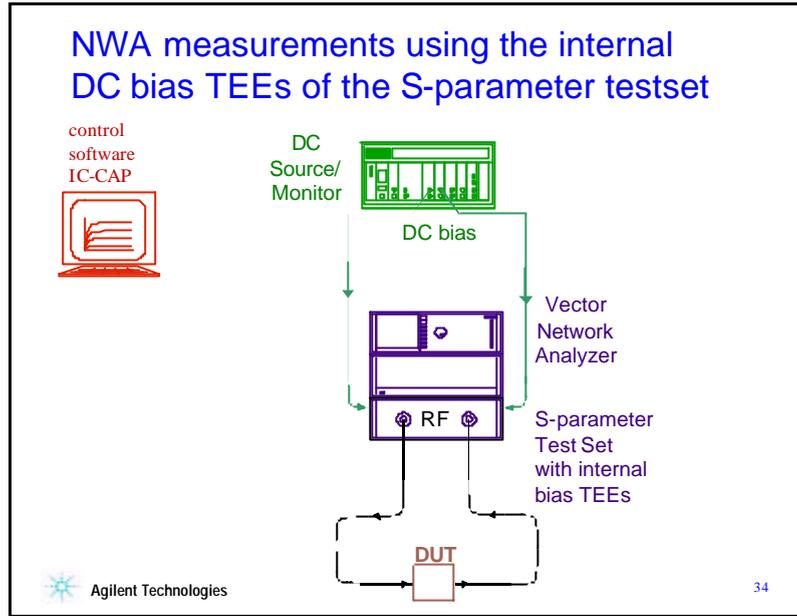
When Hewlett-Packard introduced the HP 8410 in 1967, it revolutionized microwave design. It used the a new 1430A sampler together with a superheterodyne receiver architecture to provide a calibrated microwave receiver. Together with the test sets, it featured measurements of the transmission and reflection coefficients for any twoport device.

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The block diagram in the slide above shows the core of this meter combination, the S-parameter testset. The RF Input source at the top, connected to the RF synthesizer, provides the stimulus power. The PIN switch directs the signal to either a forward or a reverse S-parameter measurement. Directional couplers then detect the injected and reflected power of the DUT. The detected signals are downconverted into four IF signals for further analysis in the VNA mainframe, where each input is digitized and signal processed in order to give the S-parameters.

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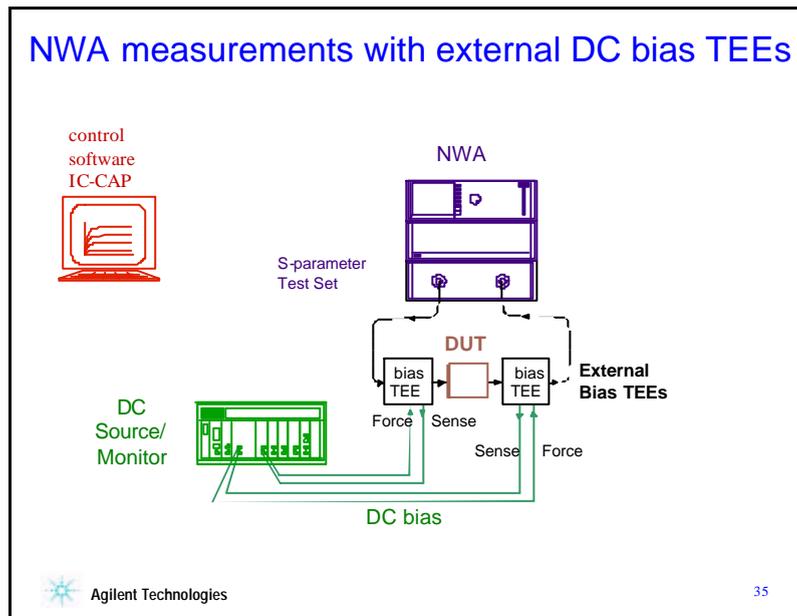


For devices like transistors and diodes, an additional DC bias has to be applied to the device. This can be done by using the DC bias inputs of the NWA's S-parameter testset. Keep in mind that there are typically  $1\text{-}2\Omega$  ohmic losses due to the internal bias TEE's inductor. This causes a voltage drop and a reduced bias voltage at the device! Many NWA's also have an internal  $1\text{M}\Omega$  resistor to ground, which prevents electrostatic discharge damage to the internal NWA circuitry.

NOTE:

In the setup presented above, make sure to use the right triax (SMU) to coax (S-parameter testset) adapter, which leaves the middle shield of the SMU triax cable (Guard) unconnected!

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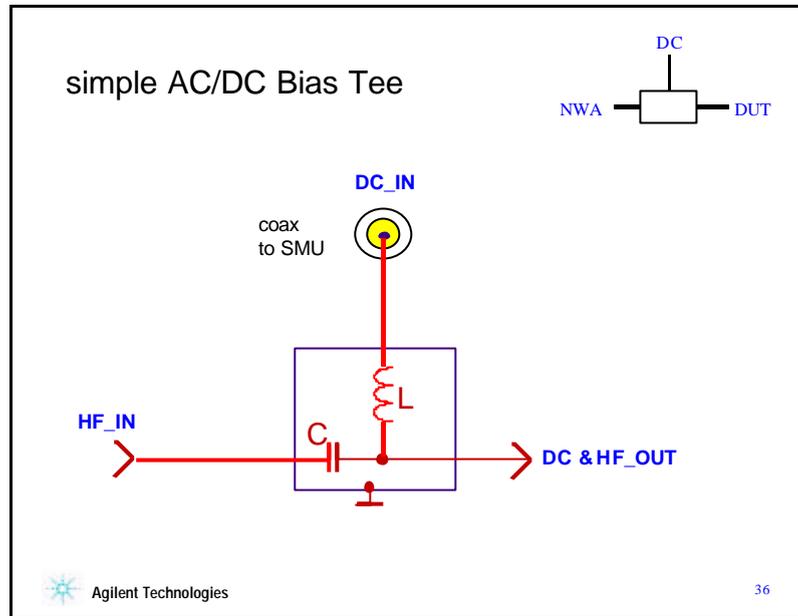


If we want to avoid the ohmic losses of the NWA's internal bias TEE, we can use external bias TEEs and apply the previously mentioned force-sense DC biasing (Kelvin measurements). However, the ohmic losses for the bias are now *not* zero, but rather  $\sim 1\Omega$ , due

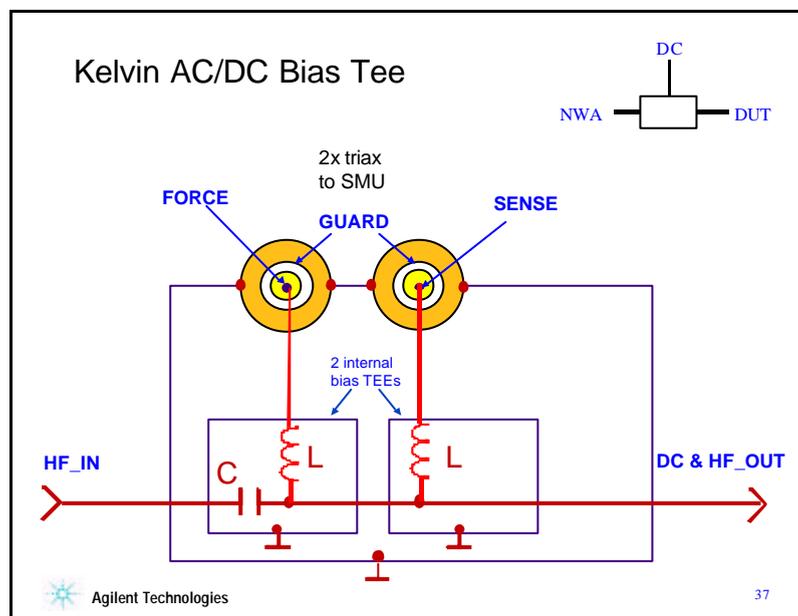
to losses in the cables and the connectors. Also, these Kelvin bias TEEs should be placed as close as possible to the DUT.

In the measurement setup above, two external bias TEEs are inserted between the two DUT connections and the network analyzer ports.  
Keep in mind to not connect the guard shield of the triax Kelvin cables.

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Slide 38

Basics of DC and AC Characterization of Semiconductors

Contents

- Basics of device measurement and modeling techniques from DC to RF
- Special aspects of network analyzer calibration
- De-embedding and required dummy structures

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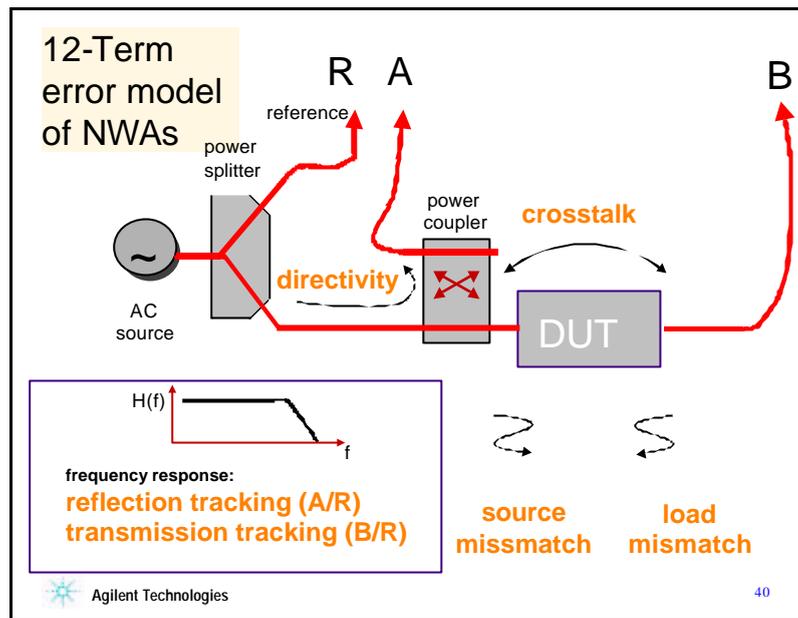
**Vector Error Correction**

accounts for all major sources of systematic error

The diagram illustrates vector error correction for S-parameters. It shows a vector  $S_{11 \text{ Device}}$  (black arrow) and a vector  $S_{11 \text{ Measured}}$  (blue arrow) originating from the same point. A red dashed line represents the error vectors. A red solid arrow labeled  $S_{11 \text{ Correction}}$  points from the tip of the  $S_{11 \text{ Measured}}$  vector towards the tip of the  $S_{11 \text{ Device}}$  vector, indicating the correction needed to align the measured value with the device's true value.

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Since S-parameters are vectors, all measurement errors contribute with magnitude and phase, and can be considered as additional error vectors. These errors have to be calibrated out with the correction vector  $S_{xx \text{ correction}}$ , as depicted above.



What is a 12-term error correction?

As can be seen above, there are 6 error contribution terms in forward direction, related to the characterizing signals R, A and B of the NWA:

1. Directivity: cross-talk of the power splitter in the NWA testset
2. Crosstalk: cross-talk inside the S-parameter test set, overlying the DUT
3. Source Mismatch: multiple reflections due to impedance mismatch of cables and connectors
4. Load Mismatch: the same for the opposite port
5. Reflection Tracking A/R: frequency dependence of signal path R->A
6. Transmission Tracking A/R: same for signal path R->B

For the reverse calibration, another 6 error terms add up to a total of 12 terms.

The procedure to get rid of these 12 terms is called the 12-term error correction.

### 12 Term Error Correction

**Forward model**

**Reverse model**

<p> <math>E_D</math> = Fwd Directivity      <math>E_L</math> = Fwd Load Match  <math>E_S</math> = Fwd Source Match    <math>E_{RTT}</math> = Fwd Transmission Tracking  <math>E_{RT}</math> = Fwd Reflection Tracking   <math>E_X</math> = Fwd Isolation  <math>E_D'</math> = Rev Directivity      <math>E_L'</math> = Rev Load Match  <math>E_S'</math> = Rev Source Match      <math>E_{RTT}'</math> = Rev Transmission Tracking  <math>E_{RT}'</math> = Rev Reflection Tracking   <math>E_X'</math> = Rev Isolation         </p>	$S_{11a} = \frac{\left( \frac{S_{11m} - E_D}{E_{RT}} \right) \left( 1 + \frac{S_{22m} - E_D'}{E_{RT}'} E_S' \right) - E_L \left( \frac{S_{21m} - E_X}{E_{TT}} \right) \left( \frac{S_{12m} - E_X'}{E_{TT}'} \right)}{\left( 1 + \frac{S_{11m} - E_D}{E_{RT}} E_S \right) \left( 1 + \frac{S_{22m} - E_D'}{E_{RT}'} E_S' \right) - E_L' E_L \left( \frac{S_{21m} - E_X}{E_{TT}} \right) \left( \frac{S_{12m} - E_X'}{E_{TT}'} \right)}$ $S_{21a} = \frac{\left( \frac{S_{21m} - E_X}{E_{TT}} \right) \left( 1 + \frac{S_{22m} - E_D'}{E_{RT}'} (E_S' - E_L) \right)}{\left( 1 + \frac{S_{11m} - E_D}{E_{RT}} E_S \right) \left( 1 + \frac{S_{22m} - E_D'}{E_{RT}'} E_S' \right) - E_L' E_L \left( \frac{S_{21m} - E_X}{E_{TT}} \right) \left( \frac{S_{12m} - E_X'}{E_{TT}'} \right)}$ $S_{12a} = \frac{\left( \frac{S_{12m} - E_X'}{E_{TT}'} \right) \left( 1 + \frac{S_{11m} - E_D}{E_{RT}} (E_S - E_L) \right)}{\left( 1 + \frac{S_{11m} - E_D}{E_{RT}} E_S \right) \left( 1 + \frac{S_{22m} - E_D'}{E_{RT}'} E_S' \right) - E_L' E_L \left( \frac{S_{21m} - E_X}{E_{TT}} \right) \left( \frac{S_{12m} - E_X'}{E_{TT}'} \right)}$ $S_{22a} = \frac{\left( \frac{S_{22m} - E_D'}{E_{RT}'} \right) \left( 1 + \frac{S_{11m} - E_D}{E_{RT}} E_S \right) - E_L \left( \frac{S_{21m} - E_X}{E_{TT}} \right) \left( \frac{S_{12m} - E_X'}{E_{TT}'} \right)}{\left( 1 + \frac{S_{11m} - E_D}{E_{RT}} E_S \right) \left( 1 + \frac{S_{22m} - E_D'}{E_{RT}'} E_S' \right) - E_L' E_L \left( \frac{S_{21m} - E_X}{E_{TT}} \right) \left( \frac{S_{12m} - E_X'}{E_{TT}'} \right)}$
---	---

- Notice that each corrected S-parameter is a function of all four measured S-parameters
- Analyzer must make forward *and* reverse sweep to update any one S-parameter
- Luckily, you don't need to know these equations to use network analyzers!!!

The formulae above are applied in the NWA in order to correct the measured S-parameter  $S_{xyM}$  with the correction terms  $E_{xx}$ , and to finally obtain the requested  $S_{xyA}$  parameters of the device under test (12 term error correction).

It is of particular interest that e.g. the resulting  $S_{11A}$  parameters are affected by *all* measured  $S_{11M}$  parameters ! This means, if there is a problem with 'only one' S-parameter index during measurements (or calibration), this will affect *all* S-parameters. This means, an absolute clean calibration and also an absolute proper measurement is required in order to get good S-parameter results!

## Calibrating a NWA



- **Full 2-port calibration**  
(reflection and transmission measurements)  
12 systematic error terms measured  
usually requires 12 measurements on four known standards (SOLT)
- Standards are defined in **cal kit definition table**  
these cal kit definitions are entered to the network analyzer
- **THE INTERNAL NWA CAL KIT DEFINITION MUST MATCH THE ACTUAL CAL KIT USED!**

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There are many different calibration techniques for network analyzers. Such are Short-Open-Load-Thru (SOLT), Thru-Reflection-Load (TRL) or Load-Reflection-Match (LRM). For the different calibration procedures, specific known standard terminations have to be measured.

The slide above depicts such standards for connectorized measurements (e.g. 3.5mm connectors).

Although there are many publications on the pros and cons of the different calibration methods, the SOLT is most commonly used for on-wafer measurements of silicon devices. One of the reasons is that due to the electrical losses of silicon, microstrip standards as required for LRM and TRL are difficult to manufacture on the wafer. Another reason for using SOLT is that this calibration is a wide-band calibration and not limited to a frequency band.

Some naming conventions:

THE CALKIT:

while in the case of the CV meter, the calibration corrects for a *single, ideal* offset capacitor, a NWA calibration relates to **cal standards** (OPEN, SHORT, LOAD, THRU etc.) from a **calkit**. These cal standards *do not* represent *ideal* standards. They represent the *real, existing standard*, including its nonidealities! It means that a SHORT is not an ideal SHORT, but instead represents rather a small inductance. The same applies to the THRU, which has a non-ideal delay time. The OPEN corresponds rather to a capacitor than to an ideal OPEN. Therefore, these non-idealities of the G-S-G probes have to be entered into the NWA *before* calibration. This is called '**entering**' or '**modifying the calkit**'.

THE CALSET:

While entering the calkit refers to the non-idealities of the calibration standards, i.e. the termination of the NWA cables during calibration, the subsequent **calibration** is based on this information, and then related to the selected

- frequency range,
- the RF power,
- the averaging of the NWA etc.

After the calibration has been performed, the correction terms are stored in the **calset** of the

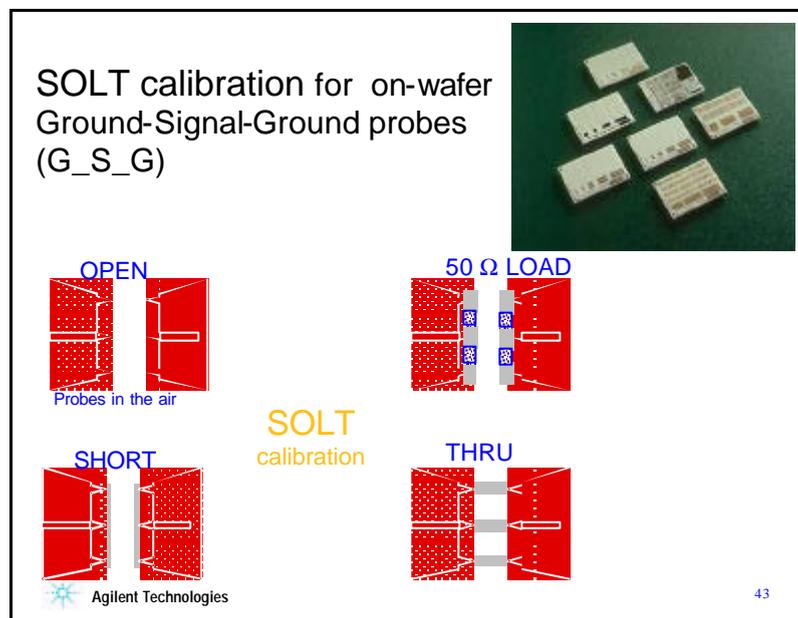
NWA. In other words, the 12-term error vectors are 'filled up', and can be used with the measurements afterwards.

Finally, when the **measurements** are performed, the **raw measured data** arrays will be corrected inside the NWA, using a correction technique related to the selected calibration method, and referring to the specified calset. When using a NWA driver software, this corrected measurement result is transferred into the software and displayed there.

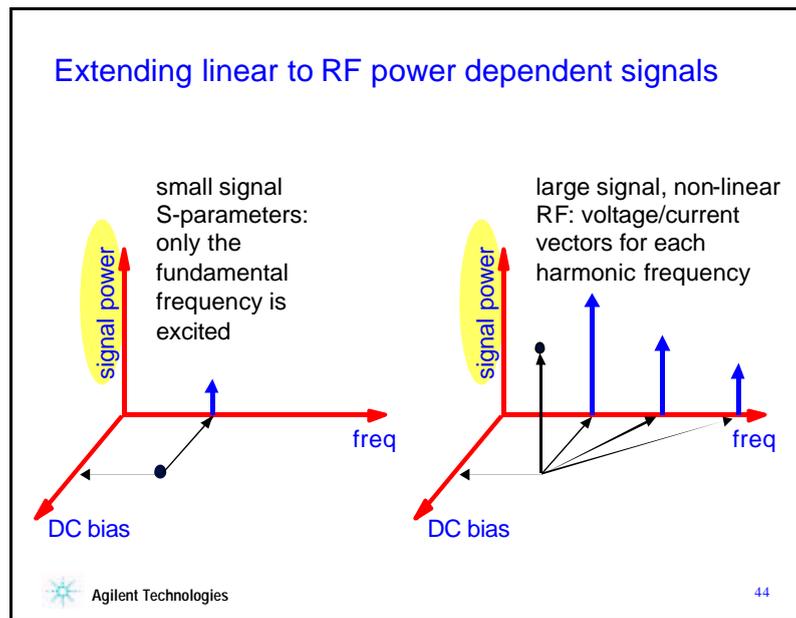
**NOTE:**

After the calibration, a re-measurement of the OPEN will not represent an ideal open, but instead exactly those parasitic components as described in the documentation of the OPEN. In the same way, a THRU shows up after calibration with its real delay time, and a SHORT represents its inductive behavior! If the calibration was ok, the remeasured standards should give exactly the same parameter values as previously entered into the NWA calkit.

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In case of a SOLT calibration, and for on-wafer measurements using Ground-Signal-Ground (GSG) coplanar probes, the slide above depicts the corresponding test structures, which are usually available on a RF-high-performance ceramic substrate, including accurate description of the non-idealities of these standards. These standards (called ISS standards) are provided by the GSG probe manufacturers. Both, the GSG probe and the ISS substrate belong together.



An absolute prerequisite for using S-parameter two-port matrices is the linear, time invariant behavior of the circuit. Only in this case, matrix conversions like for example for de-embedding, are possible! Nonlinear high-frequency measurements cannot be de-embedded by Y- and Z-matrix subtractions!

*What if ...*

***characterizing and modeling a transistor at higher RF signal levels where it behaves non-linear***

If you need to model e.g. a power RF transistor at signal levels where distortion occurs, and where the Kirchhoff law is not fulfilled for the data measured by the NWA (\*), it is absolutely mandatory to replace the *linear* SPICE S-parameter simulation by a *nonlinear* harmonic balance (HB) simulation. Only with this kind of simulation, we can emulate the conditions of the power RF transistor measurement with the NWA. From the simulation data of harmonic balance, we can derive the S-parameters of the base frequency and compare these S-parameters with those obtained from the NWA measurements. Only in this case the obtained model parameters will be correct for the power RF transistor !

(\*) if distortion occurs, harmonic frequencies show up, which by themselves shift the DC operating point. With the NWA plus SMUs, we measure only the (shifted) DC bias current and with the NWA the fundamental frequency current vector. Their sum is *not* zero (!). Kirchhoff's law states that the sum of currents, for all frequencies (including DC) into a node is zero. But with a linear NWA, we do not measure the harmonics frequencies (with magnitude and phase). Only a very special Nonlinear Network Analyzer, not to confuse with standard NWA's, can measure this complete frequency spectrum with respect to magnitudes and phases.

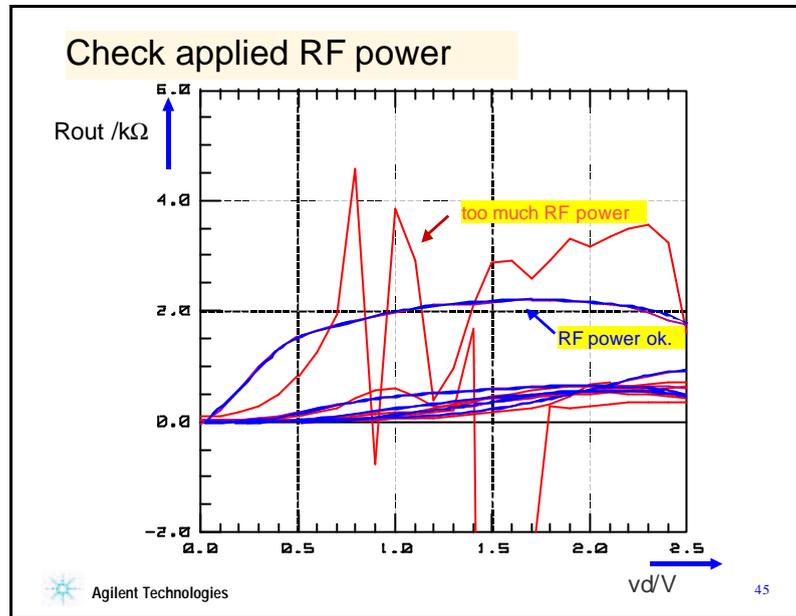
***Conclusions:***

If the DUT behaves non-linearly:

- signal compression occurs
- harmonics show up
- the DC operating point may be shifted

- loadlines and transfer curves become dynamic, i.e. RF-power dependent
- matrix conversions are no longer possible
- de-embedding by S-to-Y and S-to-Z matrix conversion (see further below) is no longer valid.

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Selecting the right RF power for nonlinear devices before starting calibration.

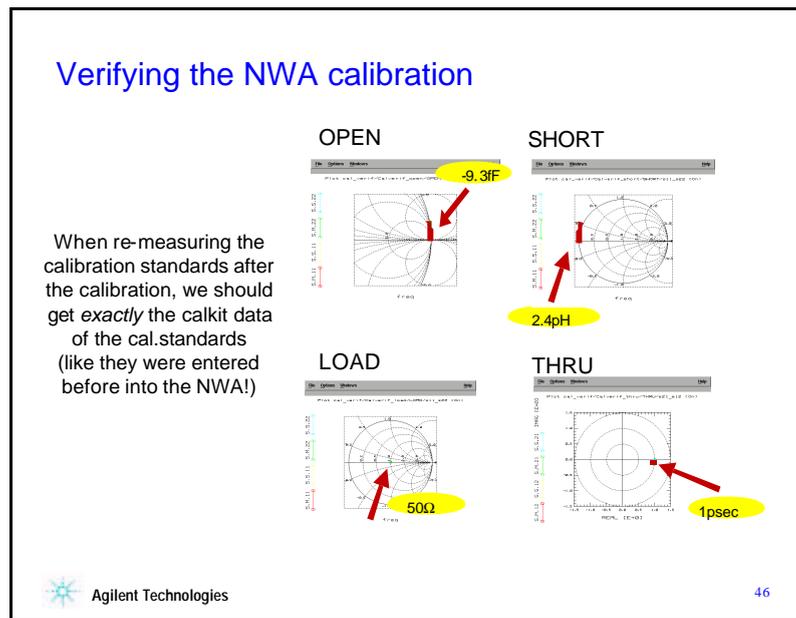
When measuring S-parameters of nonlinear devices with a network analyzer, it must be assured that these devices operate in small-signal, linear mode. Otherwise, the high frequency test signals will no longer be sinusoidal, and the occurrence of harmonics will lead to wrong S-parameter measurements and shifted DC bias conditions.

A smart method to check the correct port power settings is like this: When measuring a DC output characteristics and calculating the output resistor 'Rout' from of it, the resulting curve is very sensitive. Therefore, we can use this plot to identify possible effects of too big an AC power applied to the transistor. This means, we measure the DC output characteristics, and let the NWA perform untriggered measurements, in continuous mode, i.e. unsynchronized to the DC measurement. Then, we increase the Port power manually (or decrease the port attenuations) until we see an effect on the next 'Rout' measurement. We then know the maximum allowed RF power for the S-parameter measurements of this device!

The plot above reflects such a test. The disturbed curve happens when too much RF power is applied to the transistor.

NOTE:

'too much RF power' is a relative issue! E.g. -30dBm RF signal (1uW) is small compared to an DC operating point power of e.g. 3V and 1mA (3mW). However, -30dBm can be by far too much RF signal for a DC bias point of e.g. 3V and 1uA (3uW)!! In such a case, for e.g. a diode, the 'relative' big RF signal with its rectification effect (harmonics) will shift the DC bias point. The same small RF signal would be too weak to do the same for a mW DC operating point!



In order to verify the calibration, it is highly recommended to re-measure the calibration standards and to model them, using the calkit data of the GSG probe or the connectorized standards.

As an example, for an on-wafer SOLT calibration, we re-measure the cal.standards, e.g. the OPEN, the SHORT, the THRU and the LOAD. We know that this measurement will correspond to the nonidealities of the selected cal.standard, as specified in the NWA calkit data. In case of Cascade probes, the OPEN, for example, behaves like a negative capacitance of roughly  $-9\text{fF}$ . Now, after this measurement has been made, we can define a test circuit for that Setup in a modeling software package like IC-CAP, and enter the netlist of these calibration standards. Using SPICE3, a simulator which also permits negative capacitances, we can simulate the expected behavior of the OPEN probes. If the calibration was executed correctly, there is an excellent match between measured and simulated curves.

In a next step, we measure the SHORT, define in IC-CAP the SHORT nonidealities in a SPICE circuit, and simulate. Again, an excellent match between measured SHORT data and simulations has to be achieved. We then continue with the THRU and LOAD measurements and simulations.

Only if all 4 standards exhibits an excellent fit, we can assume a correct calibration of the NWA.

Note: This calibration verification can also be applied to check the quality of an older calibration.

The results depicted in the slide above give an example for Cascade G-S-G probes, 100um pitch.

Once again, only if the fitting between simulated and measured data is in the few-percent range, for all 4 re-measured calibration standards, the NWA calibration can be considered as good. If only one fit is bad, re-perform a new NWA calibration !!

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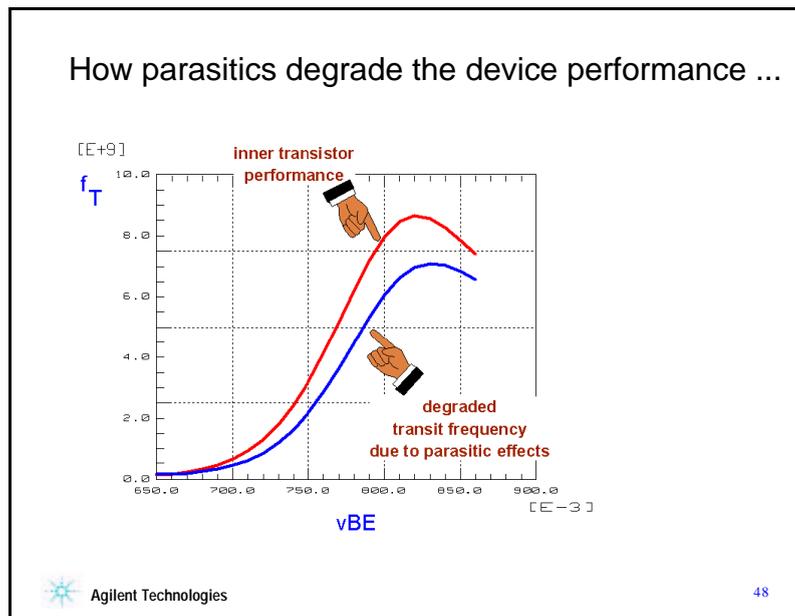
Basics of DC and AC Characterization of Semiconductors

Contents

- Basics of device measurement and modeling techniques from DC to RF
- Special aspects of network analyzer calibration
- De-embedding and required dummy structures

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## Slide 48

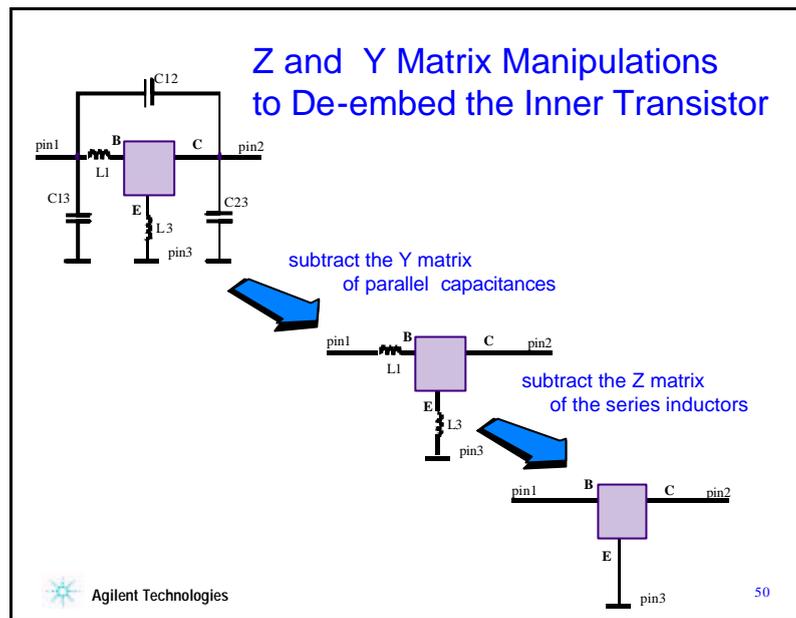


After having performed a network analyzer calibration, the calibration plane is located at the ends of the NWA cable connectors (connectorized devices) or at the ends of the probe contacts (on-wafer measurements). The device itself, including its surrounding parasitics, is then connected to this calibration plane.

In the case of a packaged device, S-parameter measurements would now include the test fixture, the package and the very inner DUT. For on-wafer device characterization, using e.g. ground-signal-ground probes (GSG), the test pads (where the probes touch down) degrade the performance of the inner DUT by their layout specific capacitive and pad parasitics.

In order to extend the calibration plane to either the beginning of the package, or to the inner DUT, these outer parasitic effects have to be stripped off. This is called de-embedding.





By rearranging the schematic components, we obtain a simplified equivalent schematic as given above.

In order to strip off the parasitic components from the outside towards the inner DUT, the slide shows the corresponding de-embedding procedure.

#### De-embedding procedure:

We have measured the S-parameters Stotal of the transistor including the carrier parasitics. With the assumption of having *nothing but* parallel capacitors as 'outer' parasitic components, we transform the S-parameters to Y, because a Y matrix represents a PI structure of components. A simple subtraction will de-embed the parasitic capacitor effects.

Now, the new 'outer' parasitic components are the two inductors, which are in series with the chip connections. Series parasitics can be easily eliminated by subtracting a Z matrix. Therefore, we transform the resulting Y-parameters from above into Z-parameters and subtract the inductors.

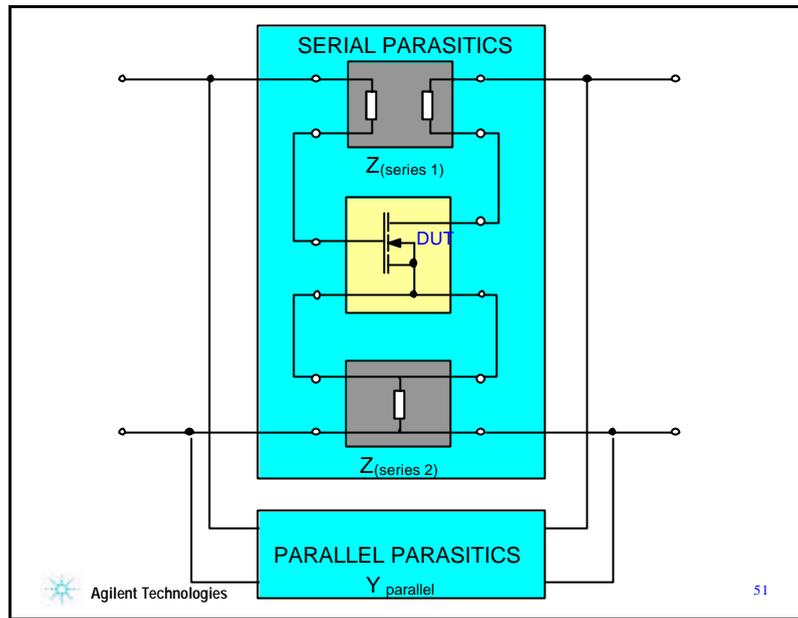
These Z-parameters are finally transformed back into S-parameters which now describe exclusively the performance of the 'inner' chip.

#### NOTE:

particularly for on-wafer measurements, de-embedding by subtracting the complete Y matrix (OPEN) and Z matrix (SHORT) is often applied. However, in this case, it must *absolutely* be assured that

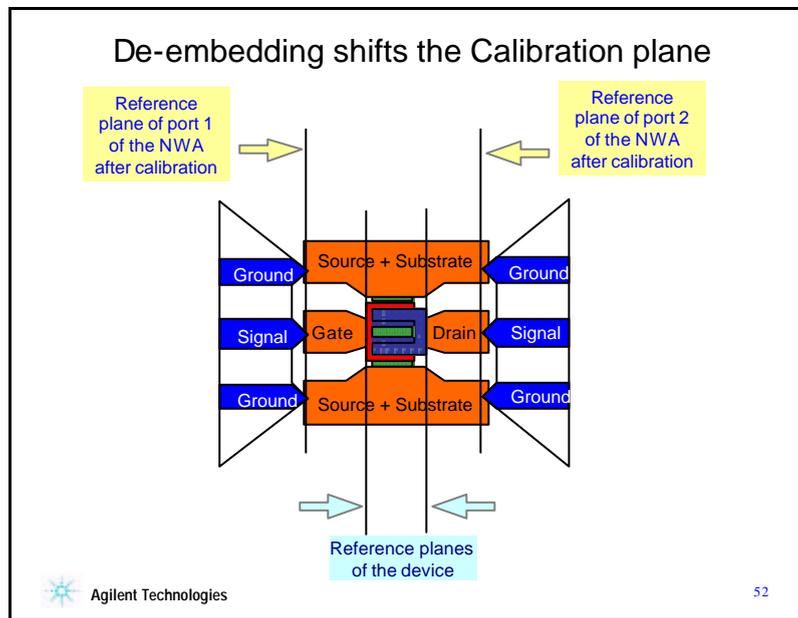
- there are no hidden series components present for Y-matrix subtractions (mixed cross-talk represented by chains of C-L-C-L etc.).
- there are no hidden parallel components present for Z-matrix subtractions.
- related to a two-step de-embedding:
  - for on-wafer measurements (OPEN → SHORT sequence):  
the SHORT has been de-embedded from the OPEN dummy.
  - for packaged measurements (SHORT → OPEN sequence):  
the OPEN has been de-embedded from the SHORT dummy.
- there are no hidden delay line effects present when subtracting the Y- or Z-matrices.

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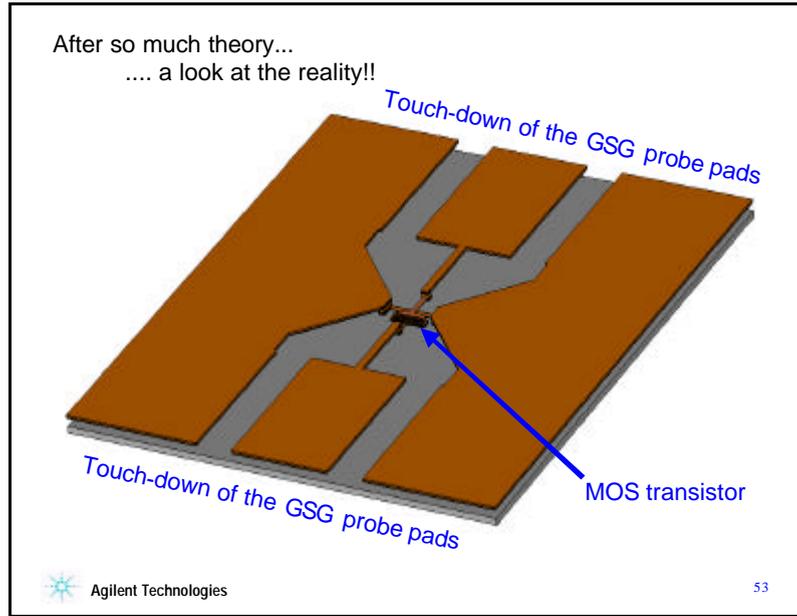
The slide above sketches the de-embedding situation for a transistor with first capacitive parasitics, followed by inductive parasitics.

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And this slide above once again visualizes the shift of the calibration plane due to de-embedding.

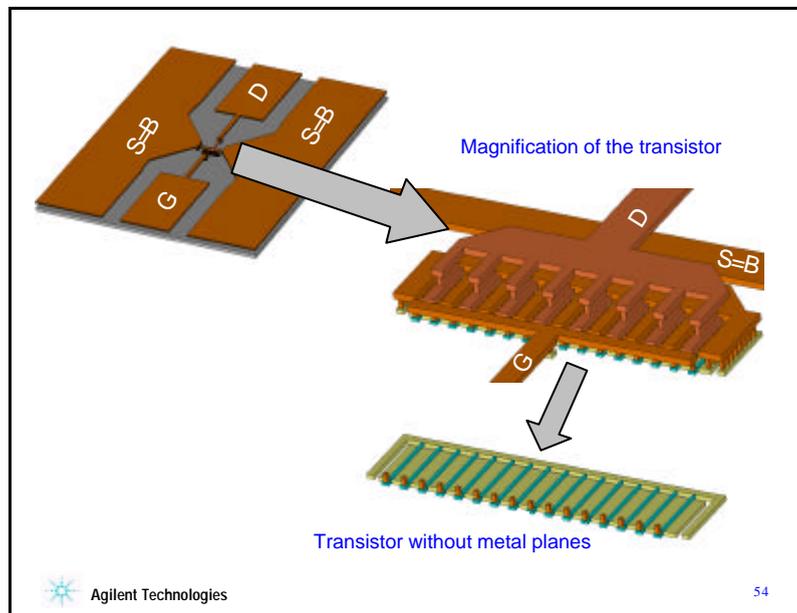
Slide 53



This slide depicts a three-dimensional representation of such a MOS transistor in its on-wafer test environment. It is interesting to note that the size of the transistor itself is very small compared to the size of the pads!

The goal of de-embedding is to shift the NWA calibration plane, which was (after the NWA calibration) at the end of the probe tips, down to the beginning of the transistor. This 'beginning' is one of the key points for a good de-embedding and a key point for good dummy structures.

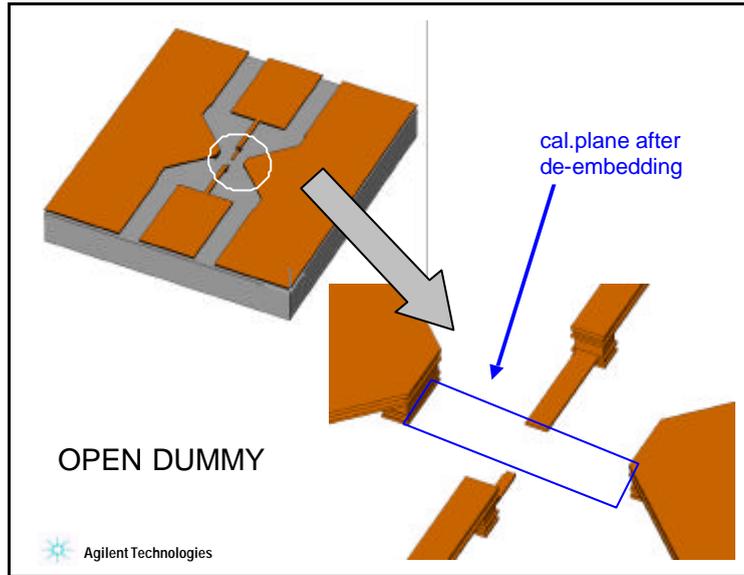
Slide 54



In the above slide, in the section 'Magnification of the transistor' is the inner transistor, which we want to model. All the rest has to be de-embedded, i.e. to be stripped-off. In other words, the NWA calibration plane has to be shifted down here.

NOTE: watch how 'high' the metal planes are relative to the active silicon area. A real mountain of metalization!

Slide 55



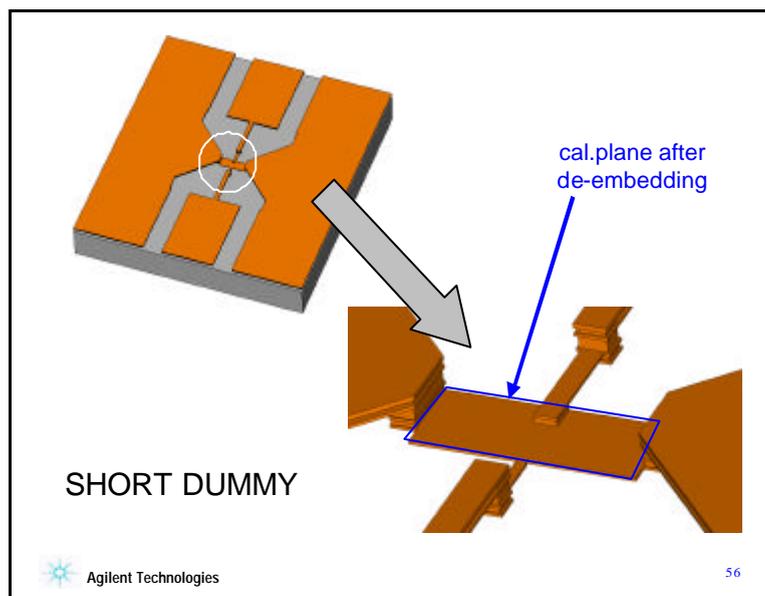
The pre requisite for a correct de-embedding is that certain test structures are available on a wafer together with the device under test (DUT) itself. Depending on the selected de-embedding method, an OPEN and SHORT dummy structure is required and must be measured. For a de-embedding verification, also a THROUGH dummy structure is necessary. The principle layouts of these structures are given in the actual and the next slides. These layouts are for Ground-Signal-Ground Probes (GSG).

Please check the 'after-de-embedding' calibration plane as marked in the figures. Everything, every part of the DUT included in these cal. plane will be part of the DUT model !

In other words, you can think of de-embedding as a shift of the current calibration plane to these new limits on the wafer.

In other words: the limits of the blue surrounded area in the OPEN dummy will become the shifted calibration plane. All what is inside will become part of the transistor model!

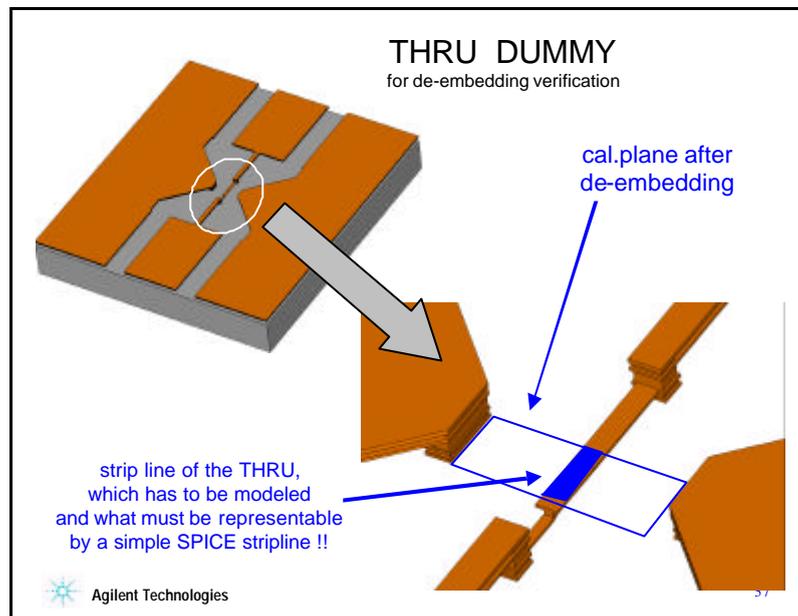
Slide 56



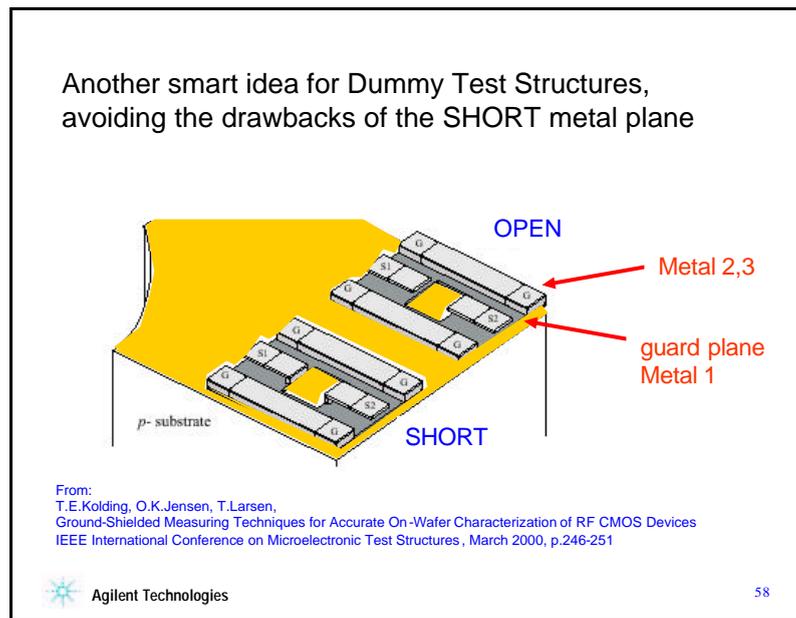
The SHORT dummy again refers to the desired shifted calibration plane. All what is inside this plane is now filled up with metal, so that we can consider this part to behave ideal, while

the striplines from Gate and Drain will behave like inductors and will show up with the SHORT dummy measurement.

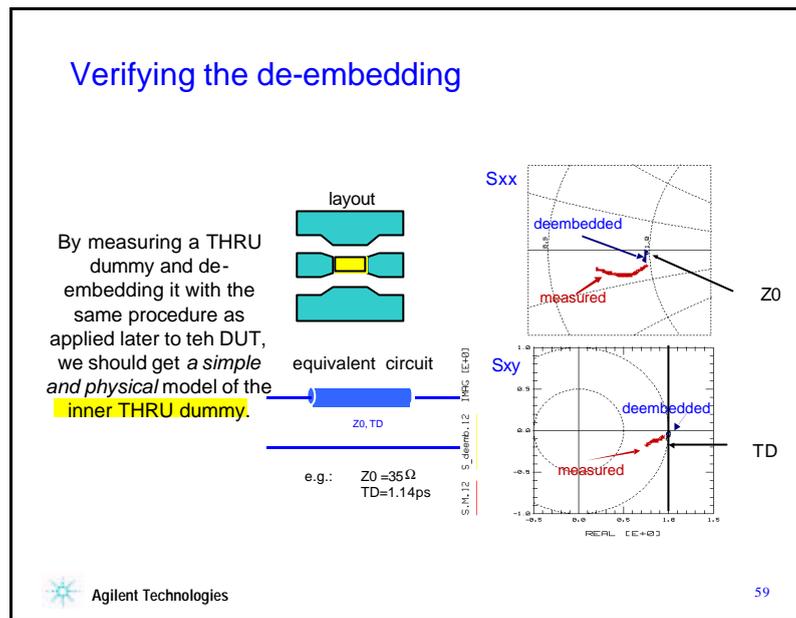
Slide 57



This is the THRU dummy, for de-embedding verification purpose. Instead of the transistor, we now have a strip line (metal 1). See the next slides for a proposed de-embedding verification procedure..



Instead of the 'classical' layout shown in the previous slides, today's layouts for silicon wafers look more and more often like the one shown in the slide above. It avoids the effects of the lossy silicon substrate by using the 1st metal plane to shield the contact pads and the lines to the DUT against the lossy silicon substrate. Especially interesting is the drastically improved SHORT dummy performance, since it applies a series of vias to ground (metal 1) at the end of the SHORT, rather than having - as with the conventional SHORT- a large metal plane (the SHORT) which is considered as ideal, while the two microstrip lines (to the contact pads) of the SHORT dummy are considered as non-ideal. Also, the OPEN is much more ideal with this alternate approach. Altogether, this layout suggestion of using the 1st metal as a shield features lower parasitics. Therefore, the de-embedding is not so much the 'difference of big numbers' like in the conventional layout suggestions, and therefore more robust.



Verifying the de-embedding procedure is very important before applying it to the very DUT, i.e. the transistor, the passive RF component etc.

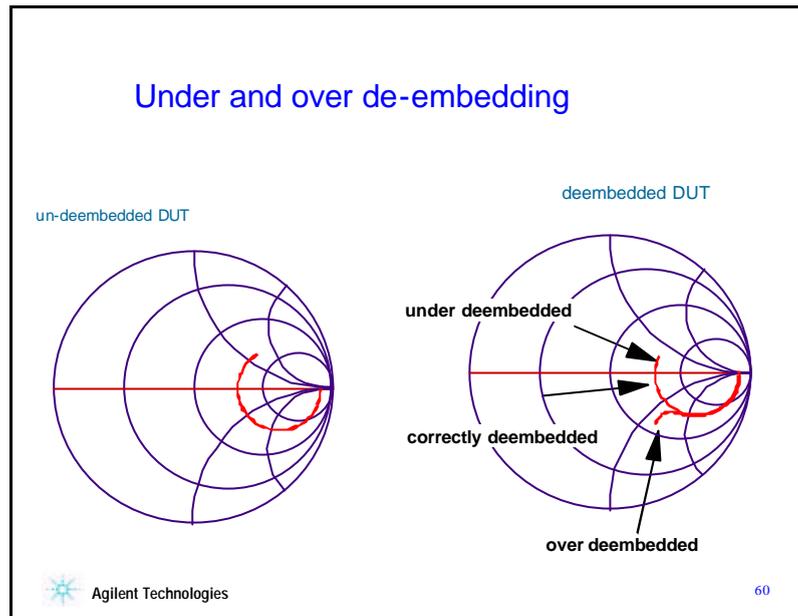
Without this verification step, errors or problems associated with the de-embedding will add to the performance of the inner, de-embedded device, and, thus, lead to a wrong measurement result, and finally to a wrong device model. This is especially critical when de-embedding (subtracting) the complete Y and Z matrices of the OPEN and SHORT dummy, because, in this case, possible problems may not show up compared to de-embedding of individual, lumped components. (With de-embedding lumped components, we would have detected such problems because they would show up with non-physical values!).

Therefore, it is suggested to

- model every dummy structure before simply subtracting their total matrices in order to verify its de-embedding prerequisites:
  - > for the OPEN dummy: no series parasitics allowed!
  - > for the SHORT dummy: no parallel parasitics allowed !

and additionally, to

- verify the de-embedding procedure with a well-known 'golden device', e.g. the proposed THRU strip line, before applying the de-embedding procedure to the very DUT.



Some remarks on the under- and over-de-embedding.

**UNDER-DEEMBEDDING**

If under-deembedding occurred, i.e. we deembed 'not enough parasitics', what means the lumped components values were estimated too small, the de-embedded traces will not be 'turned back' sufficiently, resulting in a too big a delay time. The de-embedding error will add up to the inner device and distort its model.

The better visible effect is

**OVER-DEEMBEDDING**

If over-deembedding occurred, however, the deembedded DUT curves will 'turn backwards' for higher frequencies or show some other non-physical effects. They may even turn outside the Smith chart!

This emphasizes once again the need to accurately verify the de-embedding procedure *before* applying it to the very DUT.

**CONCLUSIONS**

In this measurement overview presentation, we have considered some important aspects of

- Basics of device measurement and modeling techniques from DC to RF
- Special aspects of network analyzer calibration
- De-embedding and required dummy structures

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