Agilent EEsof EDA

Presentation on Basics of RFIC Design Examples

This document is owned by Agilent Technologies, but is no longer kept current and may contain obsolete or inaccurate references. We regret any inconvenience this may cause. For the latest information on Agilent's line of EEsof electronic design automation (EDA) products and services, please go to:

www.agilent.com/find/eesof

Agilent Technologies

2001 IEEE GaAs IC Symposium

Basics of GaAs, InP, and SiGe RFICs

RFIC Design Examples

Stephen I. Long
Dept. of Electrical and Computer Engineering
University of California, Santa Barbara, CA 93106

RFIC Design Examples

- Digital: static frequency divider
- Analog: wideband transimpedance amplifier
- Emphasize design and analysis techniques
- Simulation complements but does not replace analytical techniques

Application Example #1

- 1. Digital: Static Frequency Divider
  - Why SFD?
  - Device figures of merit & equivalent circuit model
  - How to increase clock frequency
    - Delay analysis: RC delay terms
    - Device parameters, current density, scaling

Why Static Frequency Dividers?

Master-Slave Flip-Flop

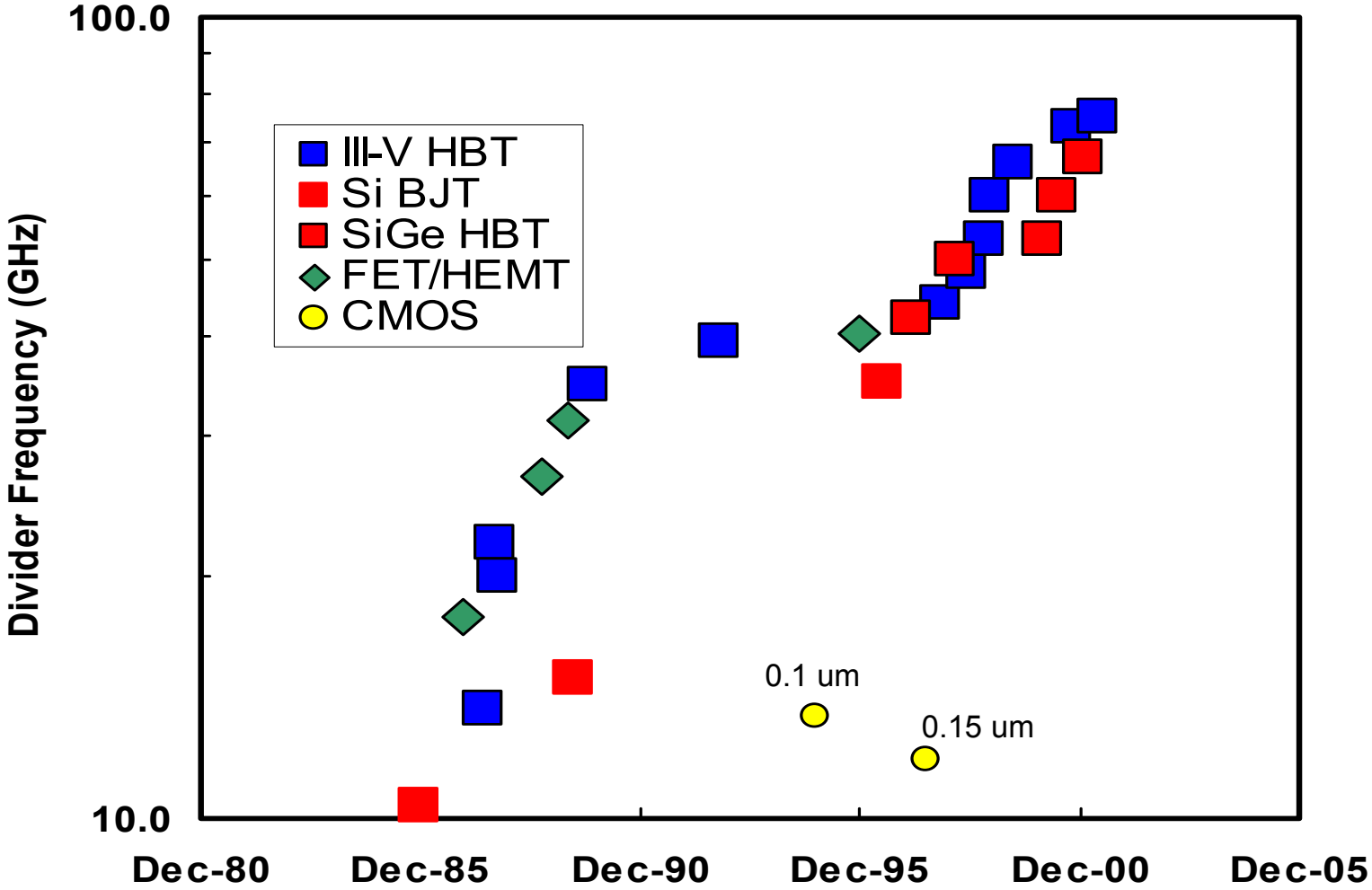
MS flip-flops resynchronize data to clock connection as 2:1 frequency divider provides simple test method.

Standard benchmark of logic speed

performance comparisons across technologies

Technology	Max freq (GHz)	Power (mW)	Ref.
Si MOSFET	16.8	3	5.2
Si BJT	30	630	5.3
AlGaAs/GaAs HBT	34.8	495	5.4
InAlAs/InGaAs PHEMT	49.2	290	5.5
SiGe HBT	67	175	5.6
InAlAs/InGaAs HBT	72.8	55	5.7
InAlAs/InGaAs TSHBT	75	800	5.8

Logic Speed: III-V vs. Silicon



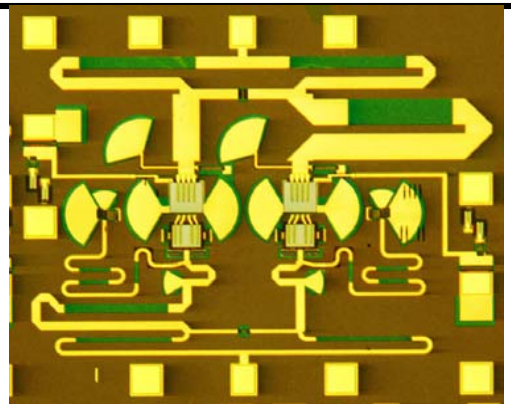
Benchmark: master-slave flip-flop configured as 2:1 **static** frequency divider

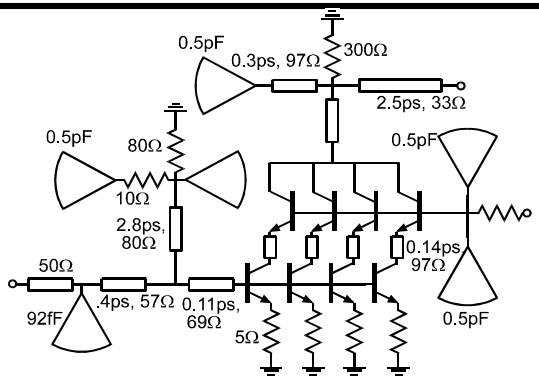
Source: M. Sokolich, HRL, M. Rodwell, UCSB

What do we need: f_τ , f_{max} , or … ?

Tuned ICs (MIMICs, RF):
fmax sets gain,
& max frequency, not ft.

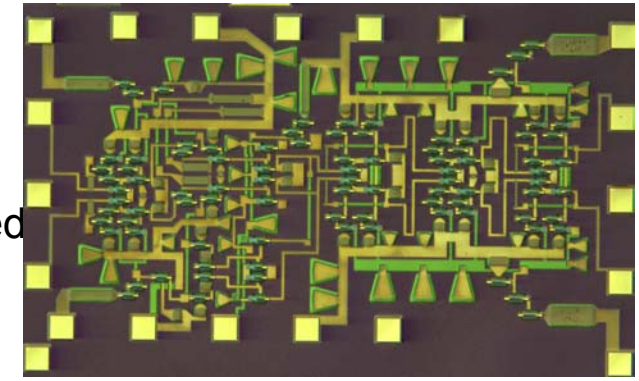
…low ft/fmax ratio makes tuning design hard (high Q)

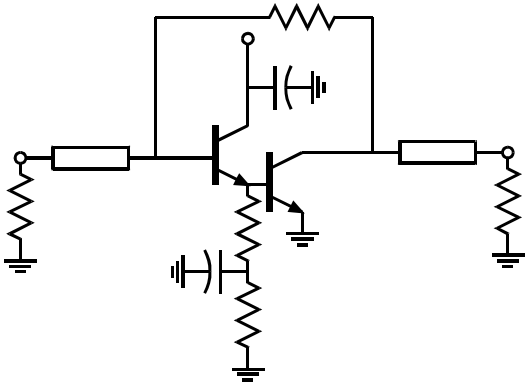




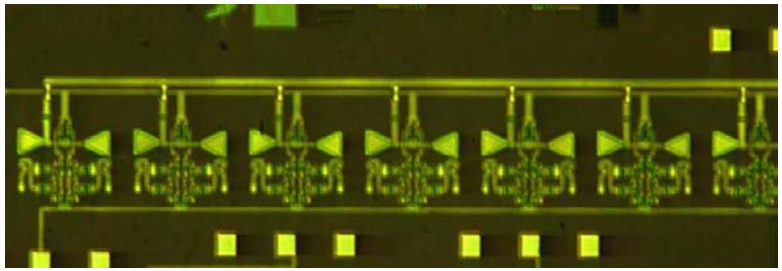
Lumped analog circuits
need high & comparable ft and fmax.

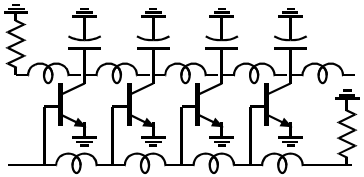
(1.5:1 fmax/ft ratio often cited as good…)





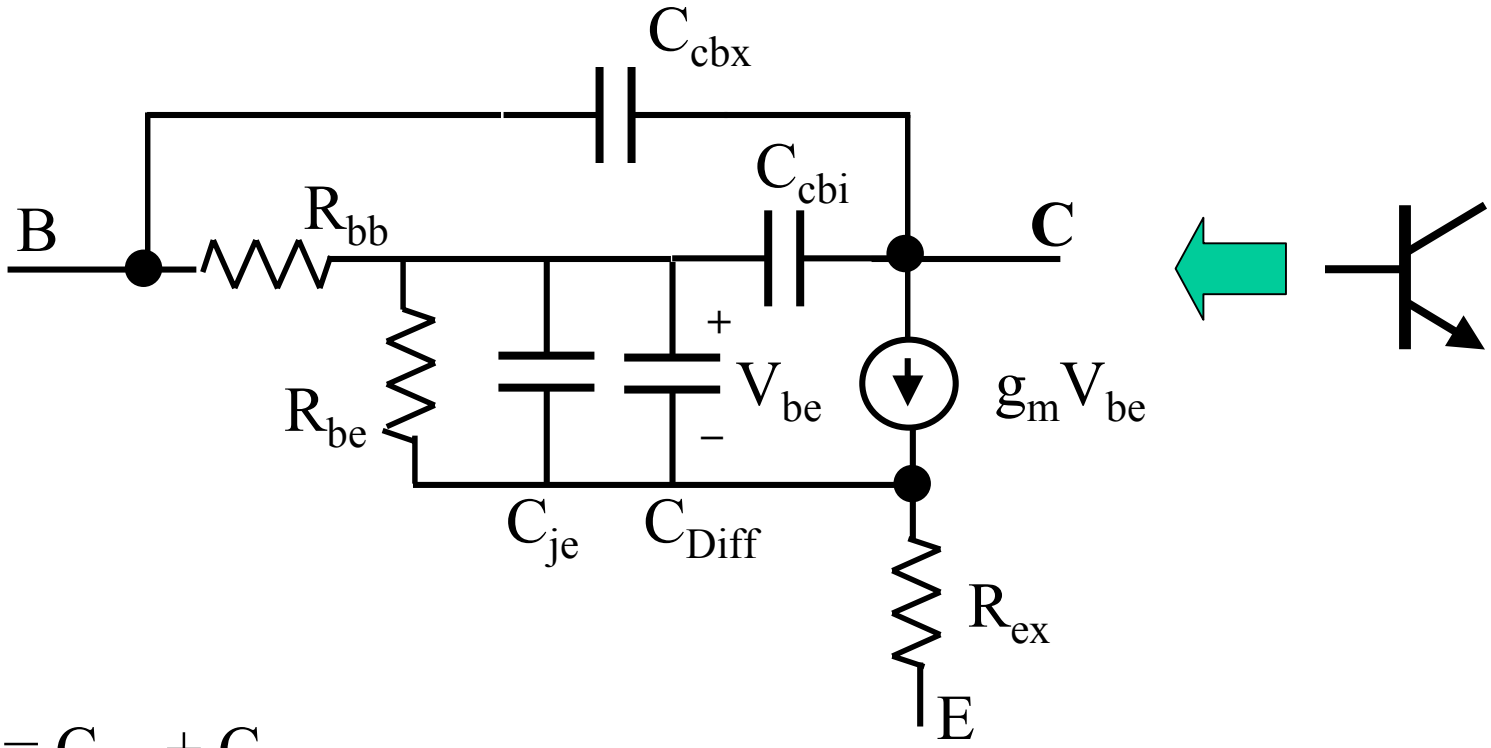
Distributed Amplifiers
in principle, fmax-limited,
ft not relevant….
(low ft makes design hard)





M. Rodwell, UCSB

Hybrid pi HBT equivalent circuit



$C_{cb} = C_{cbi} + C_{cbx}$

C_{cbi} is adjusted to give the correct f_{max}. Not geometrically determined

$C_{diff} = g_m(\tau_b + \tau_c)$

What determines digital circuit speed?

- Neither f_T nor f_{max} predict digital circuit speed

$$\frac{1}{2\pi f_T} = \tau_B + \tau_C + \frac{kT}{qI_C}\left(C_{je} + C_{cb}\right) + \left(R_{ex} + r_c\right)C_{cb}$$

$$f_{\max} = \sqrt{f_T / 8\pi R_{bb} C_{cb}}$$

- RC time constant analysis can guide the design
- Must consider both large signal and small signal parameters as required by circuit application

Propagation Delay Estimation

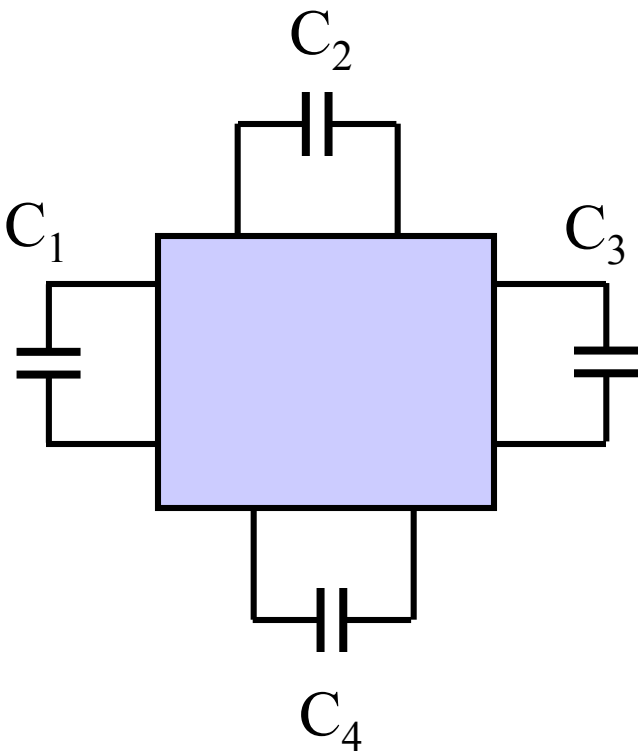
- Find t_{pd}
  - Analytical model can identify dominant time constants
  - Determine sensitivity to:
    - Device parameters
    - Bias current, voltage swing, device area
    - Wiring delays, loading due to fanout
- SPICE or ADS simulation
  - accurate as the device models
  - Estimate of t_{pd} doesn't give great insight
  - Can use for sensitivity analysis – $\Delta t_{pd}/\Delta x_i$

Analytical Delay Models

- Elmore/Ashar requires deriving H(s)
  - Frequency domain
  - Nasty unless circuit is small [Refs 4.1, 4.8]
- Open-Circuit Time Constants [Refs.4.3, 4.4]
  - Easy. The method decouples the circuit
  - Uses linearized equivalent device model
  - Always predicts equal rise/fall times
- Charge control analysis: $\Delta t = \Delta Q/2I$ [Ref. 4.7]
  - Similar result to OCTC method

Open-circuit time constants

- Redraw network with all capacitors outside the box
- No inductors allowed
- OCTC method can estimate the 3 dB bandwidth and the propagation delay
- Assume <u>first order dominant pole</u>. Moderate error if complex conjugate poles or zeros in the network.



Ref. 4.3, 4.4

Open-circuit time constants

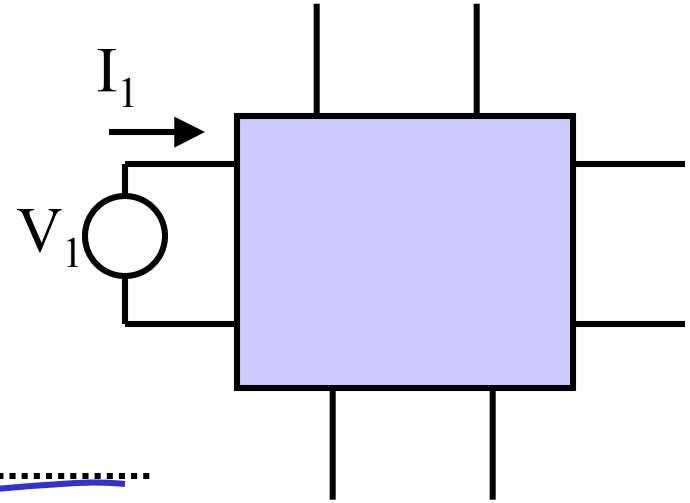
Remove all capacitors

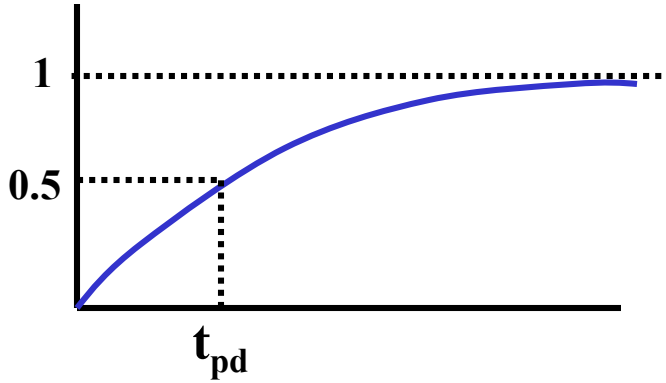
$R_{ii}^{o} = V_i/I_i$ open circuit R presented to i^{th} capacitor

$$a_1 = \sum_{i=1}^{n} R_{ii}^{o} C_i$$

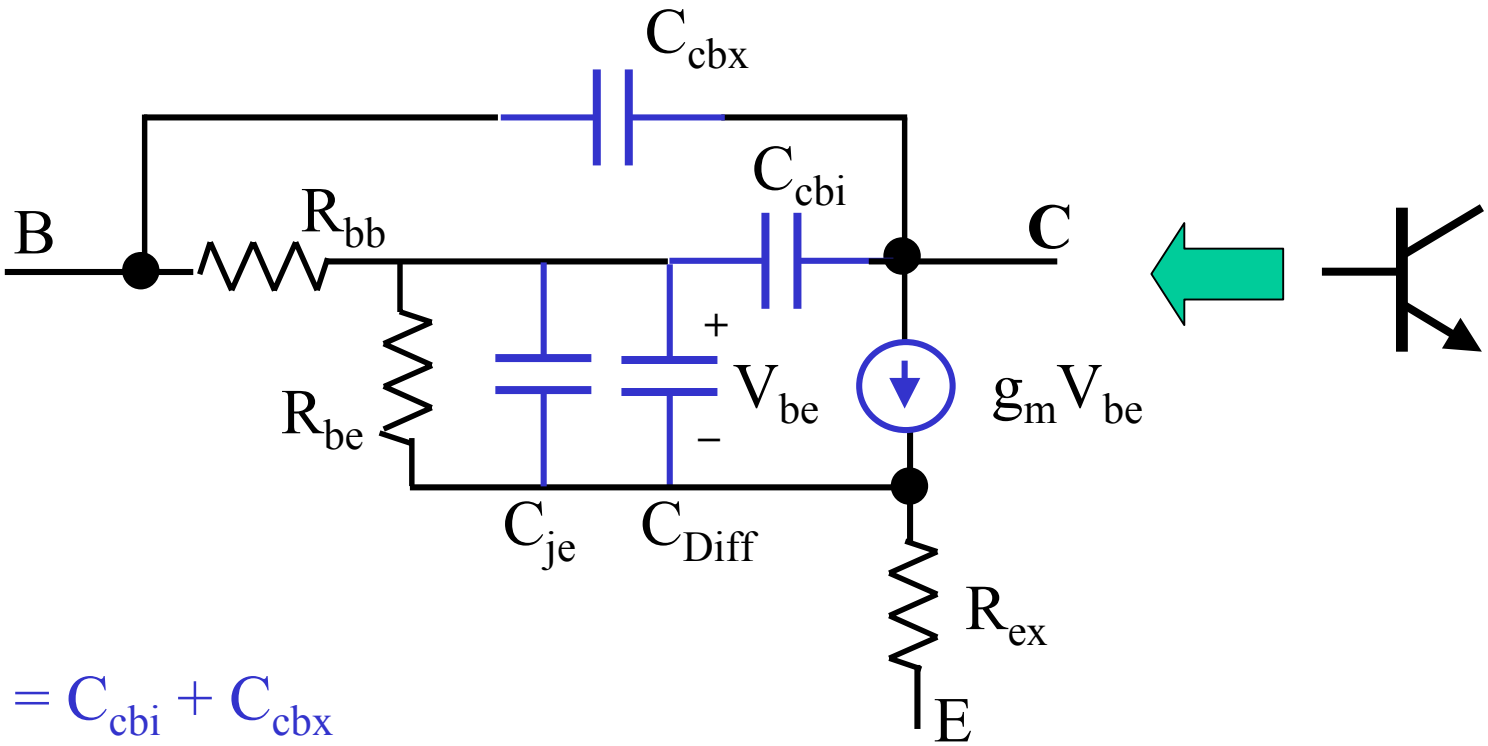
$$f_{3dB} = \frac{1}{a_1}$$

$$t_{pd} = (\ln 2) a_1$$





Hybrid pi HBT equivalent circuit



$C_{cb} = C_{cbi} + C_{cbx}$

C_{cbi} is adjusted to give the correct f_{max}. Not geometrically determined

$C_{diff} = g_m(\tau_b + \tau_c)$

Ref: 4.10

Propagation Delay Estimation

1. All nonlinear capacitances are linearized over the appropriate voltage range:

Depletion capacitances (Mainly C_{je})

$$C_{eq} = \frac{\Delta Q}{\Delta V} = \frac{Q(V_H) - Q(V_L)}{V_H - V_L} = K_{eq} C_{j0}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_H - V_L)(1-m)} \left[(\phi_0 - V_H)^{1-m} - (\phi_0 - V_L)^{1-m} \right]$$

Ref. 4.7

Propagation Delay Estimation

Diffusion Capacitance

Charge storage in base and collector regions

$$\boldsymbol{C_D = \tau_F G_M}$$ Large signal

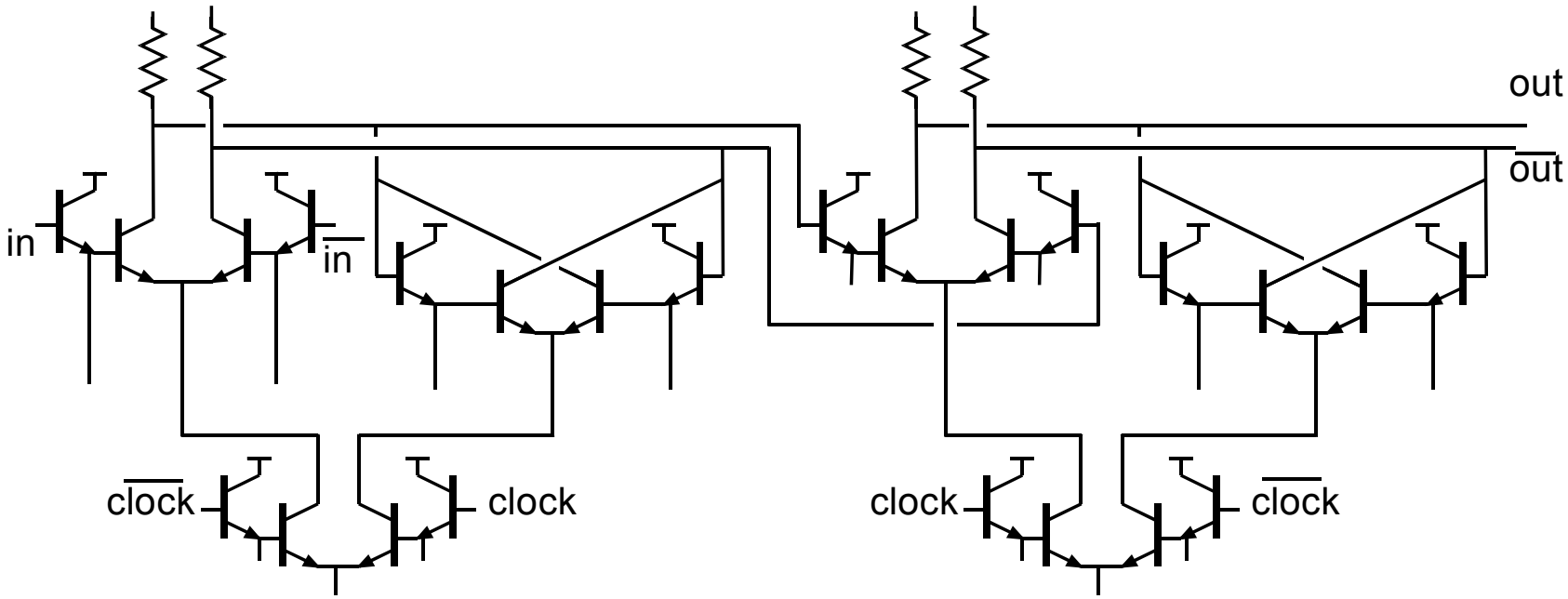
$$C_D = \tau_F g_m = \frac{\tau_F q I_C}{nkT}$$ Small signal

Transconductance is linearized for large signal case:

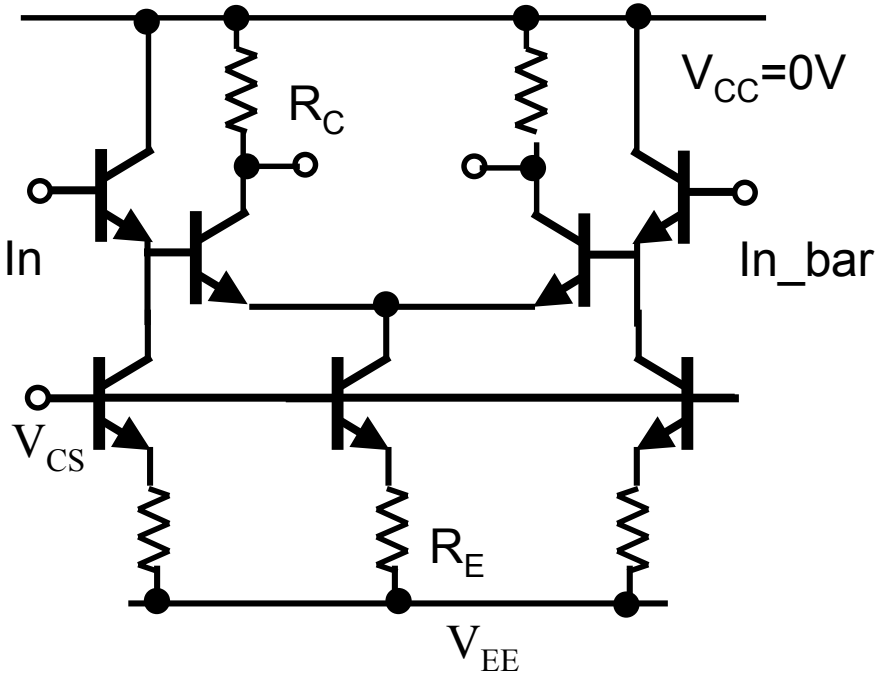
$$G_M = \frac{I_C(V_H) - I_C(V_L)}{V_H - V_L} = \frac{I_{EE}}{\Delta V_{Logic} - I_{EE} R_{ex}}$$

Ref. 4.7

Master-Slave Flip-Flop

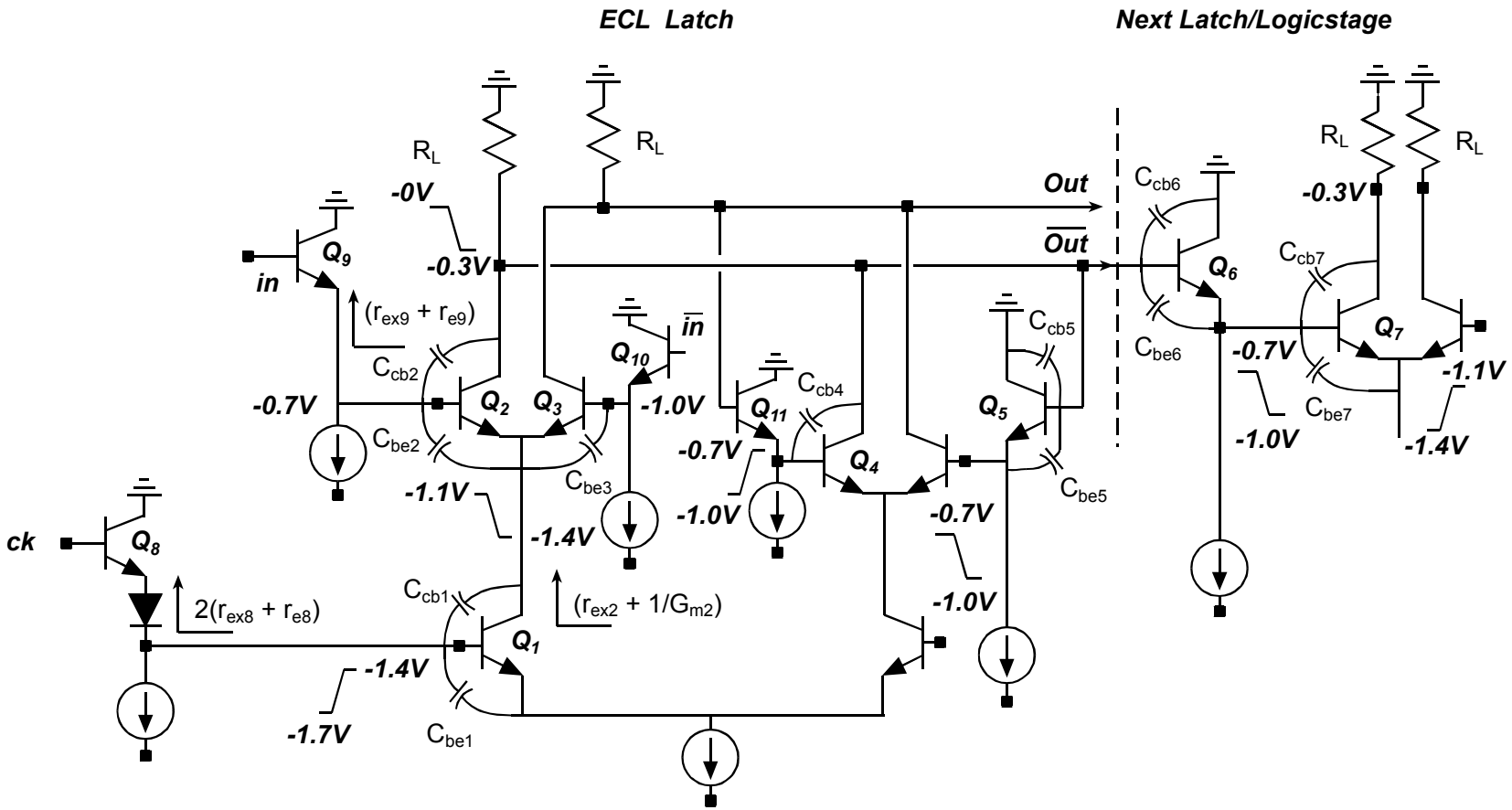


ECL DC Design



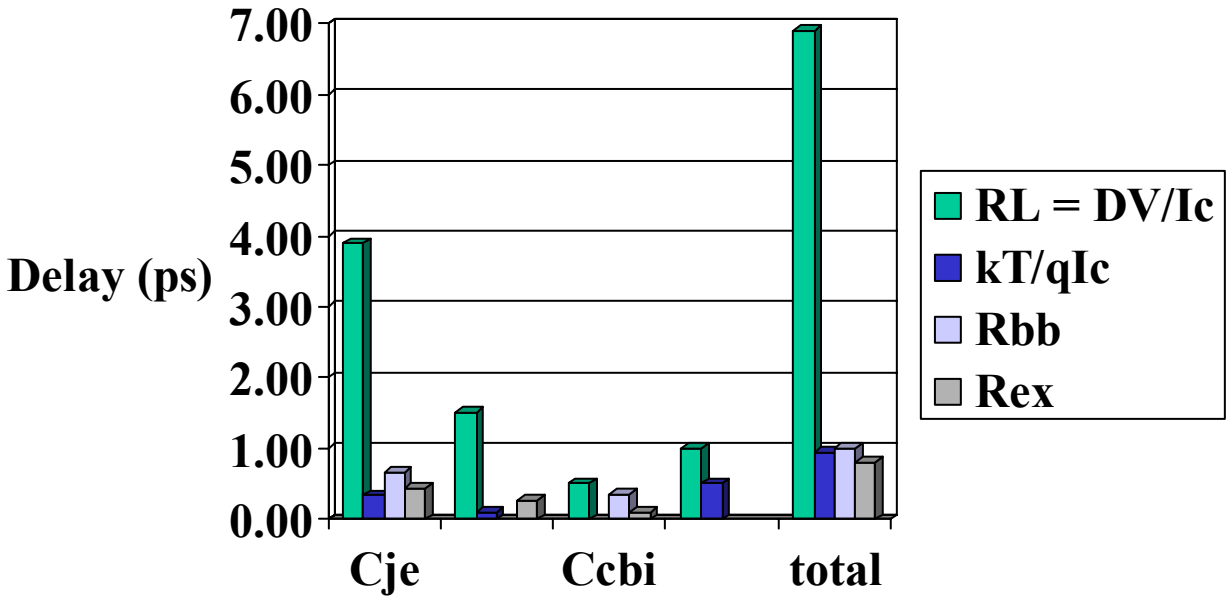
1. $\Delta V > 6\ (kT/q + Ic\ Rex)$
2. Bias devices at peak f_T, J_{max}
3. All devices active or cutoff
4. Thermal limitations

DC analysis: determine voltage swings



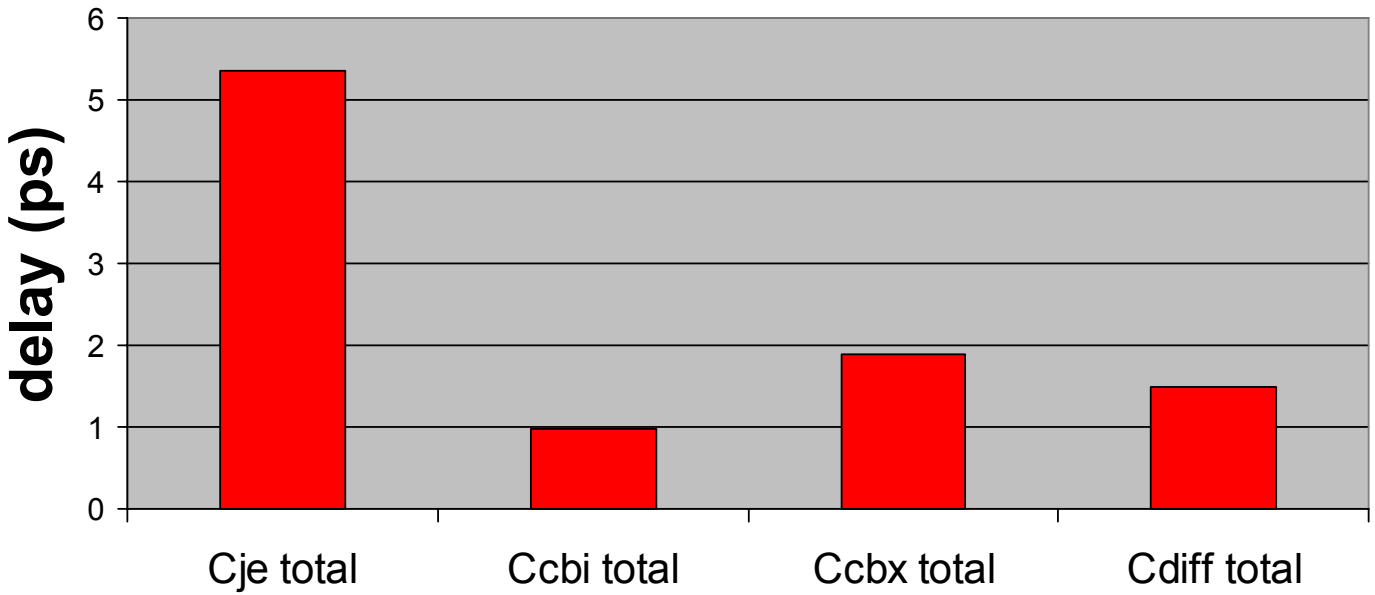
Source: T. Mathew, UCSB

What HBT parameters determine logic speed ?



Calculate R_{ii}^0 C_i time constants for each capacitor

Relative contribution of capacitances



Total delay = τ = 9.7 ps $\quad t_{pd} = 0.7\ \tau = 6.8$ ps

SFD maximum clock frequency = $1/(2t_{pd})$ = 73.5 GHz

What HBT parameters determine logic speed ?

	Cje	Ccbx	Ccbi	Cdiff	total	%
RL = ΔV/Ic	3.90	1.50	0.50	1.00	6.90	71
kT/qIc	0.34	0.10	-	0.50	0.94	10
Rbb	0.66	-	0.35	-	1.00	11
Rex	0.44	0.27	0.10	-	0.81	8
total	5.34	1.90	1.00	1.50	9.70	100
% of total delay	55	20	10	15	100	

Sorting delays by capacitances:

55% C_{je}; 30% C_{cb}; only 15% C_{diff} [e.g. $(\tau_b + \tau_c)$]

Sorting delays by resistances and transit times:

71% $\Delta V_{logic}/I_C$; 11% R_{bb}; 15% $(\tau_b + \tau_c)$

R_{ex} has a strong indirect effect

$$\Delta V > 6(kT/q + R_{ex}I_C)$$

What do we need for fast logic ?

Gate Delay Determined by :

Depletion capacitance charging through the logic swing

$$\left(\frac{\Delta V_{LOGIC}}{I_C}\right)\left(C_{cb}+C_{be,\text{depletion}}\right)$$

Depletion capacitance charging through the base resistance

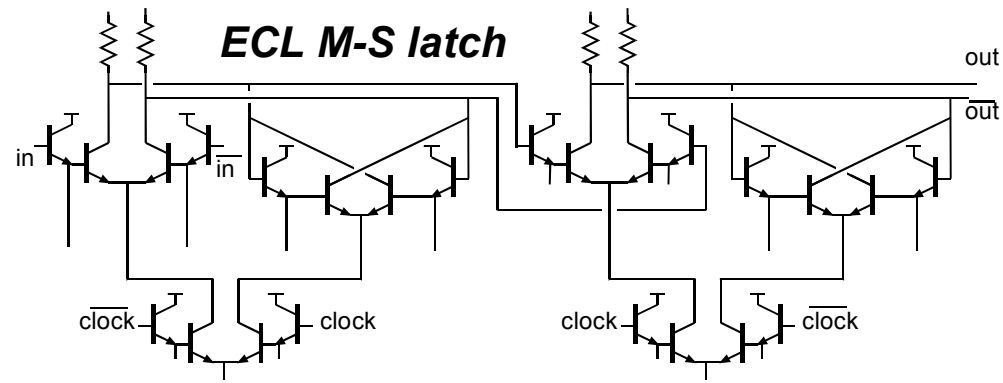
$$R_{\text{bb}}\left(C_{cb}+C_{be,\text{depletion}}\right)$$

Supplying base + collector stored charge through the base resistance

$$R_{\text{bb}}\left(\tau_b+\tau_c\right)\left(\frac{I_C}{\Delta V_{LOGIC}}\right)$$

The logic swing must be at least

$$\Delta V_{LOGIC} > 6\left(\frac{kT}{q}+R_{ex}I_c\right)$$



Neither f_τ nor f_{max} predicts digital speed

$C_{cb}\Delta V_{logic}/I_c$ is very important

→ ***collector capacitance reduction is critical***

→ ***increased III-V current density is critical***

R_{ex} must be very low for low ΔV_{logic} at high J_c

InP: R_{bb} , $(\tau_b+\tau_c)$, are already low, must remain so

Source: M. Rodwell, UCSB

Improving Delay

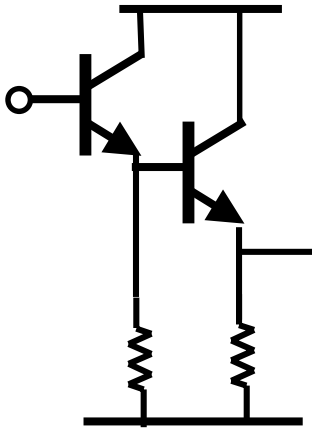
- Optimize emitter width
- Scale device areas for minimum delay
  - emitter areas of emitter follower and diff pair HBTs need to be separately optimized

Improving Delay

- Differential interconnections
  - Lower voltage swing
  - No reference voltage needed
  - Steeper pulse edges
  - Less crosstalk
  - Reduced jitter
- On-chip termination of transmission lines
  - Shunt termination with R_L at input of next stage
  - Even and odd mode terminations

Improving Delay

- Cascaded emitter followers
  - As f approaches f_T, current gain => 1
  - Used in SiGe due to lower f_T
  - Watch out for ringing! Z_{in} can have negative real part.

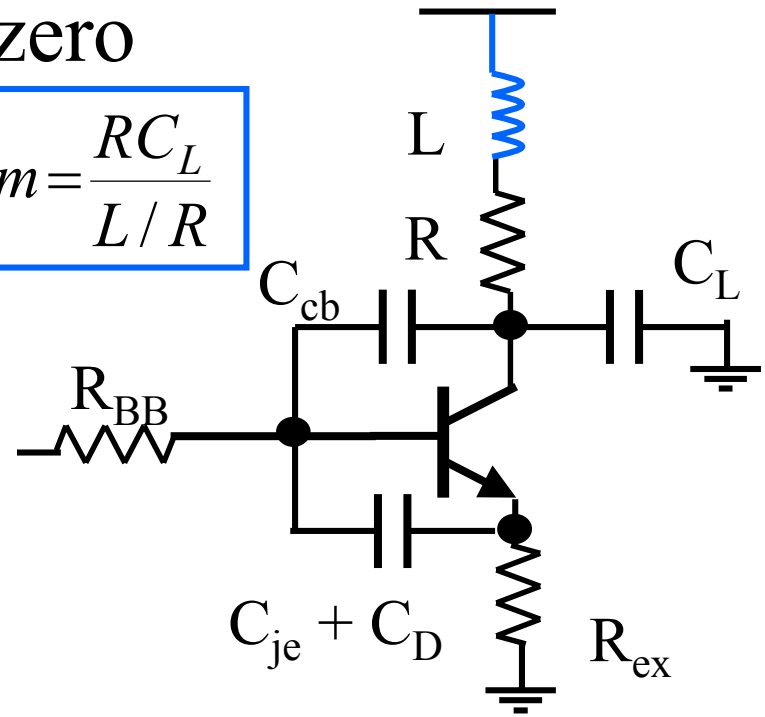


Ref. 4.9

Improving delay

- Shunt peaking: add zero

$$m = \frac{RC_L}{L/R}$$

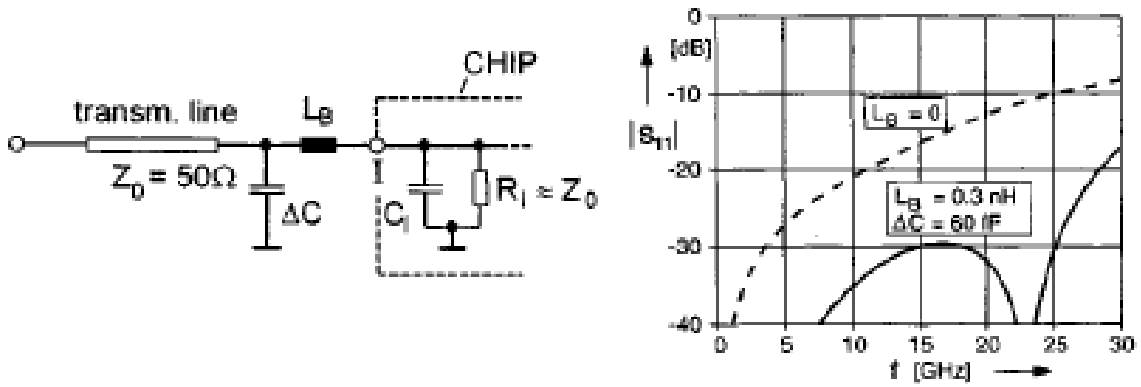


M	Risetime	Overshoot
1.66	2.1	11.4%
2.0	1.9	6.7
2.4	1.7	3.1
4.0	1.4	0
oo	1	0

Ref. 4.11

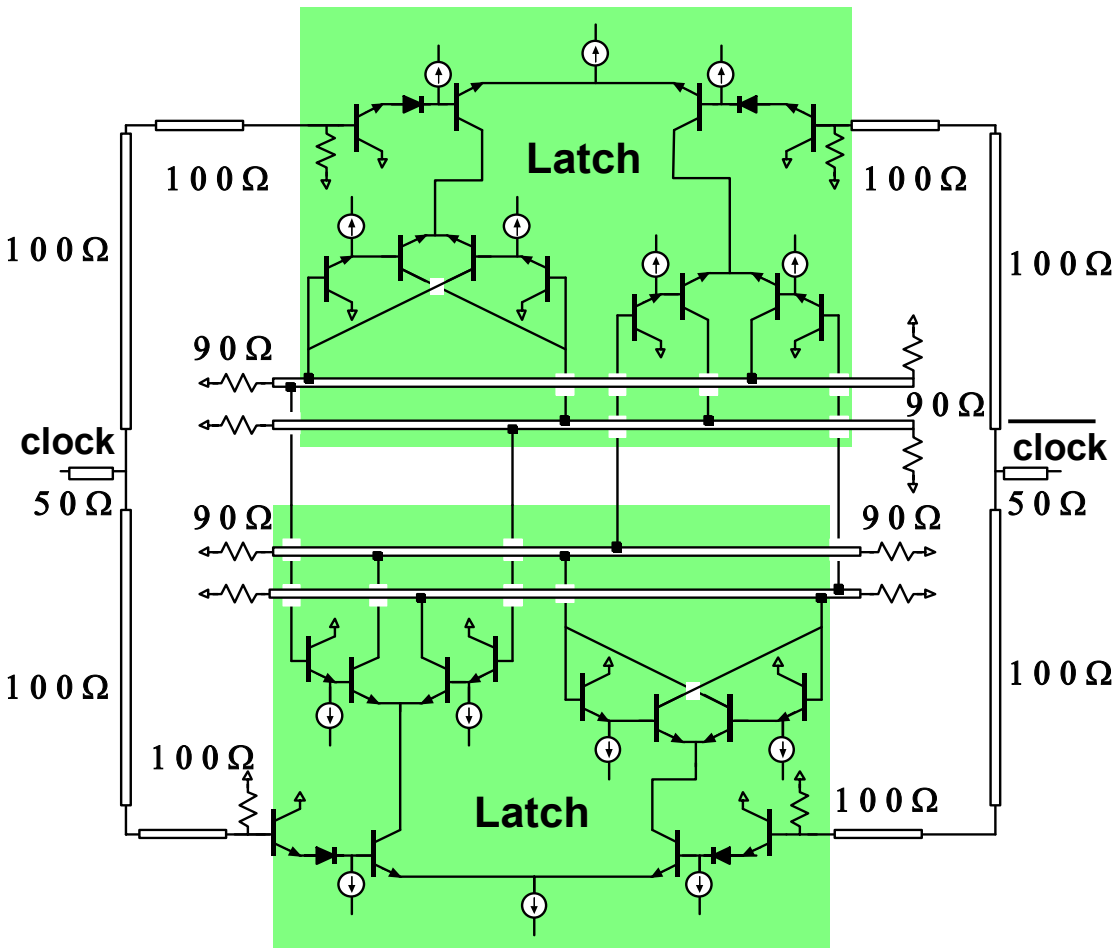
Improving delay

- Parasitic absorption
  - Use bondwire and capacitor to make lumped element transmission line at Z_0



Ref. H. M. Rein and M. Moller, IEEE J. Solid State Cir., pp. 1076-1089, Aug. 1996.

Circuit diagram: Static Frequency Divider



Design specs

- *ECL topology*
- *J_E = 1.0 mA/ μm^2*
- *V_{EE} = - 3.5V*
- *microstrip interconnect lines*
- *Internal node sees ΔV = 300 mV*
- *Output buffer has ~ 100 mV swing.*

Results: 50 - 75 GHz measurements

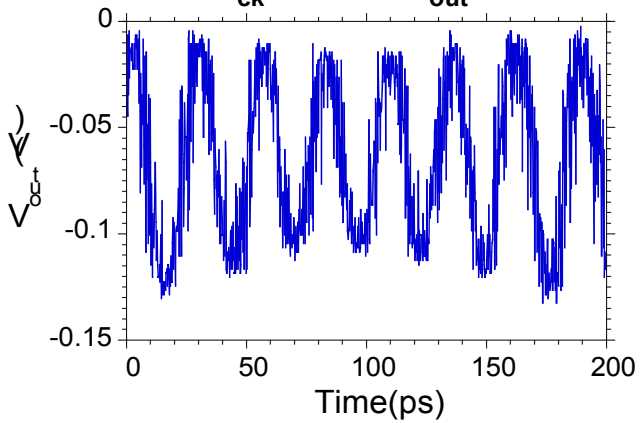
Operating conditions:

V_{EE} = -3.9 V

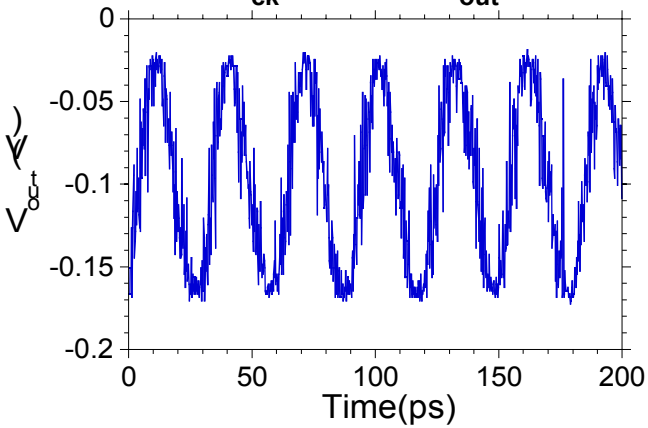
$J_{e\ max}$ = 1.8 mA / μm^2

Power dissipated is 800 mW

Divider: f_{ck}=75GHz, f_{out}=37.5GHz



Divider: f_{ck} = 66GHz, f_{out} = 33GHz



Output waveform on oscilloscope

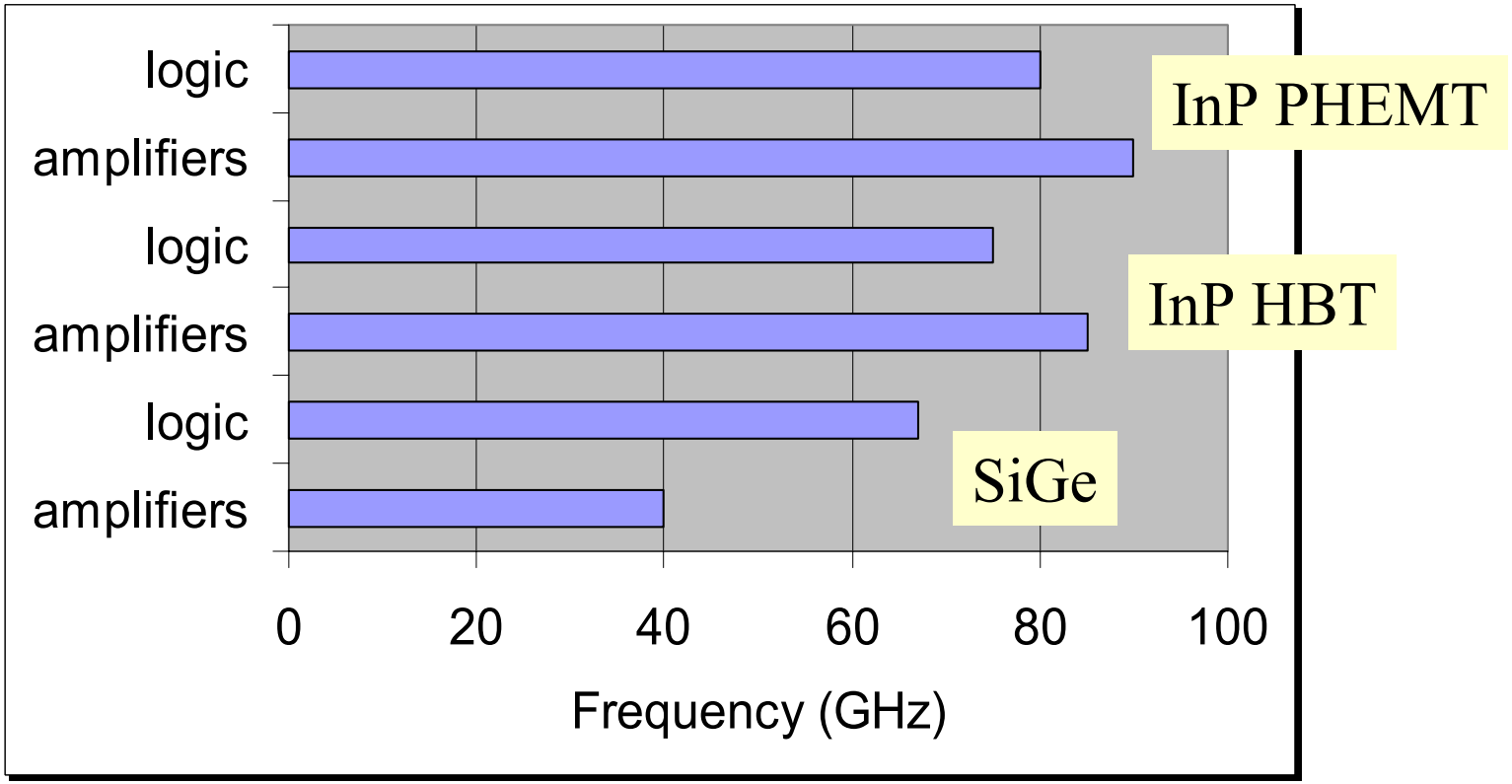
OCTC prediction: 73.5 GHz

ADS simulation: 90 GHz

Maximum measured: 75 GHz

Ref. 5.14

State-of-Art in HBTs, 2001: small-scale circuits



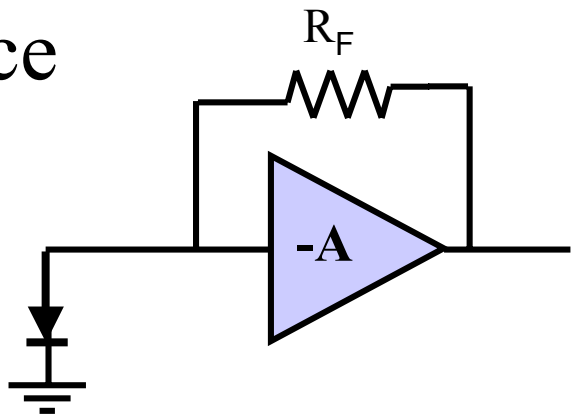
Si / SiGe has rough parity in logic with InP despite lower f_τ, f_{max}

due to higher current density, better emitter contacts

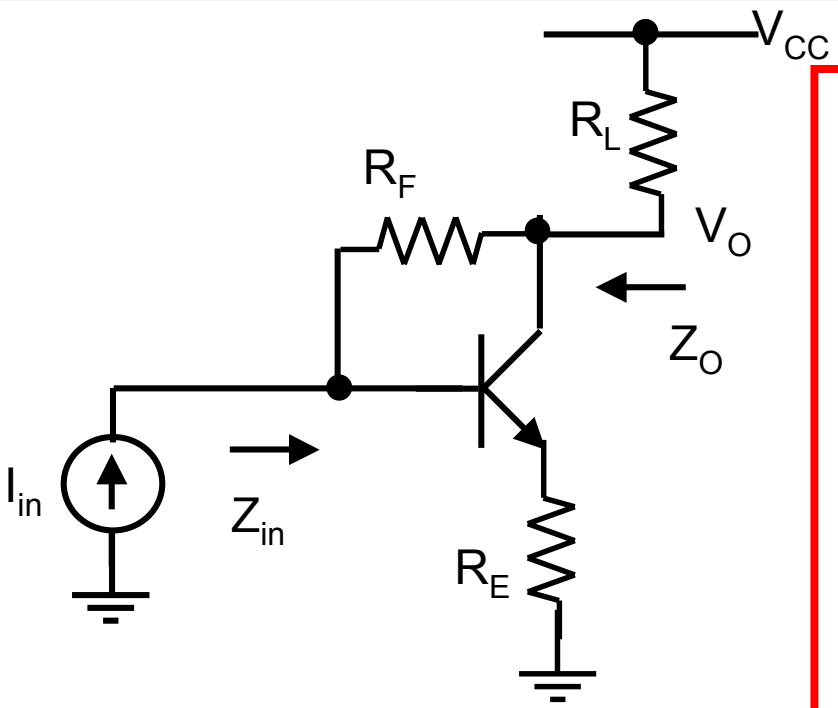
Si/SiGe has significantly slower amplifiers

Analog: application #2: Wideband amplifier

- 2. Photodiode preamp; limiting amps for CDR
  - Well-behaved transient response is essential
  - Data "eye" must remain open
  - Time constant analysis can again be useful
- Study amplifier performance
  - Transimpedance amp
  - Bandwidth enhancement
  - Transient response



TIA 1: CE with dual feedback



Design equations:

$$A_v = \frac{V_o}{I_i R_s} = -\frac{R_L}{R_E}\left[\frac{R_F - R_E}{R_F + R_L}\right]$$

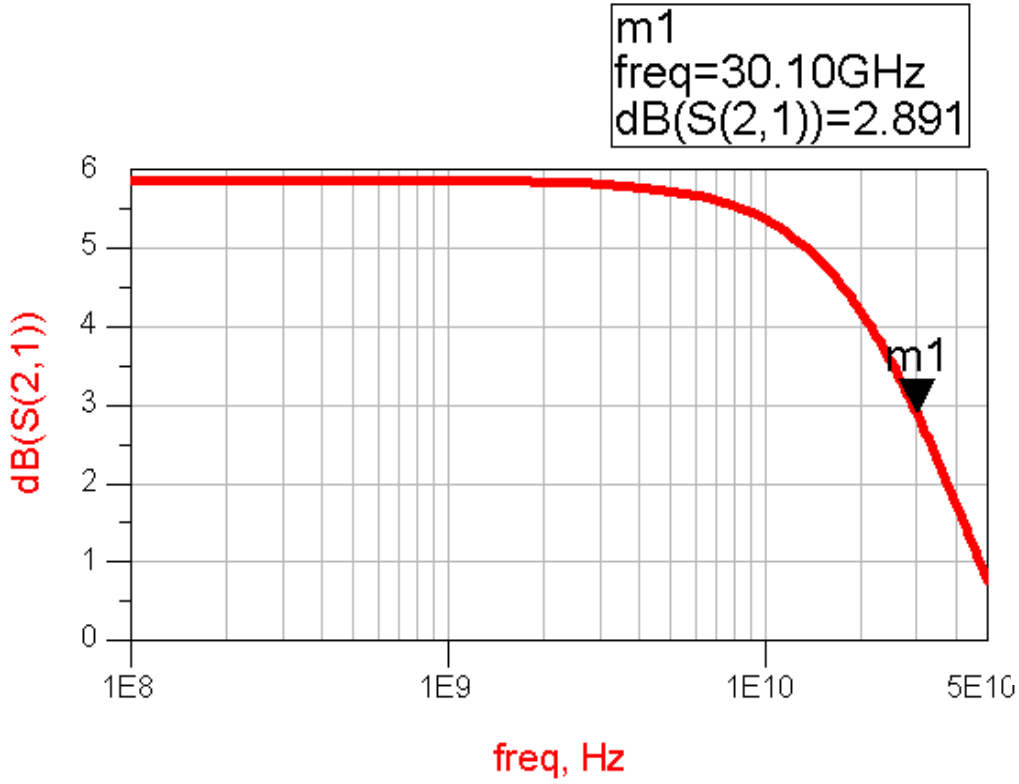
$$Z_o = Z_{in} = R_s = R_L = R$$

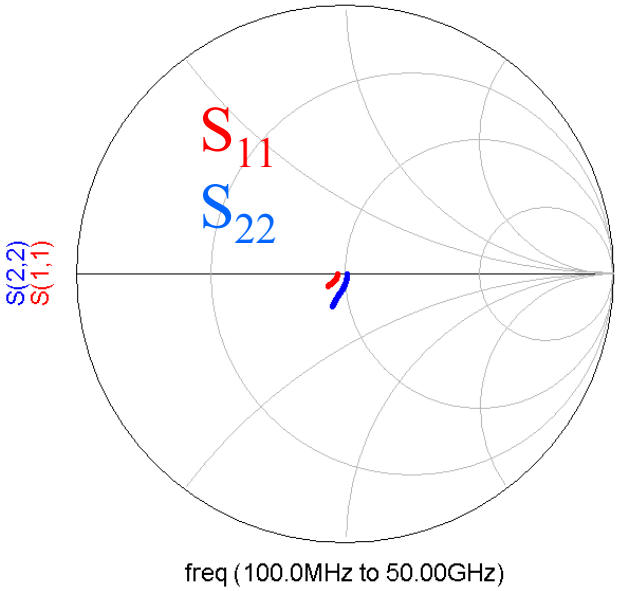
$$R = \frac{R_F}{1 - A_v}$$

R_E and R_L set the gain;
R_F sets Z_{in} and Z_o

Design for 50Ω, S_{21} = 6 dB
InP-based HBTs

CE with dual FB

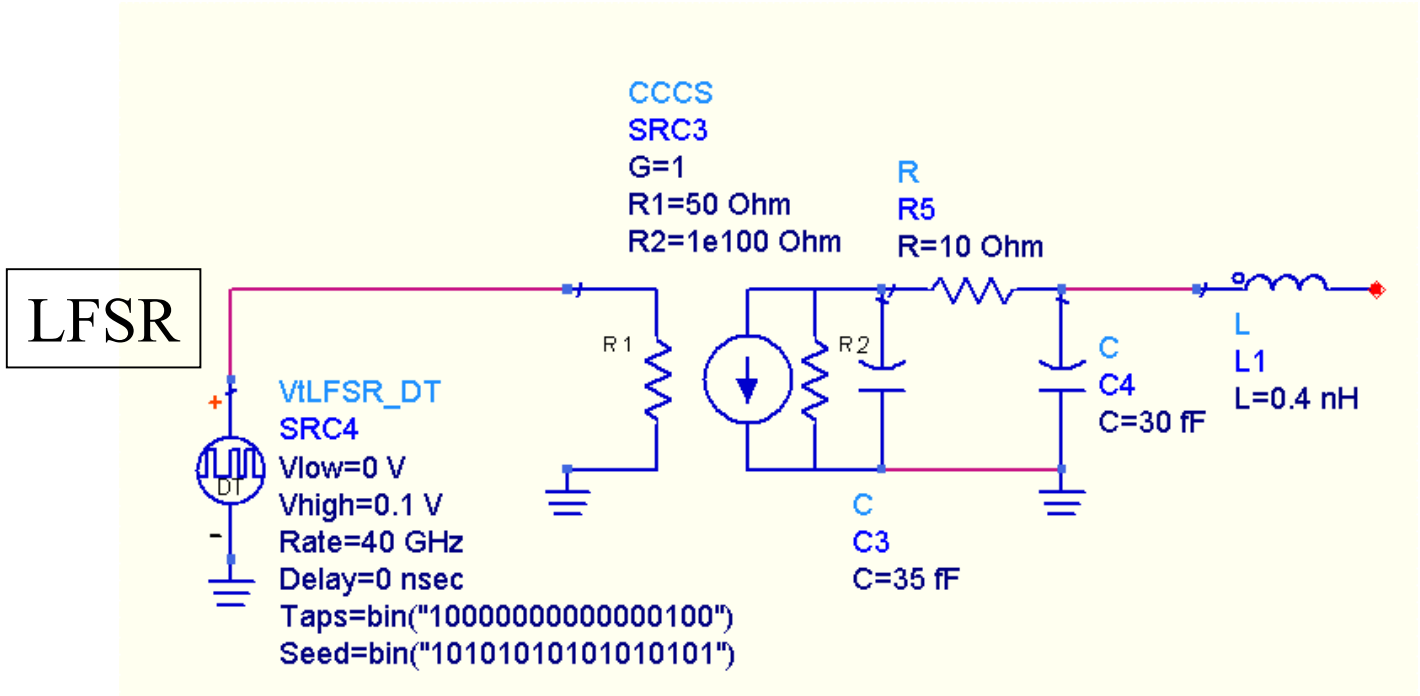




3 dB BW = 30 GHz

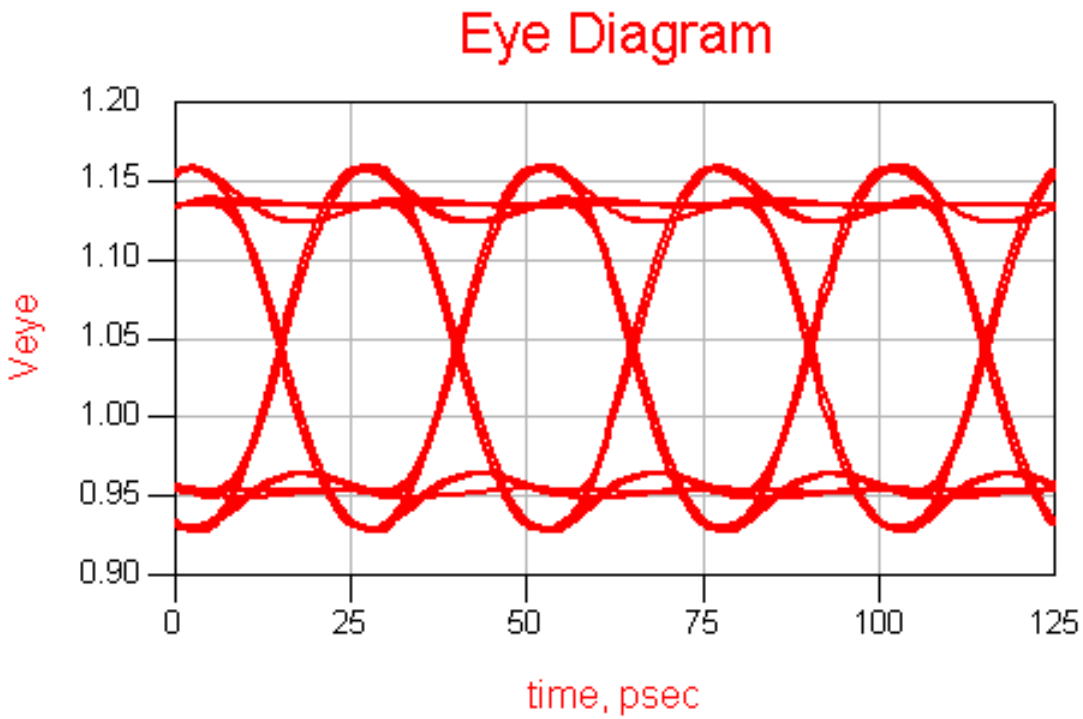
Model for 50 Gb/s photodiode

- Transient simulation
  - Model of source: photodiode with bondwire



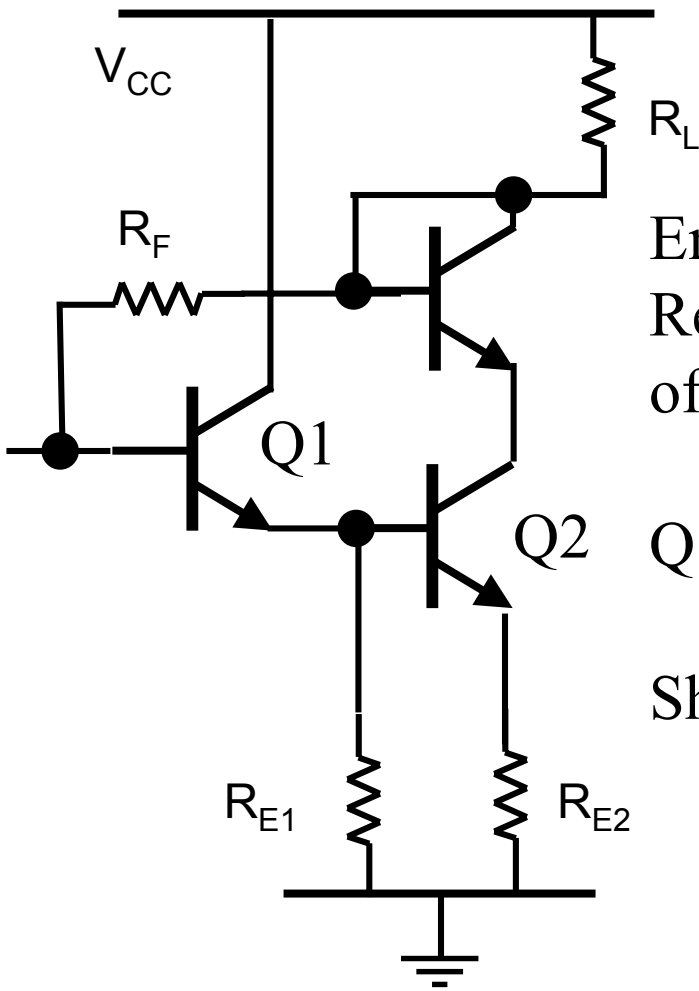
Ref: 6.1 H.-M. Rein

CE TIA 1: 40 Gb/s transient response



Well behaved transient response. 30 GHz bandwidth adequate

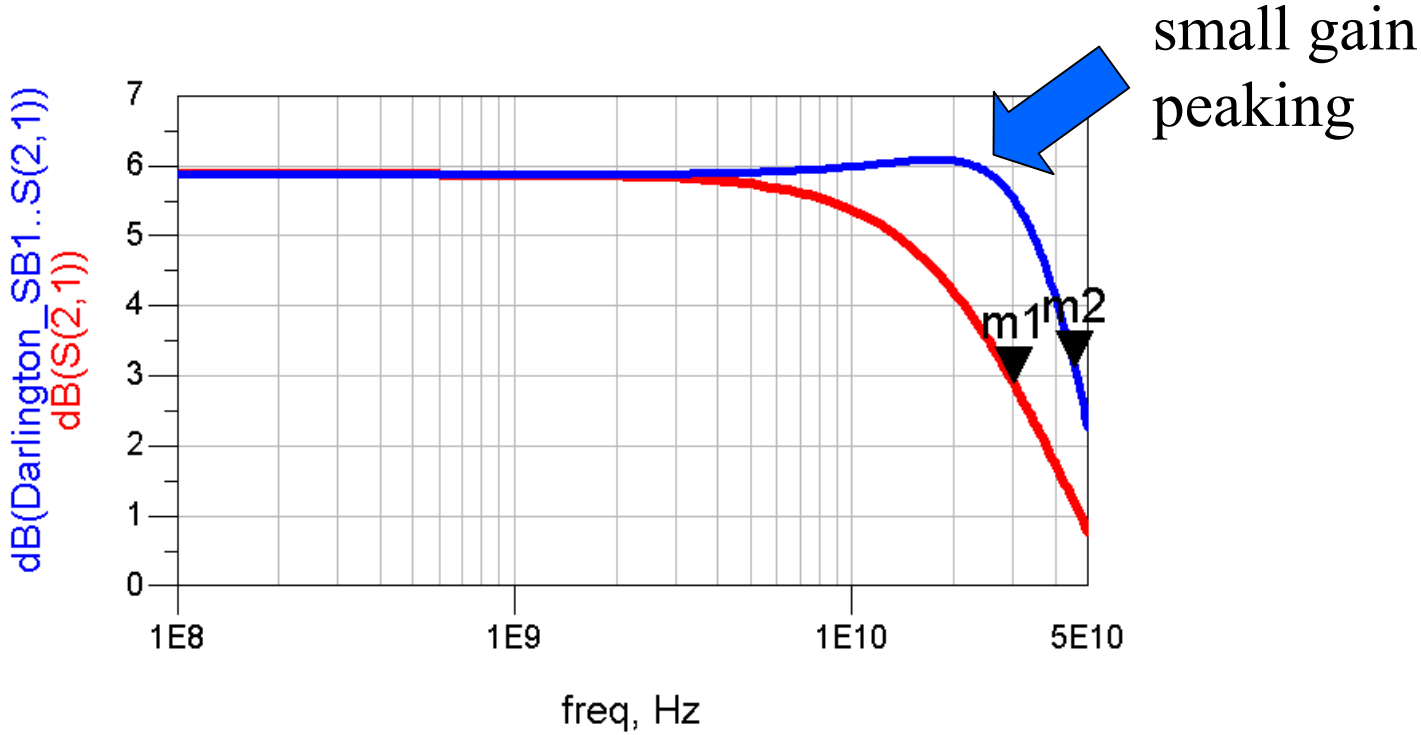
Improve BW: Darlington TIA 2



Emitter Follower first stage: Reduces time constant at base of Q2.

Q1 also decreases input capacitance

Shunt FB: R_F sets Z_{in} and Z_o



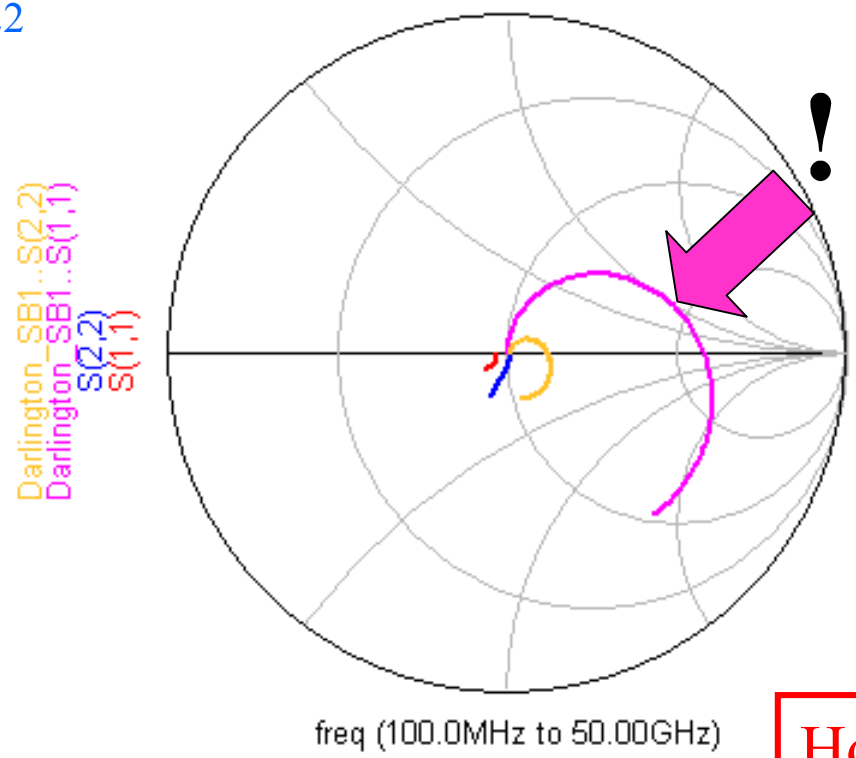
CE w. dual FB 30 GHz

Darlington w. dual FB 45 GHz

Big bandwidth improvement!

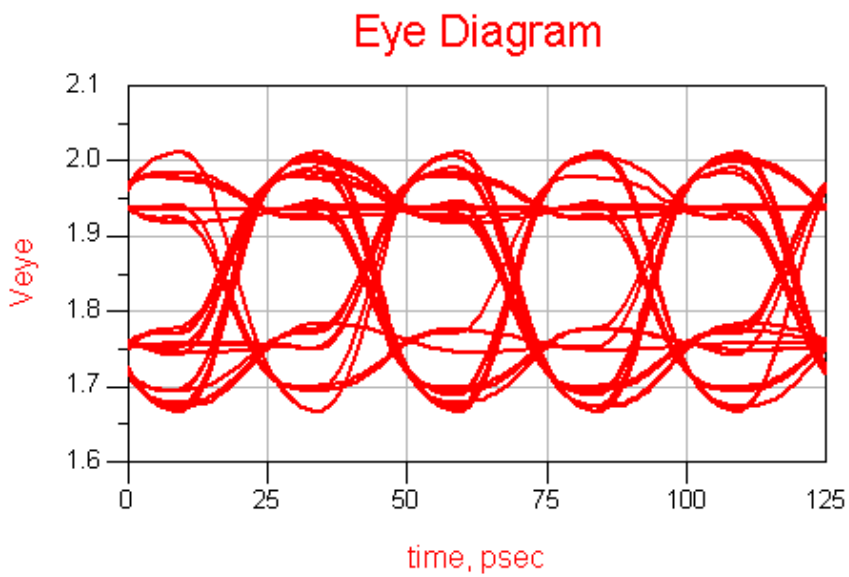
S_{11}
S_{22} CE TIA 1

We have exchanged bandwidth for S_{11}



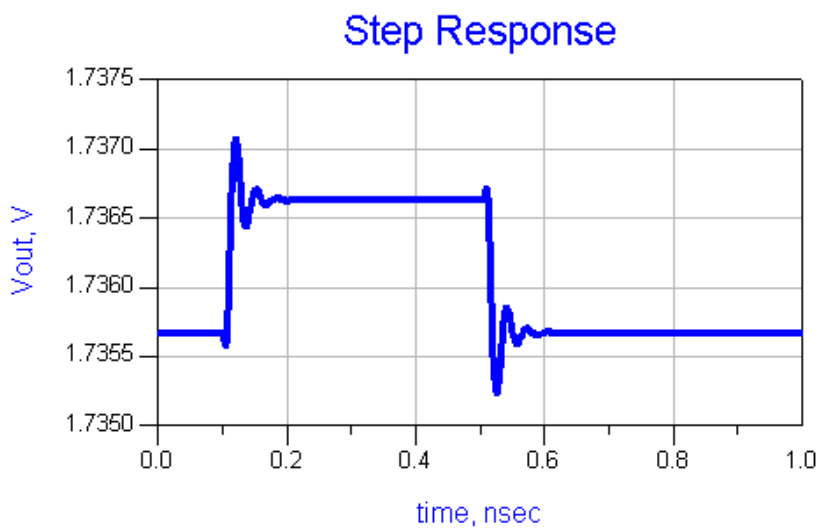
S_{11}
S_{22} Darlington TIA 2

How will this affect the transient response?



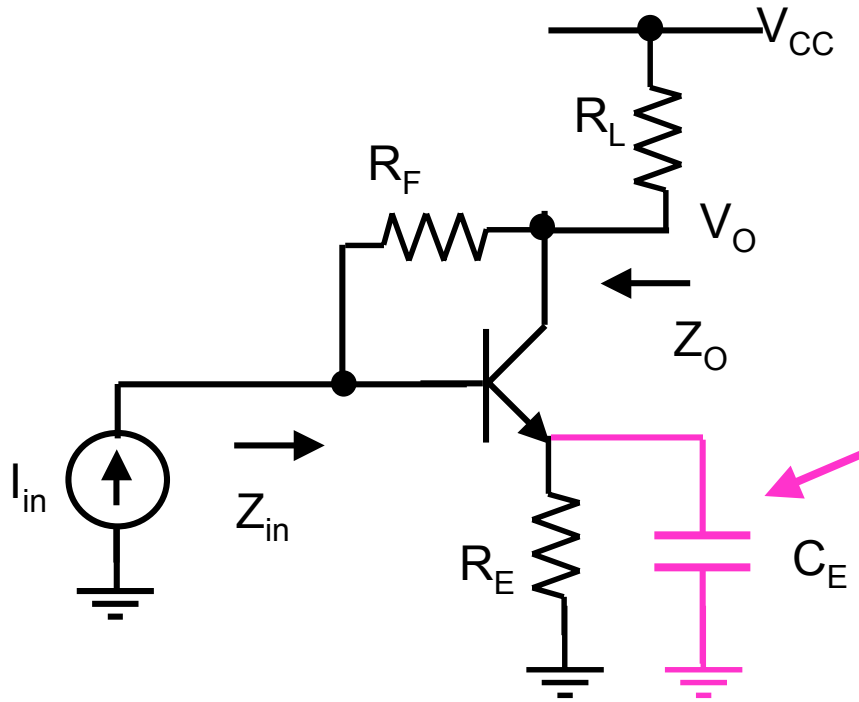
Darlington TIA

Transient response is poorer even though bandwidth has improved.



Ringing is significant

Emitter zero peaking: TIA 3



Another classic scheme for bandwidth, risetime enhancement

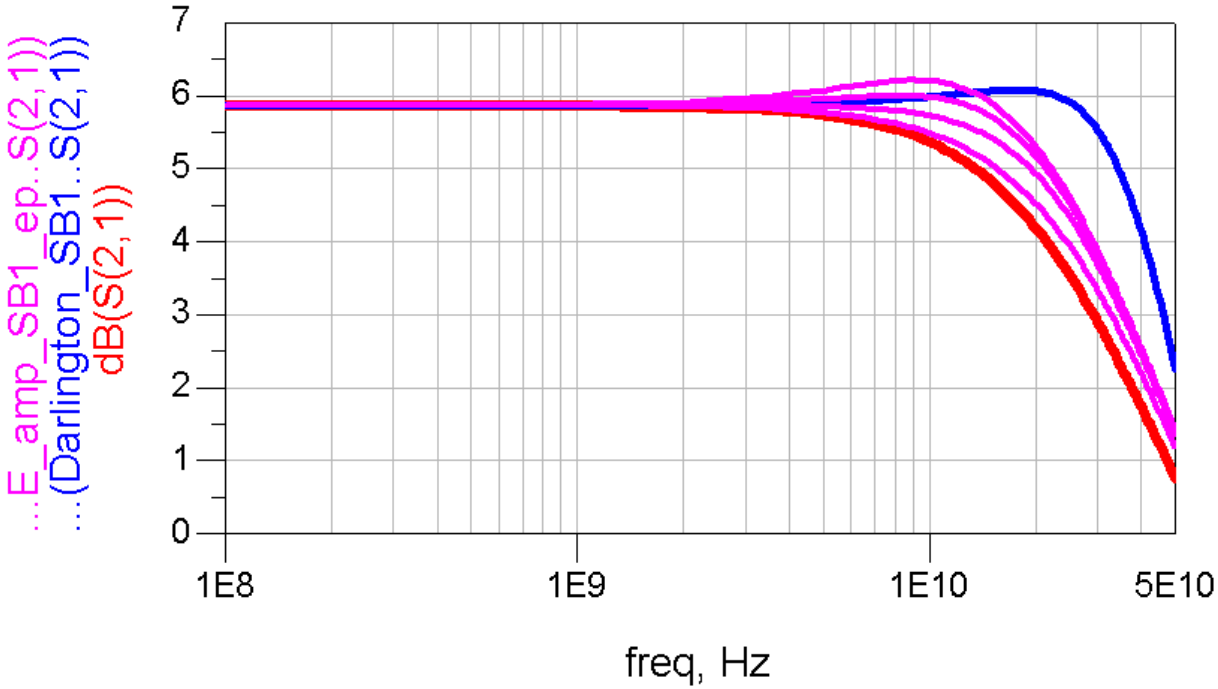
Zero added at $s = 1/R_E C_E$

Improve bandwidth/risetime by compensating for pole

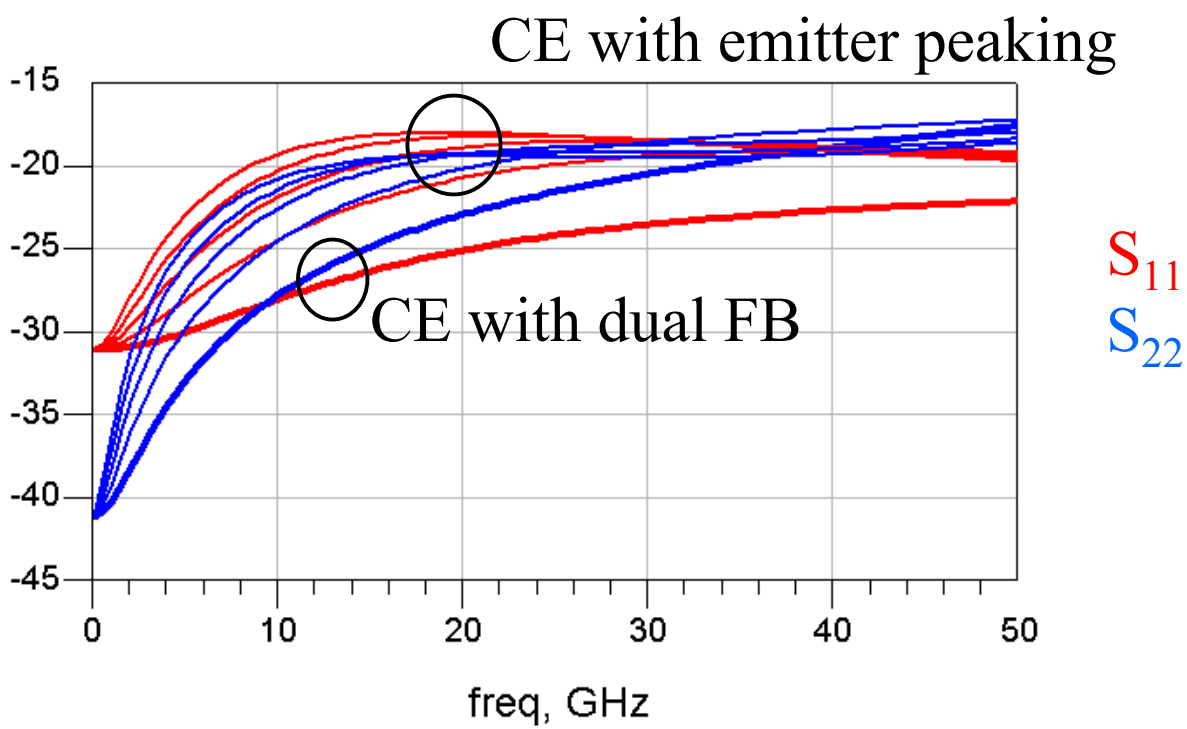
Works best when $p_2 >> p_1$

Ref. 4.11

CE with dual FB	30 GHz
Darlington	45 GHz
CE with emitter peaking	37 GHz



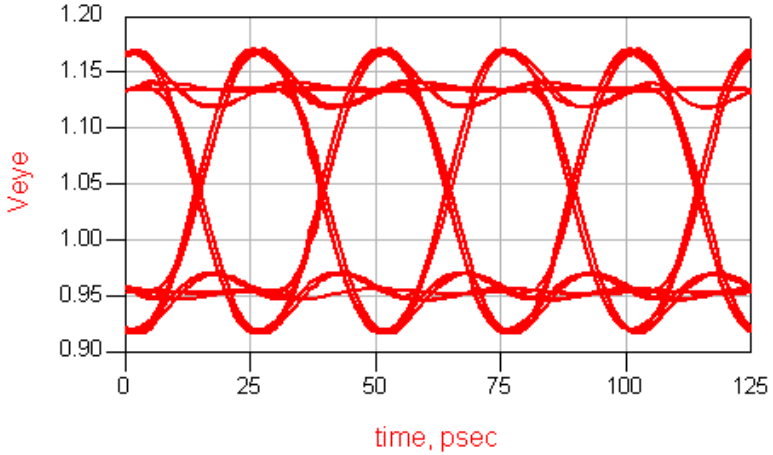
- Bandwidth improves with increasing CE
- Avoid excessive gain peaking



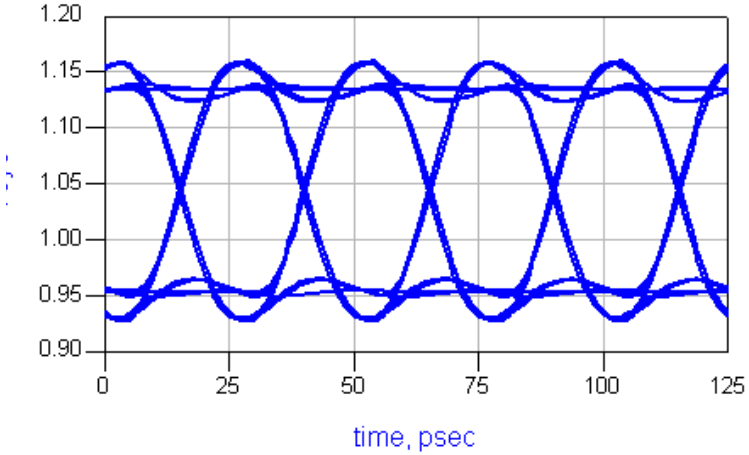
S_{11}, S_{22} degraded slightly by emitter peaking, BUT …

Transient response at 40 Gb/s is better than Darlington –
But, not as good as simple CE with FB

CE with emitter peaking
TIA 1



CE with dual FB
TIA 3



Preliminary conclusions:

- Each stage introduces extra poles
  - Can reduce phase margin due to higher order poles
- Careful design can improve BW, but
- 3 dB BW can be improved while degrading transient response
- Photodiode and interconnection model must be included

How do we analyze the TIA?

- Necessary conditions for the transfer function
  - Neglect higher than second-order terms
  - No complex-conjugate pole pairs
- Estimate pole frequencies with time constants

$$\frac{V_o(s)}{V_i(s)} = \frac{k}{1 + a_1 s + a_2 s^2}$$

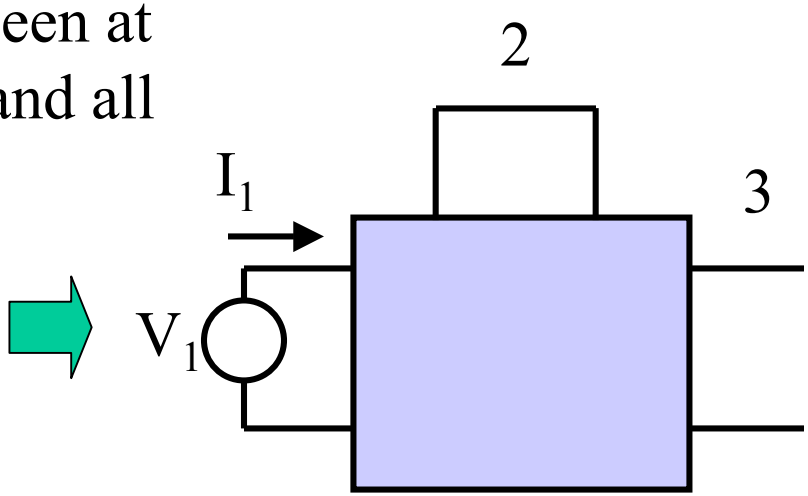
$$a_1 = \sum_{i=1}^{n} R_{ii}^{o} C_i$$ (as before – approximates dominant pole)

n = number of capacitors

a_2 can be estimated

Define R_{ii}^{j} as the resistance seen at port i when port j is shorted and all other ports open.

Here is an example of R_{11}^{2}



a_2 is the sum of products of short circuit and open circuit time constants associated with all possible pairs of capacitors. For a 3 capacitor network, a_2 is

$$a_2 = R_{11}^{o} C_1 R_{22}^{1} C_2 + R_{11}^{o} C_1 R_{33}^{1} C_3 + R_{22}^{o} C_2 R_{33}^{2} C_3$$

Ref. 6.2

Note that the first time constant is an OCTC that has already been calculated.
In addition, for any pair of capacitors, we can find an OCTC for one and a SCTC for the other. The order does not matter.

$$R_{ii}^{o} C_i R_{jj}^{i} C_j = R_{jj}^{o} C_j R_{ii}^{j} C_i$$

The second pole frequency can be estimated by the separated pole approximation:

$$\frac{V_o(s)}{V_i(s)} = \frac{k}{(1 + a_1 s)(1 + a_2 s / a_1)}$$

Here we assume that the a_3 and higher terms are small and $a_1 >> a_2/a_1$ – or use quadratic formula to find poles.

So, how does this help?

- If we know a_1 and a_2, we can estimate
  - Bandwidth
  - Gain peaking
  - Risetime
  - Overshoot and ringing frequency
  - And, most important, we can see what must be changed to avoid transient response problems!

Rewrite the denominator in a standard notation:

$$1 + a_1 s + a_2 s^2 = 1 + \frac{2\zeta s}{\omega_n} + \frac{s^2}{\omega_n}$$

Natural frequency: $\omega_n = a_2^{-1/2}$

Damping factor: $\zeta = \frac{a_1 \omega_n}{2}$

Good pulse response requires $\zeta > 1$. This prevents complex poles

BW, peaking, ringing, etc. all can be estimated from these 2 factors. (see appendix for a table)

Conclusions

- Both frequency and time domain responses can be improved by careful analysis and design
- Simulation complements, not replaces, analytical methods

For more information about Agilent EEsof EDA, visit:

www.agilent.com/find/eesof

Agilent Email Updates

www.agilent.com/find/emailupdates
Get the latest information on the products and applications you select.

Agilent Direct

www.agilent.com/find/agilentdirect
Quickly choose and use your test equipment solutions with confidence.

www.agilent.com

For more information on Agilent Technologies' products, applications or services, please contact your local Agilent office. The complete list is available at:

www.agilent.com/find/contactus

Americas

Canada	(877) 894-4414
Latin America	305 269 7500
United States	(800) 829-4444

Asia Pacific

Australia	1 800 629 485
China	800 810 0189
Hong Kong	800 938 693
India	1 800 112 929
Japan	0120 (421) 345
Korea	080 769 0800
Malaysia	1 800 888 848
Singapore	1 800 375 8100
Taiwan	0800 047 866
Thailand	1 800 226 008

Europe & Middle East

Austria	0820 87 44 11
Belgium	32 (0) 2 404 93 40
Denmark	45 70 13 15 15
Finland	358 (0) 10 855 2100
France	0825 010 700*
	*0.125 €/minute
Germany	01805 24 6333**
	**0.14 €/minute
Ireland	1890 924 204
Israel	972-3-9288-504/544
Italy	39 02 92 60 8484
Netherlands	31 (0) 20 547 2111
Spain	34 (91) 631 3300
Sweden	0200-88 22 55
Switzerland	0800 80 53 53
United Kingdom	44 (0) 118 9276201

Other European Countries:
www.agilent.com/find/contactus

Revised: March 27, 2008

Product specifications and descriptions in this document subject to change without notice.

© Agilent Technologies, Inc. 2008

Printed in USA, October 01, 2001
5989-9047EN

Agilent Technologies