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Overview on Satellite Tuner Single Chip Simulation with ADS

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Satellite Tuner Single Chip Simulation with ADS

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Abstract

This paper presents an innovative simulation methodology that has been set-up during the design of a STMicroelectronics System On Chip integrating an RF tuner, a demodulator and channel decoder for digital satellite applications. This new methodology is based on Advanced Design System (ADS) by Agilent Technologies which enables the simulation of systems described at different abstraction levels using several languages: Ptolemy, C, Matlab® for data flow, VHDL, Verilog for digital, behavioral models and transistor netlists for analog RF. This paper explains how such a simulation environment has been set-up and why it may reduce complex systems' time to market.

1. Introduction

Due to the integration of analog and RF functions on a single chip together with digital DSP cores, essentially for cost reduction and performance improvements, microelectronics companies face now system design problems. Whereas first silicon success is a reality for pure digital designs, the integration of RF blocks controlled by digital part through several feedback loops requires today several silicon runs before achieving all specifications. Some of the re-designs could be easily avoided if full chip simulation were performed systematically. Up to recently, while many simulation tools were available for each design domain (System, Digital and Analog RF), no tool was able to deal practically with all the three domains, especially for RF applications. This paper shows why ADS design platform [1] could boost the application of the Top/Down and Bottom/Up design methodologies for RF System On Chips. This demonstration is based on the simulation of a new generation of single chip satellite tuner STV0399 [2] generating directly digital MPEG2 stream from the RF input signal.

2. System Description

This circuit consists of an RF tuner that directly converts RF signal to base-band signal (Zero-IF Tuner), a multi-standard QPSK, 8-PSK and BPSK demodulator working over a wide symbol frequency range (from 1 to 45 MBauds), and a Forward Error Correction (FEC) system for DVB and DirecTV standards. It is intended for use in digital satellite television applications and is made in standard 0.18 μ m CMOS technology allowing low power consumption (0.7watt).

It has been designed to shift the pre-selected satellite IF band from 950 MHz to 2150 MHz (no external filter) into two quadrature base-band signals by mixing the amplified RF signal with two orthogonal reference oscillator signals (no external tank) as shown in Fig.1.

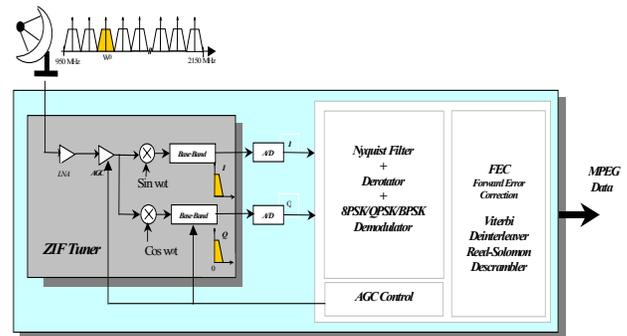


Figure1 : Block diagram of front-end

RF Input Stage: The RF input stage consists of a low noise amplifier (LNA), a switchable attenuator followed by a phase splitter and a first AGC stage.

The LNA is defined to improve the noise figure of the receiver and to provide reverse isolation from the local oscillator.

Optimum SNR is guaranteed by 2 AGC stages: the first stage (AGC0) lets optimize the dynamic range at the mixer, while the second (AGC1) operates in the base-band stage.

AGC0 calibration is carried out just after channel switching by measuring the power at mixer input and performs the trade-off between highest input power and mixer linear operating range. The AGC0 is set-up during channel change and its operating point is frozen during the demodulation.

Mixer and Local Oscillator: The local oscillator signal is generated internally using two PLL in the band from 915 to 2150MHz. A double balanced mixer is used to improve local oscillator isolation

Base-band Stages: After the mixer, a set of two low pass filters is provided in order to prevent folding of unwanted signals during ADC sampling.

ADC Converters: The signals are digitized via integrated dual 6-bit analog to digital converters, interpolated and digitally filtered by a Nyquist root filter.

Digital Stage: The digital signal then passes through the digital carrier loop fitted with an on-chip derotator and tracking loop, lock detector, digital timing recovery. Note that the base-band AGC1 is controlled by measuring the RMS value of I and Q signals after Nyquist filter and by comparing them with a programmable value. The integrated error signal is then applied to a multiplier on each I and Q path.

3. Design Methodology

Several design teams are involved for the design of such systems for system architecture, analog RF and digital design. Each team using dedicated simulation tools that are not always inter-operable, many design errors may occur at the interface. In order to improve design quality, a common design platform in which each team can plug-in their design tools is required. The following describes an interesting solution using ADS environment.

3.1 System Level Design

System architecture definition and block specification optimization have to be performed by powerful signal processing tools such as Matlab®/Simulink® [3], SPW® [4], COSSAP® [5], Agilent Ptolemy [1] or just C programs.

The main advantage of Agilent Ptolemy over the others is the richness of its communication model libraries available for the newest communication standards (UMTS, WLAN, HyperLAN, WCDMA, DTV...). These libraries let simulate easily emission or reception chains using appropriate modulators or demodulators and evaluate the impact of block non-linearities and noise on the constellations, EVM

and BER. The RF front-end architecture of the STV0399 has been first studied and optimized in this way.

Moreover, Matlab® or C models already developed by digital teams can be easily called from Agilent Ptolemy by using special components written in Ptolemy language. It is even possible to launch Simulink, although it is not efficient. Better simulation performances have been obtained by translating Simulink schematics into Agilent Ptolemy. This was the case for the ADC block.

3.2 Co-simulation with a digital simulator

VHDL or Verilog code of the digital part is tested using stimuli defined at system level. Agilent Ptolemy is able to generate these stimuli but also to co-simulate with digital simulators (ModelSim™ [7] and Verilog-XL [8]). Digital models are simply encapsulated by a Ptolemy models. Co-simulation is required to test feedback loops such as AGC control loops after channel switching. It allows also verifying FEC capabilities with oscillator phase noise and multiple channels.

The figure 2 shows simulation results for a symbol rate of 6.25Mbauds for 30000 symbols and with phase noise. The “CN_estimator” curve is a digital output computed by the circuit using correlation tables and is a SNR indicator. The “agc2” wave is also a digital output (displayed as integer) that tunes the AGC0. This signal increases up to the maximum due to a low power input (80dBm). Finally the QPSK constellation is plotted when the “CN_estimator” signal becomes constant.

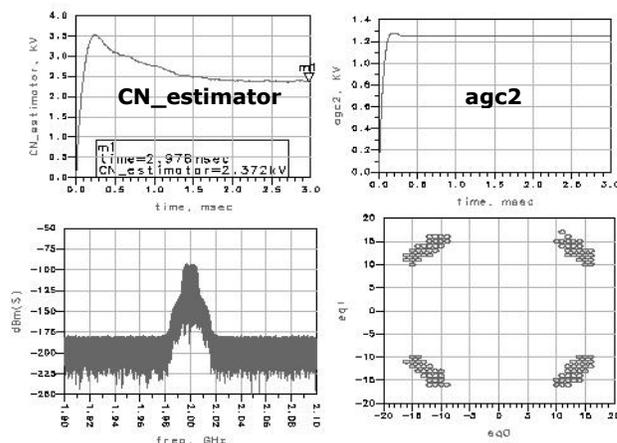


Figure 2: System co-simulation results

3.3 Co-simulation with a RFIC simulator

In order to accurately assess circuit performances, some parts of the system level data flow description may be replaced by more accurate descriptions at electrical level. In order to close the gap that traditionally exists between system and electrical levels, Agilent Ptolemy is able to co-simulate with ADS Circuit Envelope simulator [1] that combines time and frequency techniques to deal with digitally modulated high frequency signals.

While RF input signal, defined by its carrier value, is converted automatically from data-flow to electrical domain, output envelope selectors must be added at I and Q outputs for carrier selection. Digital inputs must also be converted from bit to real values.

However, due to the complexity of the RF front-end part (3000 MOS), simulation using a full transistor description is not suitable for AGC control loop analysis or BER estimation. To tackle this limitation, analog behavioral models of the amplifiers and mixers, generated by S-parameters and harmonic balance transistor level simulations, have been used instead. These models can take into account S parameters and noise figure variations versus frequency and gain compression with phase shift versus input power. These table-based models can be combined to create more complex structural models, as for the AGC which gain is digitally programmable.

The following table gives a comparison of simulation times for the system with the AGC0 described at different levels, for 7000 symbols and on a SunUltra10 workstation.

Description Level	System Level	Behavioral Level AGC0	Transistor Level AGC0
CPU time	2 811s	4 389s	81 400s
Ratio	1	1.6	29

Note that transistor schematics have been captured in Cadence Design Framework and netlisted by ADS RFIC Dynamic Link [1].

4. Conclusion

This paper has described how ADS design platform has been used successfully for the simulation of a complete single-chip front-end for digital satellite using several description levels: system, digital VHDL and electrical behavioral or transistor levels. The ADS simulation results have been compared to measurements with good correlations. Therefore, ADS is promised to become

STMicroelectronics's golden simulation environment for RF System On Chips.

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