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Overview on Radio-Frequency Circuits Integration using CMOS SOI 0.25 μ m Technology

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Radio-Frequency Circuits Integration Using CMOS SOI 0.25 μ m Technology

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Abstract

Interest in SOI technology has been increased due to recent progress in modeling parasitic effects needed for analog IC design. In this paper a brief overview of the SOI technology is done. A user compiled model built for ADS is then described before the analysis of 2 RF designs: a wideband Low Noise Amplifier (300MHz-900MHz with more than 10dB gain and 5dBm IIP3) and an antenna switch (with 0.5dB insertion loss and more than 50dB isolation) on the same bandwidth.

1. Introduction

There are already few years that Silicon On Insulator (SOI) technology has been investigated in. Due to couple of advantages, such as the junction capacitance reduction which allows faster switching of SOI MOS, better Soft Error Rate (SER) [1],[2],[3],[4], better density of integration due to latch-up immunity, SOI has been identified to be a good competitor of CMOS technology in digital and SRAM design. Nevertheless, it is only recently, guided by other advantages (for passive components) and the aim of mixed chip development, that investigations in Radio-Frequency (RF) design began. In this paper, a brief overview of the SOI technology is done. After a presentation of the LETISOIRF model, developed for the Agilent Advanced Design Systems tool (ADS), two different RF designs will be analyzed: a wideband LNA (300MHz-900MHz with more than 10dB gain) and an antenna switch.

2. Technology presentation

Silicon On Insulator (SOI), the name come from the insertion of the insulation layer (the BOX: Buried Oxide layer) beneath the devices. In partially depleted technology, the MOS structure does not change much and technological process is exactly the same just the manufacturing process for SOI wafer is different [5].

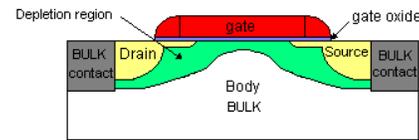


Figure 1: Bulk MOS cross section

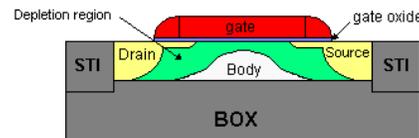


Figure 2: partially depleted SOI MOS cross section

The SOI MOS cross section below involves a couple of advantages such as the junction capacitance reduction due to the diminution of the junction surface. Since these parasitic capacitances impact greatly on the device speed performances, SOI devices have better high frequency performances. The latch-up structure of CMOS technology is avoided due to the BOX [5]. This improves significantly integration and packing density. The isolation of the active body from the substrate improves the SER as well, at small dimension, indeed impact ionization in the substrate can no more affect the body and then the channel region [1],[2],[3],[4]. An output conductance g_{ds} reduction can be notice due to the absence of highly doped buried layer in SOI MOSFET. This may be really interesting for switch design, especially for high isolation. Moreover, availability of High Resistivity Substrate (HRS SOI) implies possibility to reduce cross-talk through the substrate in mixed-mode ICs and to reduce substrate losses. It allows as well higher Q passive components manufacturing. SOI technology has also proved better performances for low voltage an low power applications.

Nevertheless, SOI technology has some undesirable effects with which designers have to manage. The most well know are the floating body effects [6]. These include 2 effects: the bipolar effect which is due to the presence of a parallel bipolar transistor which can turn on under certain charge accumulation condition in the body; and the Kink effect which results of a charge accumulation in the body due to impact ionization. This effect is more noticeable at $V_{ds}=V_{dd}/2$ [5] indeed this point is an impact ionization peak. However these effects can be controlled thanks to a body contact or body tie (body link to the source) which allow to fix the body potential.

3. ADS model implementation

In order to establish potentiality of SOI for RF design, a user compiled model has been developed for ADS using C language. This model characterizes a $0.25\mu\text{m}$ partially depleted technology from DC up to 10GHz.

This RF model is composed of the intrinsic and extrinsic parts. Regarding the intrinsic part, several effects have been implemented [9]:

- Accurate description of threshold voltage
- Short and narrow channel effects
- Gate-controlled recombination and generation
- Drain induced barrier lowering effect
- Impact ionization current
- Parasitic bipolar transistor
- Non-quasi-static effects

And the extrinsic part takes into account:

- Access parasitic resistances
- Gate resistance and gate inductance
- A complete substrate network
- Parasitic capacitances due to the use of multifinger architectures

Figure 3 illustrates a comparison between the simulated S-parameters using the LETISOIRF model and the measured S-parameters of a n-channel $0.25\mu\text{m}$ SOI MOSFET with the floating body.

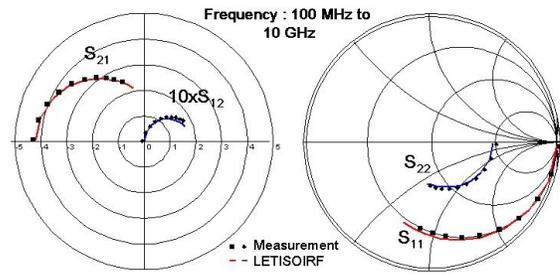


Figure 3: S-parameters of $0.25\mu\text{m}$ SOI MOSFET

The RF model allows to predict accurately the SOI MOSFET behavior up to 10 GHz. Moreover, for analog simulation, low and high frequency noise model has also been integrated in this model. This noise model is based on the complete description of all noise sources, such as the channel noise, impact ionization noise, junction noise, thermal noise in the access resistances. Figure 4 shows an example of a low frequency noise modeling.

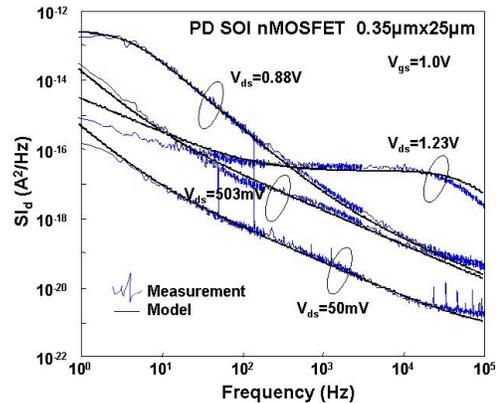


Figure 4: LF noise of a $0.35\mu\text{m}$ SOI nMOSFET with the floating body

4. LNA conception methodology

A very wideband Low Noise Amplifier (LNA) has been implemented (figure 5). Specifications were the following: 350MHz to 900MHz band divided in 2 parts the first 350MHz to 500MHz and the second 750MHz to 900MHz, 10dB gain on the overall band, 5dB IIP3, a noise figure as low as possible, and a 50Ω matching at both input and output. No specification was given regarding consumption. The whole design is based on these

priorities including the desire of a fully integrated system.

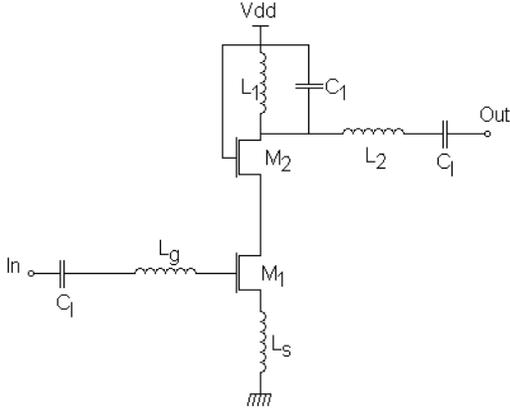


Figure 5: LNA design

A. Input matching

In order to obtain a 10dB gain on the overall bandwidth with a 50Ω input impedance, a Gm of 150mS is needed. Because of the very large bandwidth, a poor input quality factor (Qin) has to be performed with this input architecture. Therefore Qin is chosen equal to 0.8.

$$Gm = gm \cdot Qin = \frac{1}{L_s \cdot \omega_0} \quad (1)$$

From (1), equation of total LNA gain, the degeneration inductor value, Ls, is imposed to 0.9nH (close to bonding inductor). The input impedance of this LNA (Zin) is needed to be 50Ω. It is given from the following expression [7]:

$$Zin = j(L_s + L_g)\omega + \frac{1}{jC_{gs}\omega} + L_s\omega_t \quad (2)$$

Where ω_t is gm divided by C_{gs} . Therefore, the product L_s with ω_t has to be closed to 50Ω. Since L_s and gm are already imposed by all previous considerations, C_{gs} is now fixed and then W_1 , width of MOS 1, as well ($W_1=600\mu\text{m}$). L_g is used to set an appropriate resonance frequency. All these considerations lead the design to exhibit an S_{11} parameter less or equal to -6dB on the overall bandwidth (350MHz to 900MHz) as shown on figure 6.



Figure 6: Input matching S_{11}

Nevertheless, the input matching network is responsible of the LNA consumption. Up to now, no consideration has been done regarding this point (remember that it was not the point in this design).

$$I_{consumption} = \frac{L}{Q^2 L_s^2 \omega_0^2 \mu_0 C_{ox} W} \quad (3)$$

From (3) an $I_{consumption}$ closes to 50mA can be reach. Therefore, for low consumption design, other trade-offs have to be done or a better architecture may be chosen.

B. Noise factor

The Noise factor of this kind of LNA may be expressed as following:

$$F = 1 + \frac{R_l}{R_s} + \gamma \cdot \chi \cdot g_{ds} R_s \left(\frac{\omega_0}{\omega_t} \right)^2 \quad (4)$$

Where χ is a function of both technology and Qin, γ a noise factor. The cascode MOS does not contribute significantly in the noise factor.

C. Output matching

The output matching network is a RLC network. The use of 2 inductors and capacitors provides 2 different resonance frequencies (one at 400MHz and the second at 850MHz). This allows a better matching on each bandwidth.

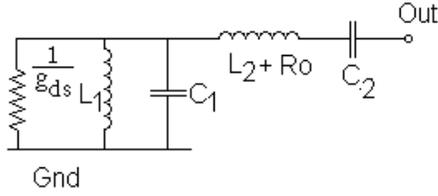


Figure 7 : equivalent output matching network

The equivalent output matching network of the LNA, shown on figure 7, provides an output impedance (Z_{out}) as described below:

$$\text{Re}\{Z_{out}\} = \frac{L_1^2 \cdot R_{ds} \cdot \omega^2}{R_{ds}^2 (1 - L_1 \cdot C_1 \cdot \omega^2)^2 + L_1 \omega^2} + R_0$$

$$\text{Im}\{Z_{out}\} = \frac{L_1 \cdot R_{ds} \cdot \omega (1 - L_1 \cdot C_1 \cdot \omega^2)}{R_{ds}^2 (1 - L_1 \cdot C_1 \cdot \omega^2)^2 + L_1 \omega^2} + L_2 \omega - \frac{1}{C_2 \omega}$$

Where $\text{Re}\{Z_{out}\}$ is the real part of the output impedance and $\text{Im}\{Z_{out}\}$ represents the imaginary one. Therefore L_1 and C_1 are chosen to provide a real part close to 50Ω around both frequencies 400MHz and 850MHz. The values of L_2 and C_2 are determined to cancel the imaginary part. There are 3 frequencies at which $\text{Im}\{Z_{out}\}$ equals zero:

$$\left\{ \begin{array}{l} \omega_1 = \frac{1}{\sqrt{L_1 C_1}} \\ \omega_2 = \sqrt{\frac{A + \sqrt{A^2 - 4L_1 C_1 L_2 C_2}}{2L_1 C_1 L_2 C_2}} \\ \omega_3 = \sqrt{\frac{A + \sqrt{A^2 + 4L_1 C_1 L_2 C_2}}{2L_1 C_1 L_2 C_2}} \end{array} \right. \quad (5)$$

where $A = L_2 C_2 + L_1 C_1 + L_1 C_2$

From equations (5), ω_1 is imposed because L_1 and C_1 are already chosen. Then a system (S) of 2 equations with 2 variables has to be solved to find values for L_2 and C_2 .

$$(S) \left\{ \begin{array}{l} \omega_2 = 400\text{MHz} \times 2\pi \\ \omega_3 = 850\text{MHz} \times 2\pi \end{array} \right.$$

Next table shows a summary of implemented impedances:

L_1	10nH
L_2	15nH
C_1	7pF
C_2	5pF

table 1 : summary of impedances implemented

Figure 8 is a representation of the output matching. On both band the matching is good enough:



Figure 8 : Output matching S_{22}

D. Simulation results

All simulation results are resumed in the next table. It has to be notice than the overall design performance has been check with different bonding values ($0 < L_{bonding} < 1.5\text{nH}$).

Bandwidth	350-500MHz	750-900MHz
Technology	SOI 0.25 μm	
Gain	> 10 dB on the overall bandwidth	
Reverse Gain	< 40 dB on the overall bandwidth	
S_{11}	< -6dB	< -8dB
S_{22}	< -4dB	< -5dB
NF (dB)	3.7	3.2
IIP3 (dBm)	5.36	

table 2: simulation results

5. Switch conception topology

A. Switch consideration

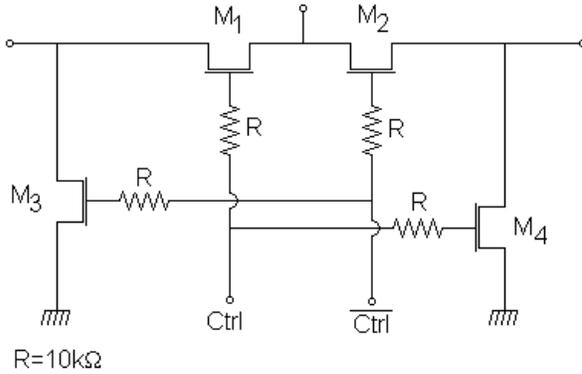


Figure 9: Switch design

The switch (figure 9) has a classical switch structure. M1 and M2 are the basic MOS switches. Their optimization is done for a very good insertion loss considering an acceptable isolation trade-off ($W = 220\mu\text{m}$). M3 and M4 are used to improve isolation by coupling the off signal to ground. Therefore these MOS are optimized for isolation

Technology	SOI $0.25\mu\text{m}$	Bulk $0.5\mu\text{m}$ [8]
Isolation	-50dB	-40.1dB
Insertion loss	-0.49dB	-0.97dB
IIP3	36dBm	33.3dBm

since they should not have too much leakage to the ground when they are off ($W = 150\mu\text{m}$)[8]. Gate bias resistances R have been added in order to improve dc bias isolation ($R=10\text{k}\Omega$).

SOI is particularly interesting for this application since parasitic junction capacitors are lower than the one of Bulk MOS technology. Indeed for an equal C_{ds} in both technology (therefore an equal isolation), the SOI MOS may have a bigger W allowing better insertion loss. Moreover no body contact or body tied should be used in this application because the lower C_{ds} is, the better the isolation will be. A tied or contact body will increase C_{ds} as shown on figure 10&11.

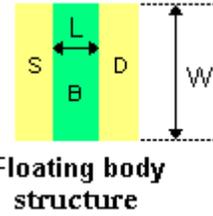


Figure 10: floating body SOI MOS

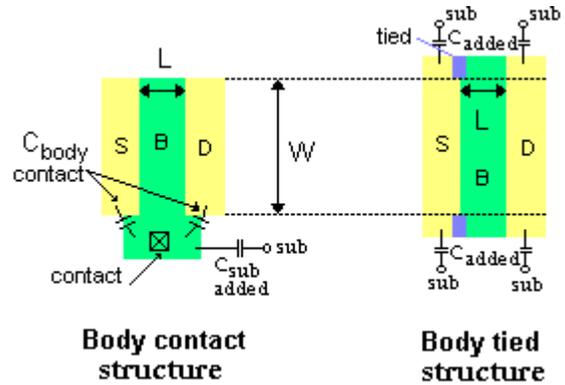


Figure 11: added capacitances due to tied or contact

B. Simulation results

As shown in table 3, the switch performances are quite good.

table 3 : switch simulation results

6. Conclusion

In this paper, two RF designs performed successfully with $0.25\mu\text{m}$ SOI technology have been introduced. Regarding the LNA design, no real advantage has been found using a standard substrate resistivity but more investigations have to be done. Nevertheless, SOI has proved its efficiency in switch designs improving isolation and insertion loss. Therefore promising performances may be expected for mixer designs. Since trend is to increase operating frequency, SOI technology could show more advantages.

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applications in 0.12 μ m SOI technology. He is currently working as RF designer in the CEA-LETI laboratory where he designs RF blocks using SOI technology.

Olivier Rozeau received the M.S. degree in electrical engineering from ENSPG (Ecole Nationale Supérieure de Physique de Grenoble, France) in 1997 and a Ph.D. degree about passive and active device characterization and modeling in SOI technology in 2000. He is currently working as modeling engineer in the CEA-LETI laboratory where he develops RF MOS transistor models for SOI technology.

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Revised: March 27, 2008

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Printed in USA, March 01, 2002
5989-9080EN