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Presentation on High Efficiency RF Power Amplifiers using Bandpass DSM

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High Efficiency RF Power Amplifiers Using Bandpass Delta-Sigma Modulators

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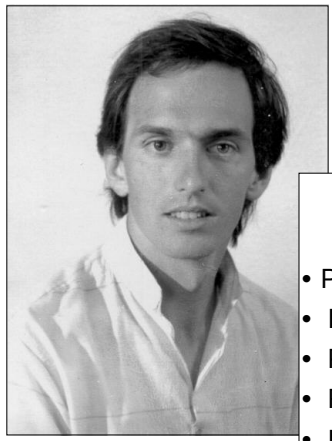

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- Professor: Simon Fraser University
- Focus on integrated RF/DSP applications
- PhD, 1988, Carleton University, Canada
- RF/Microwave communications systems
- Expert in High Efficiency RF Power Amplifiers

Sigma-Delta Power Amp

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Shawn P. Stapleton is a Professor at Simon Fraser University. He research focuses on integrated RF/DSP applications for Wireless Communications. He received his BEng in 1982, MEng in 1984 and PhD in 1988 from Carleton University, Canada, where his studies were focused on RF/Microwave Communications. Before joining Simon Fraser University, Shawn worked on a wide variety of projects including: multi-rate digital signal processing, RF/Microwave communications systems, and Adaptive Array Antennas. While at Simon Fraser University he developed a number of Adaptive Linearization techniques ranging from Feedforward, Active Biasing, Work Function Predistortion to Digital Baseband Predistorters. He has published numerous technical papers on Linearization and has given many presentations at various companies on the subject. He continues to research the field of utilizing DSP techniques to produce Power Efficient Amplifiers for Mobile Communications applications..

Shawn P. Stapleton is a registered Professional Engineer in the province of British Columbia.

High-Efficiency Switching Mode Power Amplifiers Using Bandpass Delta-Sigma Modulators

1 Introduction

2 Bandpass Delta-Sigma Modulator

3 Amplifier Circuit and Bandpass LC Filter

4 Simulation Schematics and Results

5 Conclusion

Sigma-Delta Power Amp

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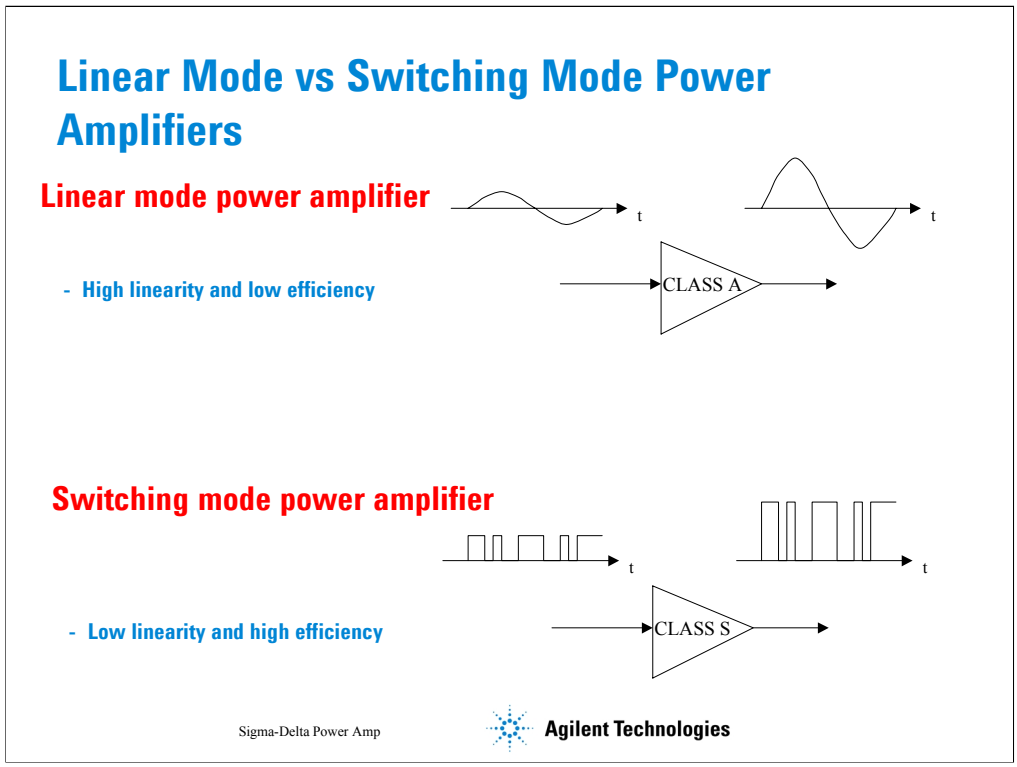
Abstract – In this seminar we investigate the application of bandpass Delta-Sigma modulators (DSM) to switching mode power amplifiers (SMPA) for cellular applications. A double-loop, second-order lowpass DSM is used as prototype to design a bandpass DSM using the lowpass-to-bandpass transformation . The quantization noise produced at the bandpass DSM output has a spectrum valley centered on digital angular frequency of 1/4 the sampling frequency. The binary digital output signal of the bandpass DSM is subsequently fed into a pre-amplifier circuit to produce a continuous-time pulse signal which drives a SMPA. A switching mode (also called class-S) power amplifier system consists of three parts, i.e.

- Signal converter which converts a RF input signal to a two-level square-wave signal

-Amplifier circuit which amplifies the two-level signal which increases the output power

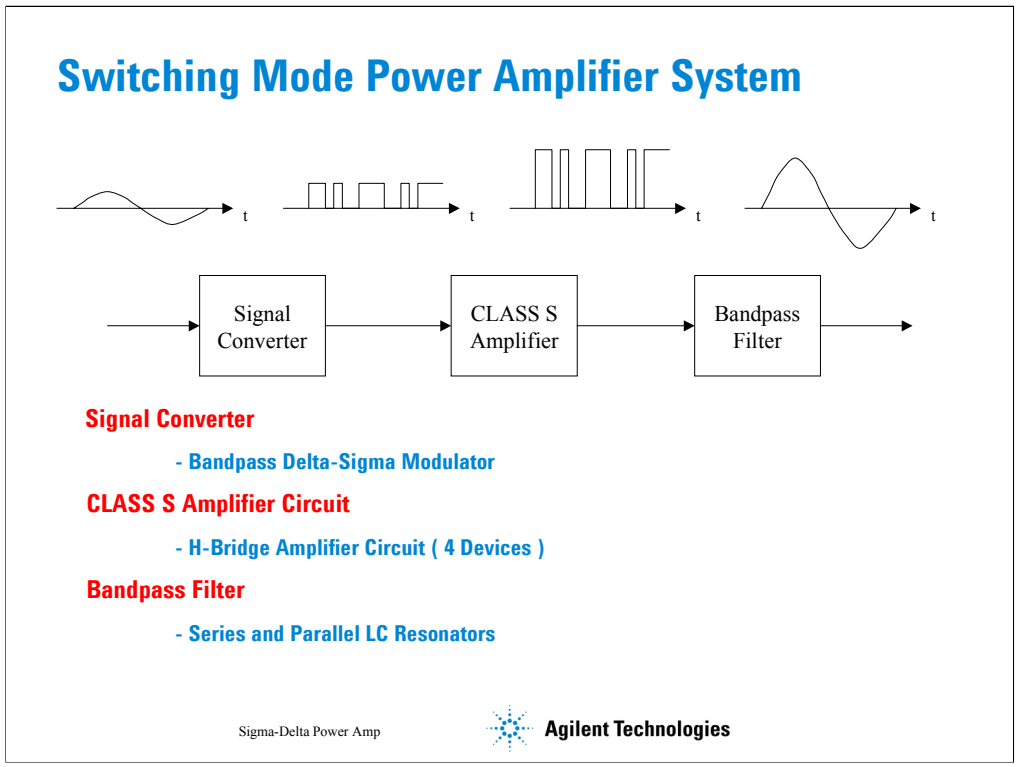
-Bandpass filter which extracts the useful signal from the output signal of the amplifier

In our investigation a bandpass delta-sigma modulator serves as signal converter, and an H-bridge amplifier circuit with four transistors and a Butterworth/Chebyshev bandpass LC filters are used.



Existing power amplifiers for AMPS and CDMA wireless applications commonly use class-A biased transistors combined with feed-forward linearization techniques. These designs produce medium to high output powers with low inter-modulation products. However, their DC to RF power conversion efficiency is low. In solar powered wireless repeater applications, DC to RF efficiencies of over 30% are required.

To improve DC to RF amplifier efficiency several SMPAs have been proposed. The transistors of a SMPA are operating either in the cut-off or in the triode region, requiring no quiescent current. Normally, a pulse-width-modulated signal produced by a pre-amplifier circuit is employed to drive the transistors of the amplifier.



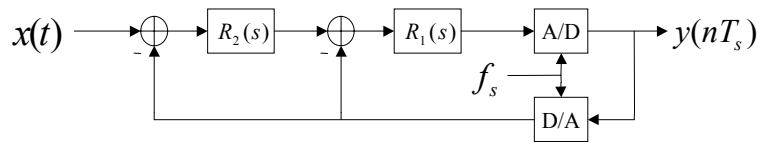
A bandpass Delta Sigma Modulator (DSM) is used to convert the RF input signal into a binary digital signal.

A bandpass delta-sigma modulator converts an analogue RF input signal to a two-level pulse-density modulated signal. Generally it is a non-linear feedback system. The non-linearity is due to the quantization at the output. The output of the bandpass DSM is fed into a pre-amplifier circuit to produce a continuous-time pulse-width modulated signal, which subsequently drives the transistors in an H-bridge amplifier circuit. A bandpass filter is required to attenuate the out-of-band quantization noise and harmonics.

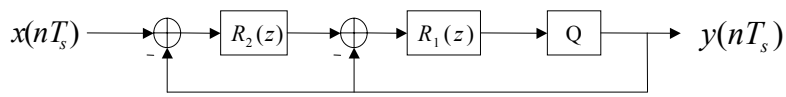
There are many bandpass delta-sigma modulator structures investigated. The structure chosen in our investigation is called a double-loop bandpass (4th-order) delta-sigma modulator.

Bandpass Delta-Sigma Modulator

Double-Loop BPDSM Structure



Equivalent Discrete-time Model



$$R_1(z) = \frac{-2z^{-2}}{1+z^{-2}} \qquad R_2(z) = \frac{-0.5z^{-2}}{1+z^{-2}}$$

$$z_{\infty 1,2} = e^{\pm j\frac{\pi}{2}} \qquad f_\infty = 800\ \text{MHz} \qquad f_s = 4f_\infty = 3.2\,\text{GHz}$$

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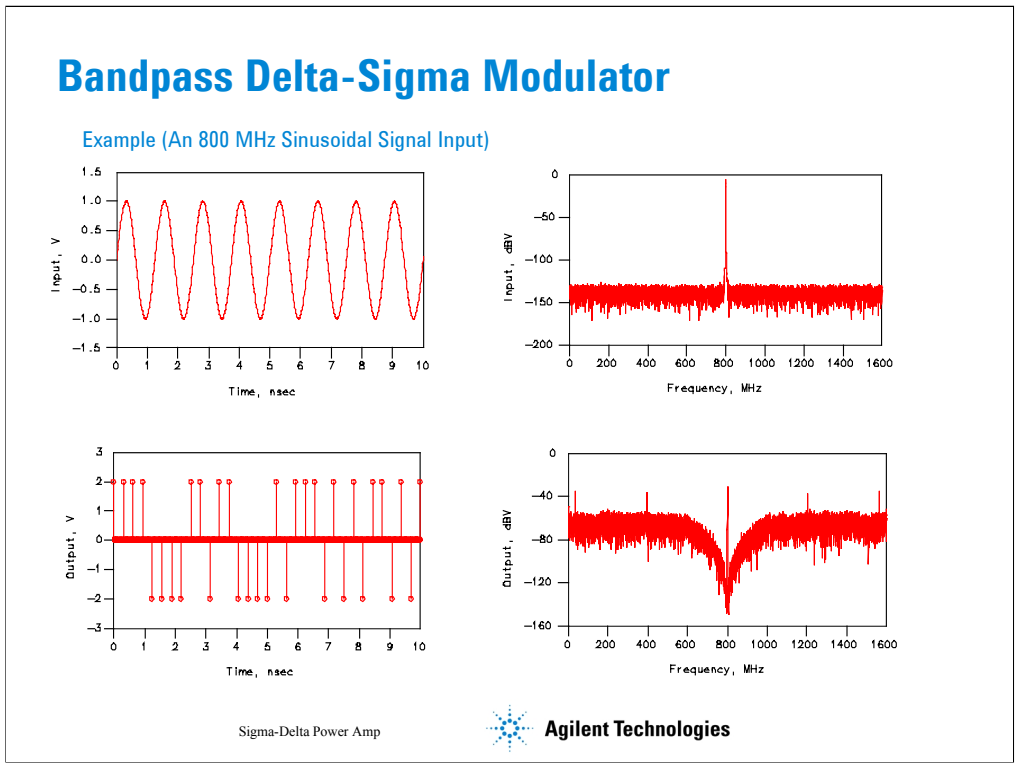
In DSM high oversampling rates are necessary. A lowpass DSM requires a sampling rate much greater than the highest frequency of interest present in the input signal. For a bandpass DSM, however, a lower sampling rate can be used as long as it is much greater than the bandwidth of interest present in the input signal. One method of designing a bandpass DSM is to start with a suitable lowpass DSM prototype and employ a lowpass-to-bandpass frequency transformation.

Its noise-transfer-function is then centered at the bandpass frequency . If we oversample by a factor of 4 , then the sampling rate of the bandpass DSM should be 3.2 GHz for an input signal with a center frequency of 800 MHz.

In order to create the pulse width modulated signal, a 1 bit A/D and D/A is required. This also simplifies the development of the DSM when using analog circuitry.



To demonstrate the operation of the bandpass delta sigma modulator a 800 MHz sinusiodal signal is used. The lower left hand figure represents the output of the DSM in the time domain and the corresponding frequency domain plot is on the right hand side. One can observe the spectral notch in the quantization noise created by the DSM. The poles of the DSM transfer function are located at 1/4 the sampling frequency, which is 3.2 GHz. Therefore our 800 MHz input signal will experience a good signal to noise ratio.

CLASS S Amplifier Circuit Device

Selected Characteristics of *GaAs FET (FLK202XV)*

Drain-Source Voltage (max. rating)

V_{DS} = 15 V

Gate-Source Voltage (max. rating)

V_{GS} = -5 V

Total Power Dissipation (max. rating)

P_T = 12.5 W

Saturated Drain Current (typ. value)

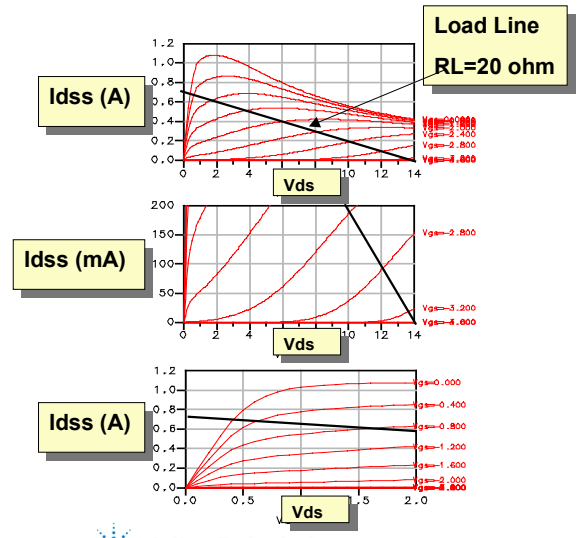
I_{DSS} = 800 mA

Pinch-off Voltage (typ. value)

V_P = -2.0 V

Power Gain at 800 MHz

$G_p \cong$ 15 dB



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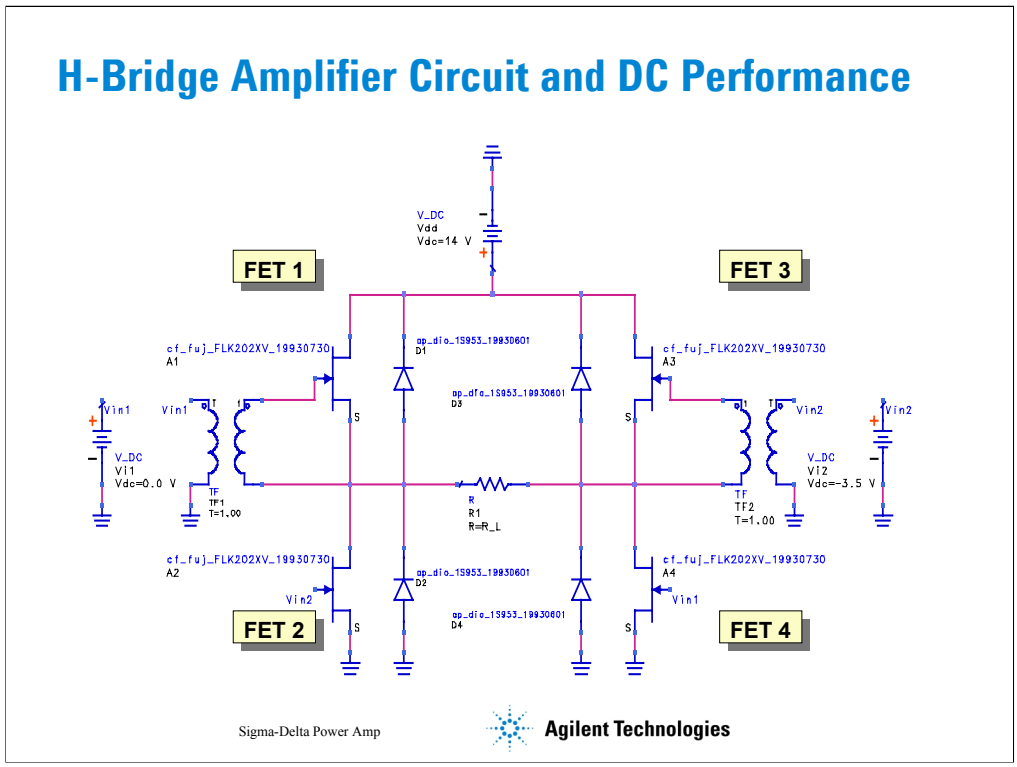
Microwave devices operating up to 10 GHz have to be used in our amplifier system, even though input signals are supposed to be in UHF band. That is because the sampling rate in the delta-sigma modulator is 4 times as high as the center frequency of the RF input signal.

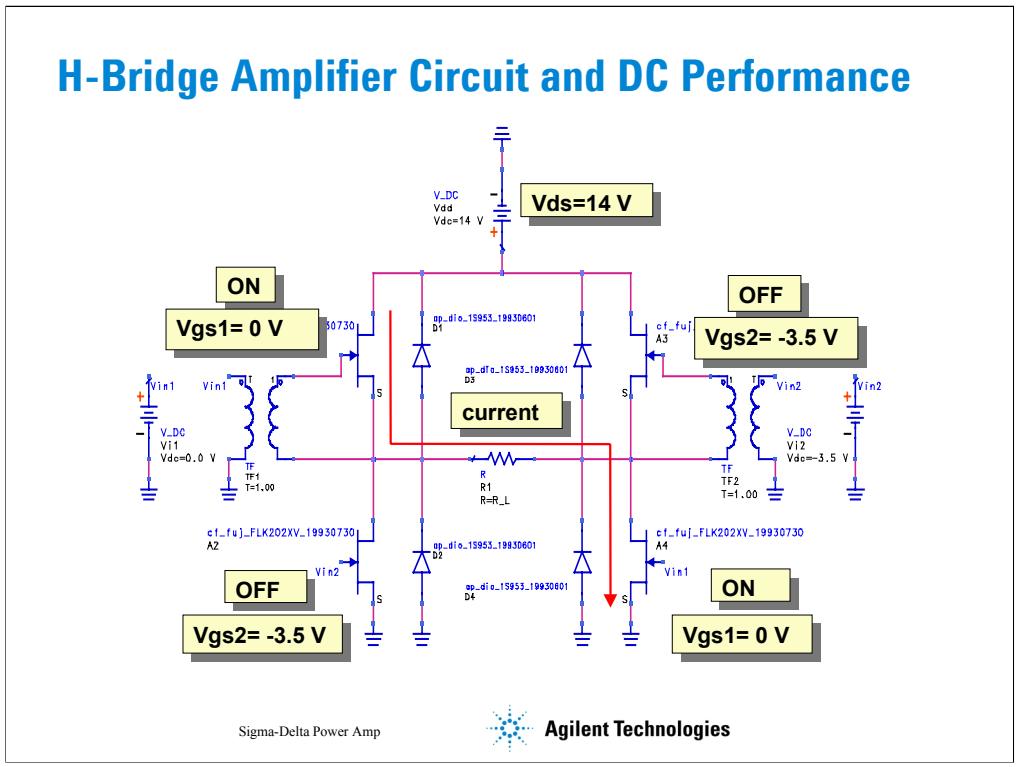
The characteristics of a Fujitsu's FLK202XVdevice are demonstrated.



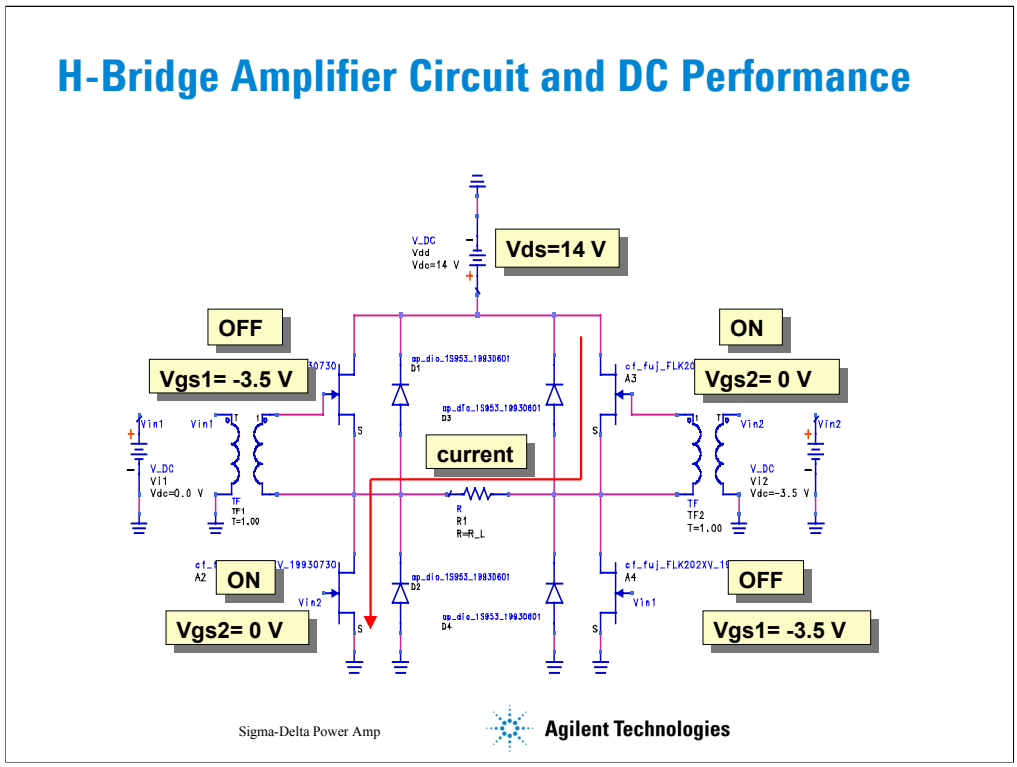
From the many SMPA configurations available, we have chosen the complementary voltage-switching H-bridge circuit as shown in the Figure.

Two complementary pulse voltage signals are driving the four FETs shown in the circuit. At any rising edge of the first input signal, FET1 and FET4 are turned on, while FET2 and FET3 are turned off. After a transient time, the amplifier output voltage (i.e. the input signal to the bandpass filter) is the DC supply voltage less the voltage drops across FET1 and FET4 in the triode region. The circuit stays in this state until the next rising edge of the second input signal arrives. During this time, the DC source power is converted to the RF load power by the current flowing through FET1 and FET4.

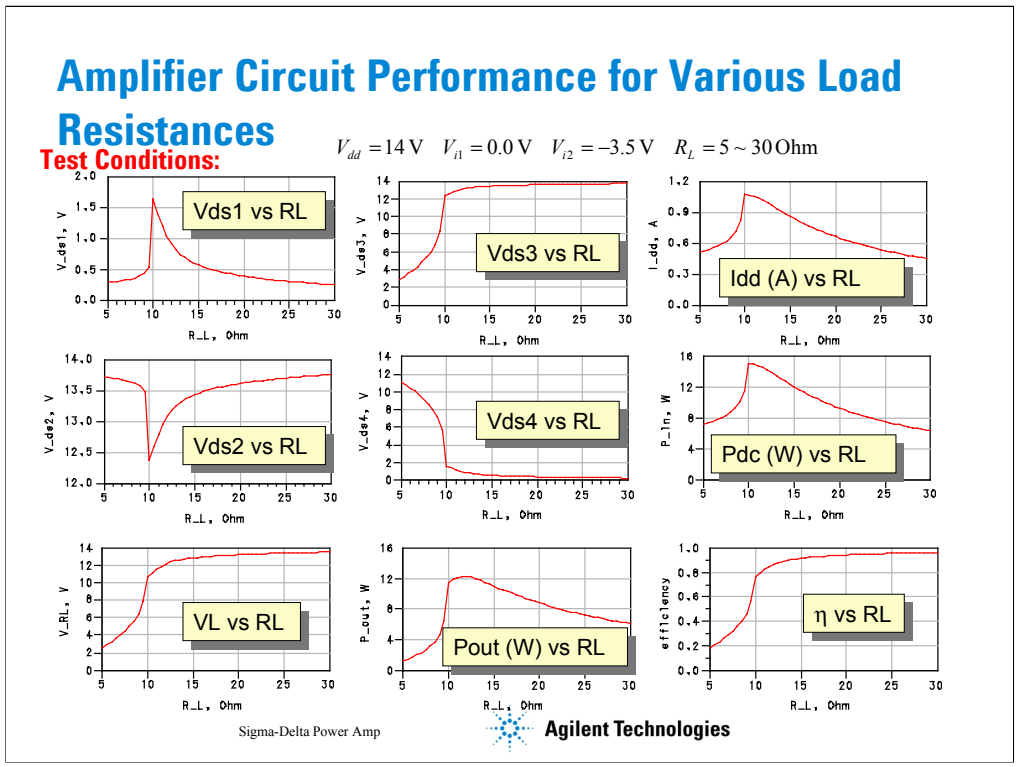
Once the next rising edge of the second input signal arrives, the circuit will change into another state; FET2 and FET3 are turned on, while FET1 and FET2 are turned off. The circuit behavior in this state is symmetrically the same as that in the last state described.



The current flow is indicated for one of the states. Using 4 devices here allows the output power to be doubled versus the typical 2 device topology. The diodes in the circuit are used to protect the devices from a reverse current flow. The output bandpass filter is not presented in this schematic.

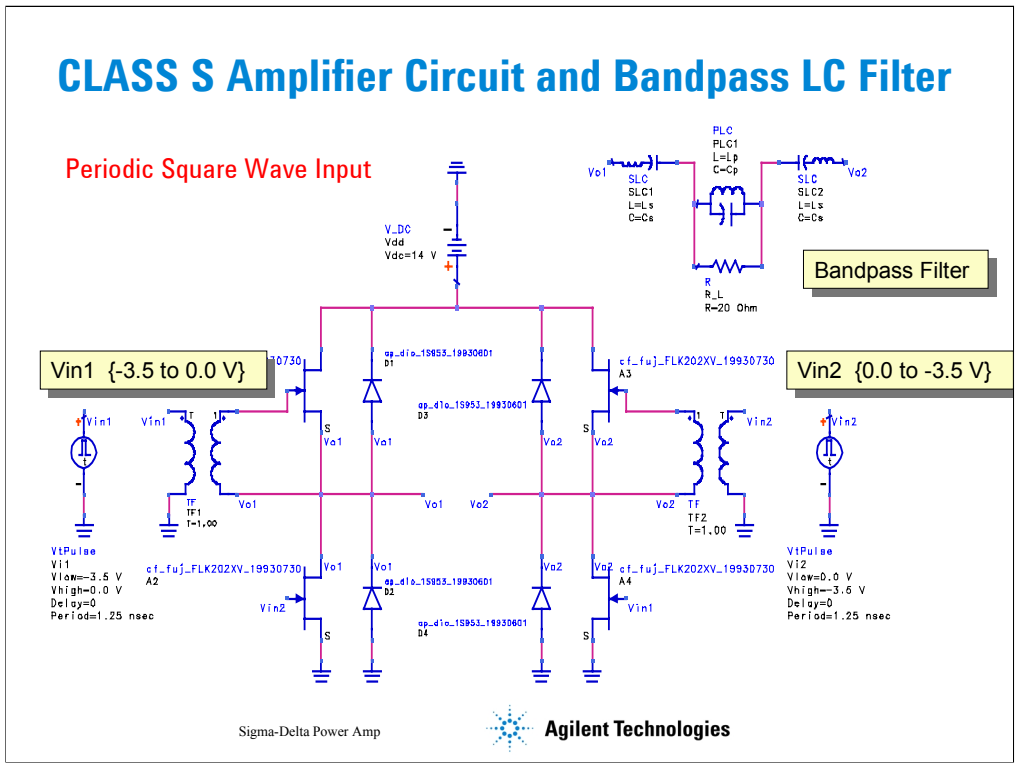


The current flow is indicated for the reverse state.

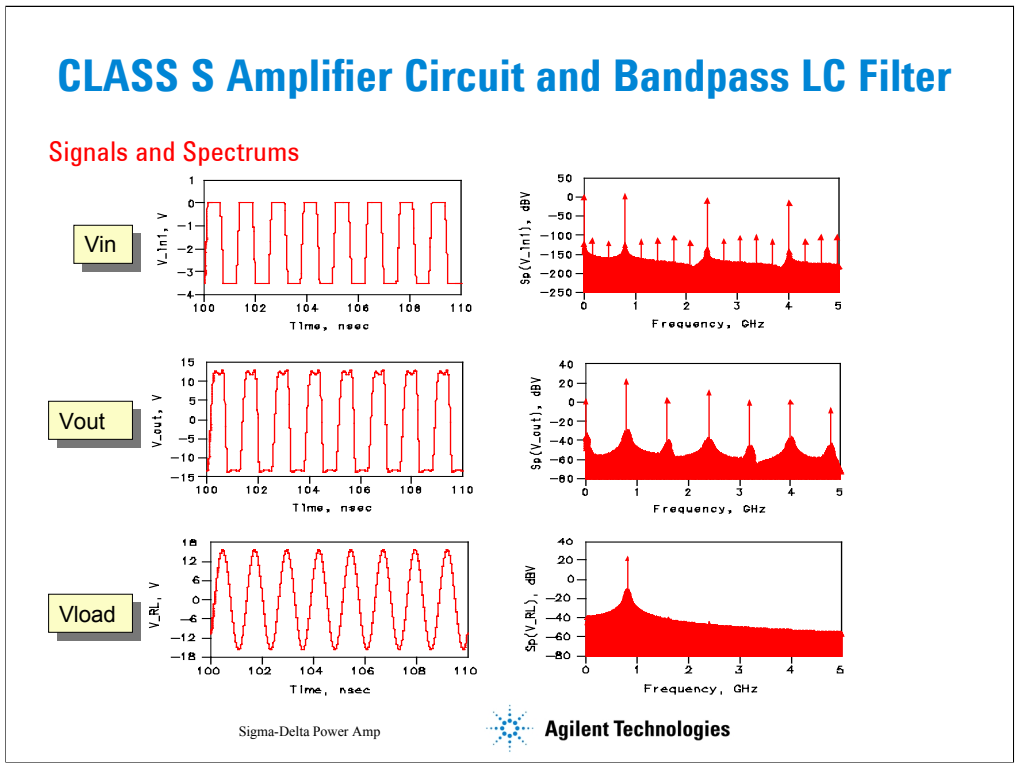


The performance of the H-Bridge switching mode amplifier is observed for various load conditions. Except for the transition time the devices work in two disctinct DC states, one with a low current (i.e. cut-off-state) and the other with a low voltage (i.e. saturation-state for BJT or ohmic-state for FET).

The diagrams in this page show the various DC-voltages and DC-currents in the circuit as well as power and efficiency depending on the variation of the load resistance (5 to 30 ohms). We can observe that a resistance of 20 Ohms is an optimum trade off between output power and efficiency.

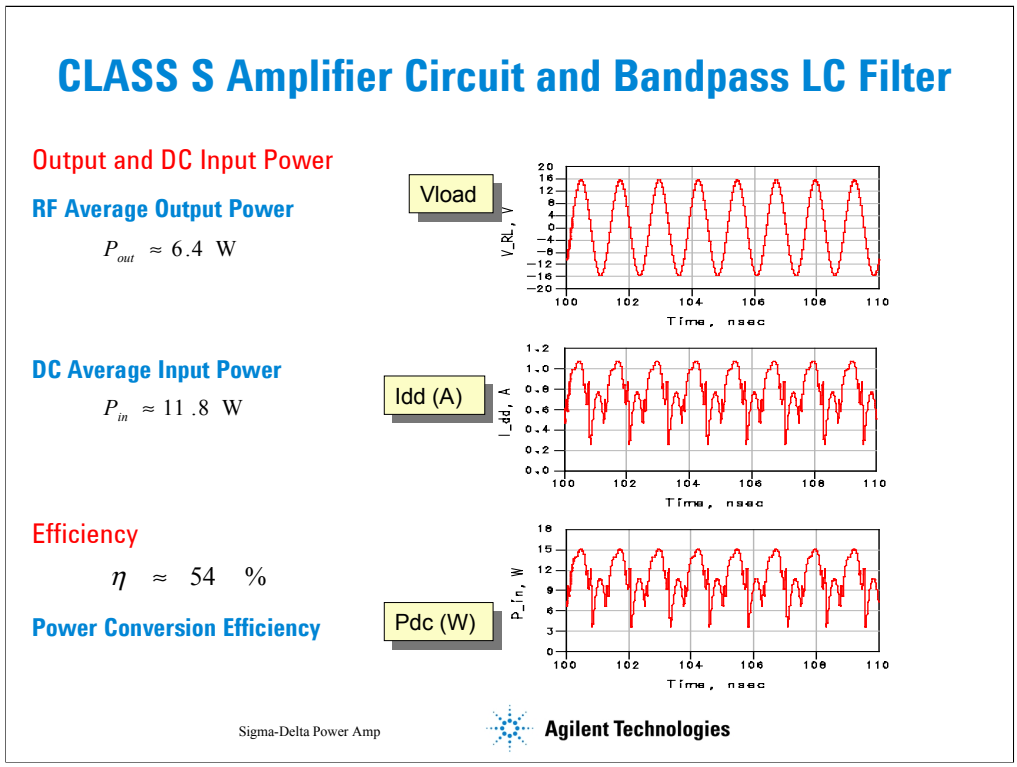


A periodic square wave is applied to the H-Bridge amplifier. The bandpass filter is 3rd order and the reactive components are assumed to have a Q of 100. The two sources are obtained by slipping one source into two phase-reversed parts.

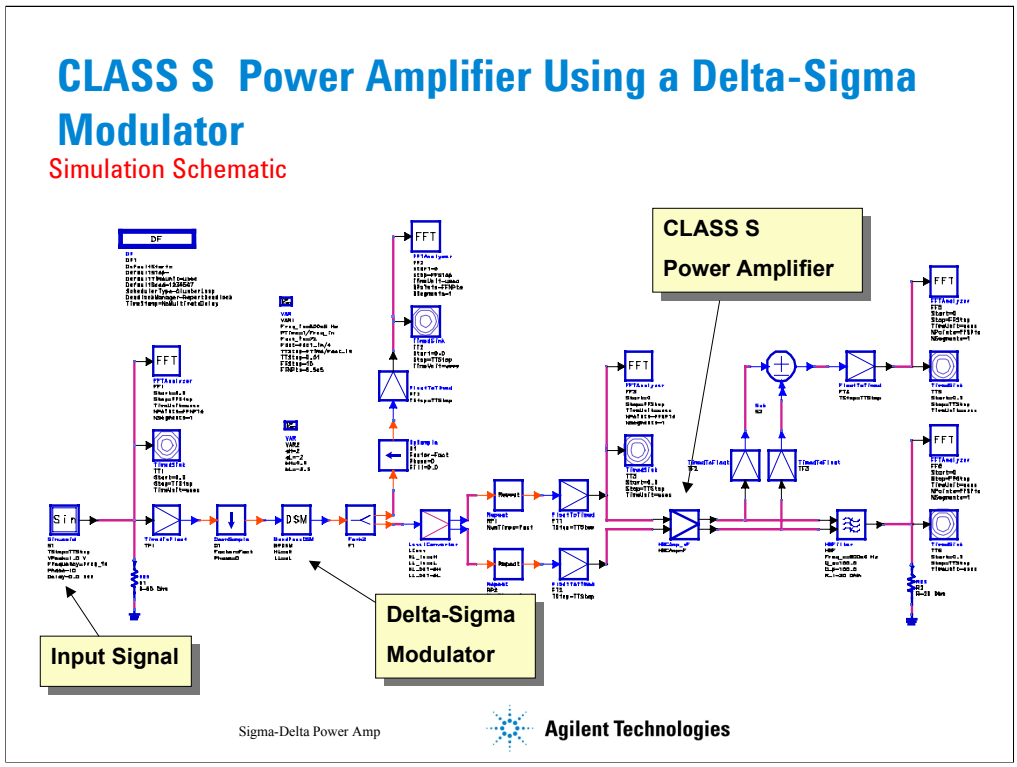


A periodic square wave is the input to the Class S amplifier. We can observe the distortion that is created at the output of the H-Bridge circuit. The signal is then reconstructed using a bandpass filter and appears across the 20 ohm load.

We can see that one of the distortions introduced by the class-S amplifier circuit is a higher noise floor in the output signal. The level of distortion is dependent on the speed of the Class S amplifier devices.

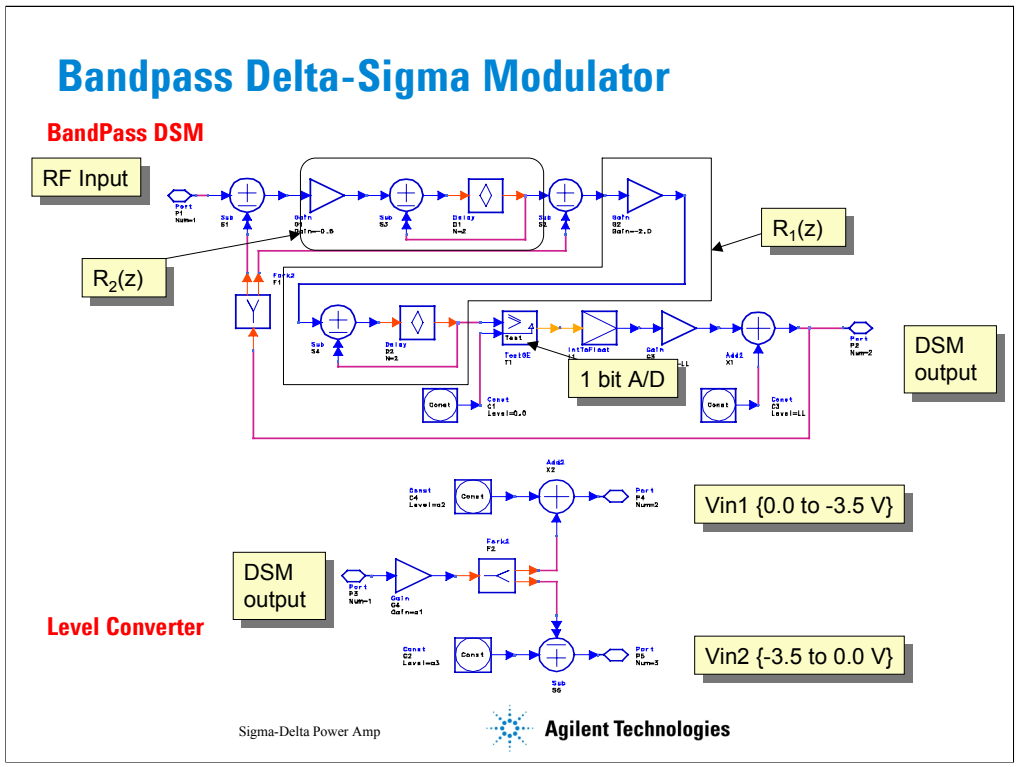


The efficiency of the Class S amplifier is approximately 54% for an output power of 6.4 Watts. This does not include the 200mW input signal power nor does it include the power dissipated by the Delta-Sigma modulator. A delta-sigma modulator was fabricated by Rockwell [2] using HBT technology and for a sampling rate of 3.2 GHz the power dissipated was just over 1.5 Watts.

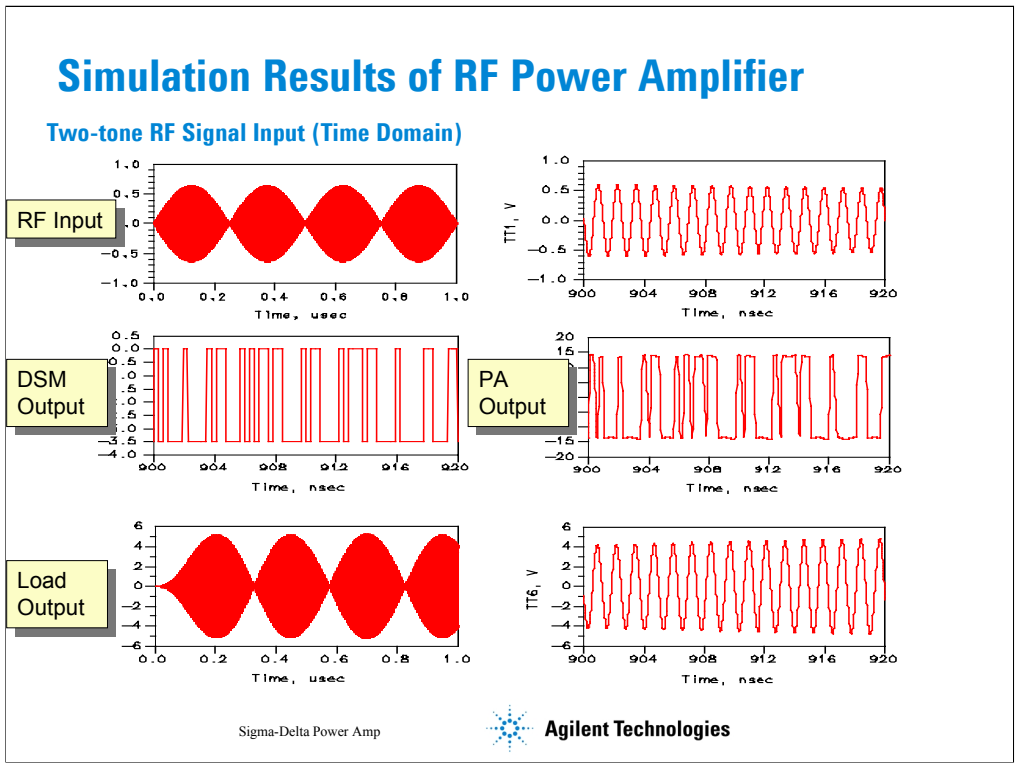


This is the schematic drawing for the Class S power amplifier project file.

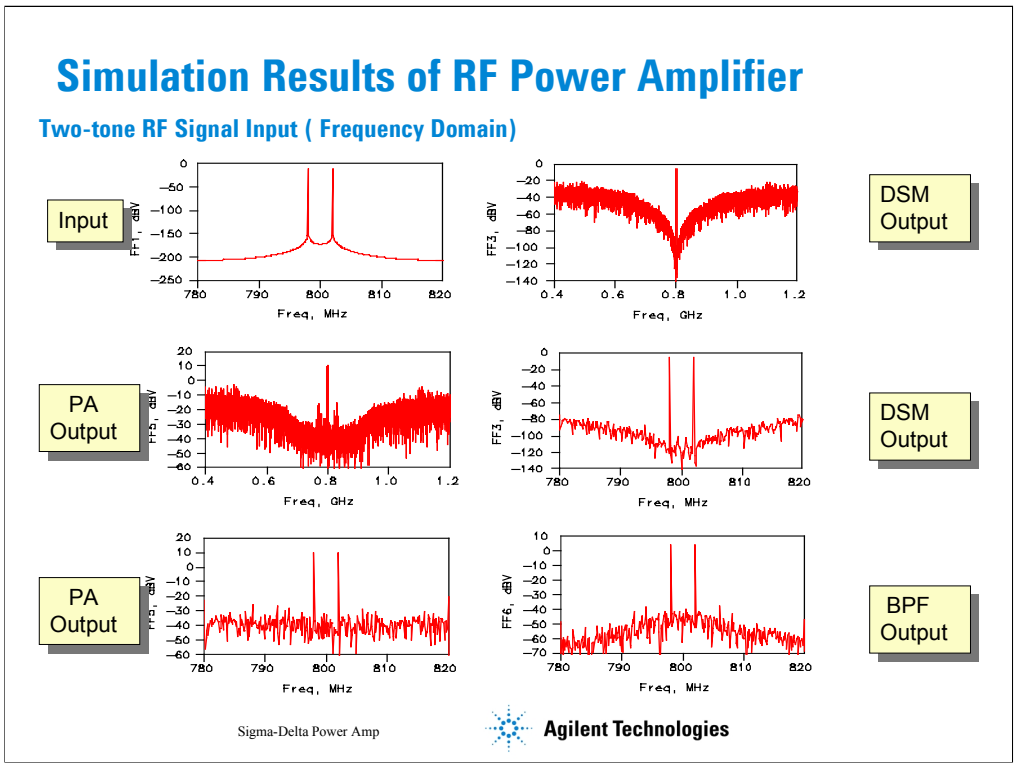
The circuit project consists of a signal generator and some measurement components such as signal display/processors and spectrum analyzers. This top schematic contains four sub-networks. Two of them are the H-bridge amplifier circuit and the bandpass filter. The schematics of the other two sub-networks, bandpass delta-sigma modulator and voltage-level converter are displayed on the next page.



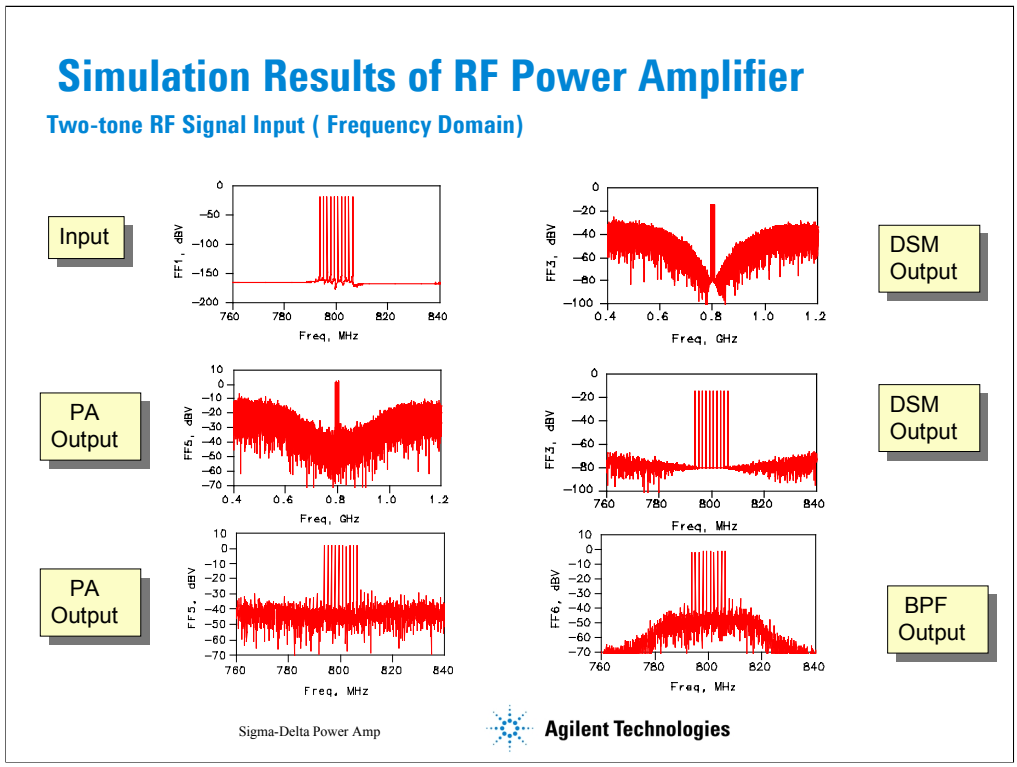
The individual components of the Delta-Sigma modulator are identified.The circuit was simulated using Agilent Ptolemy and the co-simulator in the Advanced Design System. The various blocks in the bandpass delta-sigma modulator are identified by there transfer functions. The Level Converter is used to transform a unbalanced signal to a balanced signal at the same time as imparting a DC offset for bias purposes.



A computer simulation of the whole amplifier system has been carried out for a two-tone input signal with the frequencies of 796 MHz and 804 MHz. The simulation results are presented in the time as well as in the frequency domain. From these we can see that an approximate replica of the input signal is well reproduced by the bandpass filter, although the amplifier output signal is totally corrupted in the time domain by the quantisation noise from the bandpass DSM and the distortion introduced in the H-bridge amplifier circuit.



Two sinusiodal tones (805MHz and 795MHz) are injected into the delta-sigma modulator. The spectral notch in the quantization noise floor is centered at (1/4 of a 3.2GHz sampling rate). The order of the bandpass delta-sigma modulator will determine the SNR versus spacing between the tones. Higher order modulators are more difficult to fabricate and are less stable. The PA output plot of our 4th order system demonstrates that a spurious output can appear. The spurious signals are dependent on the level of the input tones as well as their spacing. The resultant BPF output has approximately a 50 dB SNR for the 10 MHz bandwidth.



This ten-tone input signal has a bandwidth of about 14MHz and is centered at a frequency of 800 MHz. In the simulation the ten carriers are chosen with the same amplitude, but random initial phases. The resultant output signal has a SNR of approximately 45 dB. We can observe the noise shaping due to the analog RF bandpass filter.

Conclusion

- A second order BPDSM has been simulated. This BPDSM converts a RF analog signal into a 1-bit digital signal with about -80 dBc in-band SNR.
- A 800MHz switching mode power amplifier has been simulated. Its DC-to-RF power conversion efficiency can reach 54% with an output power of 6.4 watts. The SNR is 50 dB over a 4 MHz bandwidth and 45 dB for a 14 MHz bandwidth.
- Higher order BPDSM and alternative amplifier configurations can improve the in-band SNR performance.
- The growing need for high efficiency Cellular Power Amplifiers will inevitably lead to switching mode circuits.

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