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A SCALEABLE MODEL GENERATION METHODOLOGY OF
BIPOLAR TRANSISTORS FOR RF IC DESIGN

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Abstract
This paper presents a scaleable model generation methodology of bipolar transistors. Although the methodology has been targeted towards the compact model HICUM, it can also be applied to an appropriate subcircuit extension of the conventional SPICE Gummel-Poon model (SGPM), thereby allowing its usage in any environment. The methodology enables a generation of extensive model libraries containing transistor models for a large variation of geometry configurations available in a given technology. Such a library is mandatory for RF integrated circuit (RFIC) design, since proper transistor sizing is required to meet the stringent requirements of wireless consumer applications.

Modeling results for transistors of a production RF BiCMOS process are presented, demonstrating excellent agreement over a wide range of geometries and bias conditions. A circuit level verification with a Bluetooth RF front-end device is also provided as an example of first-pass design success enabled by the described methodology.

I. Introduction

The market of wireless communications demands low-cost, high-performance RFICs. Due to their excellent RF performance, bipolar transistors are being widely used in RFIC designs. Accurate performance prediction is crucial for first-pass design success, which is especially important for reducing cost and gaining invaluable market leadership. An accurate prediction, though, depends not only on a physical compact model formulation but also on the actual model parameters. While the compact model itself usually draws the major attention, the model parameter extraction and generation is often overlooked.

Conventional model parameter extraction is based on fitting the electrical characteristics of a single transistor. While this method can be suitable for designing certain small or discrete RF/Microwave components, due to its empiricism it usually provides very little insight into the process and, therefore, also very limited predictive capability regarding, e.g., process performance optimization and statistical modeling. Also, the extensive engineering cost associated with the method to generate extensive model libraries containing hundreds transistors of different geometries would make the method impractical for competitive industrial environments.

RFIC design is usually constrained by many system specifications such as noise, linearity, and power consumption. For portable applications, circuit design is even further constrained by the battery supply voltage. As a result, RFIC designers have to size the transistors properly to optimize the overall performance of an RF front-end block.

In this paper, we describe the application of a systematic methodology for model parameter extraction and generation, which meets the above requirements. The methodology generates a single unique set of specific parameters, which can then be used to calculate the actual (“SPICE”) model parameters for transistors of almost any geometry.

The methodology can also be applied to a simple subcircuit extension of the SGPM. Although over the years the SGPM has been found to have many deficiencies, a simple subcircuit extension with a careful parameter extraction can, in fact, meet most of the requirements for those RF front-end circuits, such as low-noise amplifiers (LNAs) and mixers, in which the transistors are operated at sufficiently low current densities (well below peak $f_T$). However, for large-signal applications where transistors are operated at high-current densities, such as power amplifiers (PAs) and drivers, HICUM is preferred.

The paper is organized as follows. The methodology is introduced in Section II. Device-level results are presented in Section III, followed by circuit-level verification in Section IV.

II. The Methodology

The methodology is based on the geometry scaling principles built into TRADICA [1]. The program generates model parameters for desired transistor configurations based on 1) geometry description, 2) process specific parameters, and 3) model specific parameters. Therefore, the methodology begins with gathering geometry information, such as (minimum) design rules. It is critical here to ensure that the parameters are generated according to the actual transistor layout. A coupling between model and layout generation is advantageous from a consistency point of view.

As the next step, the technology-related parameters are collected, such as field oxide...
thickness, emitter spacer width, size of the emitter metal overlap over base poly. These parameters are important for calculating the bias independent parasitic isolation (oxide) capacitances $C_E\text{ox}$ and $C_{Cox}$ that exist in parallel to the bias dependent BE and BC depletion capacitances $C_{IE}$ and $C_{IC}$, and are also scaled in a different way. $C_E\text{ox}$ and $C_{Cox}$ have to be eliminated from the extraction of the model parameters for $C_{IE}$ and $C_{IC}$. Without this elimination, the scaleability of $C_{IE}$ and $C_{IC}$ is limited. For the CS depletion capacitance $C_{JS}$, the treatment is different and depends on the isolation technique.

Next, the process-specific parameters are extracted. First, the area and periphery components of $C_{IE}$, $C_{IC}$ and $C_{JS}$ can be extracted, respectively, from the extrapolation and the slope of the total depletion capacitance, normalized to the respective area, versus the ratio of perimeter over area, i.e. $C/A$ versus $P/A$.

The sheet resistances of the internal (pinch) base and base link region are extracted from special enclosed-emitter test structures [2] with different emitter widths. By subtracting the current flowing through the short structure from that of the long structure, the non-parallel current flow across the corners and fore side is completely eliminated, allowing the above mentioned base sheet resistances to be precisely extracted from the results obtained for the different emitter widths. Using an additional structure with zero emitter width, the base link resistance, which is the primary part of the extrinsic base resistance for many processes, can also be determined [2].

The base contact and, e.g., silicide sheet resistance can be determined from a “contact chain” structure which features four equally spaced contacts. The contact portion and the silicide portion of the total resistance can be separated by sensing the voltages between the inner two contacts, that are caused by a current forced between first the outer and then the inner two contacts. In a similar manner, the collector contact and buried layer sheet resistance are extracted from a respective collector contact chain structure. Consistent results have been obtained for the emitter resistance using different methods [3][4], with the first one allowing self-heating effects to be simultaneously excluded, but being more difficult to apply. The emitter contact resistance is then extracted from the slope of the straight line obtained from the emitter resistances of transistors with different emitter areas. Note, that for processes with non-self-aligned BE formation the emitter resistance is not necessarily given by the poly-mono-silicon interface resistance and, therefore, not directly related to the emitter area.

With the above process-specific parameters, that were independently extracted, TRADICA can now be used to accurately calculate parameters of the extrinsic (parasitic) components according to the layout of transistors. The direct calculation, by its own definition, ensures a scaleable and consistent parameter generation for the extrinsic transistor components.

Based on accurate values for the extrinsic components, the internal transistor parameters can now be extracted. We start with the consideration of collector current spreading. The related current spreading angle $\delta_C$, which influences the modeling of the high current roll-off of $I_T$, is extracted from the critical current $I_{CK}$ obtained for transistors with different emitter window widths [5] at the same $V_{CE}$ value. $I_{CK}$ can be determined from the transit time $\tau(I_{C},V_{CE})$. Using the extracted $\delta_C$, the transit time parameters and, finally, the dc parameters are extracted. This methodology, although initially developed for HICUM, can also be applied to the SGPM (parameters $I_{TF}$ and $I_{KF}$). However, the details of the extractions of transit time and DC parameters are model-dependent and, thus, different for HICUM and SGPM. While the transit time parameters of HICUM can be quickly and reliably extracted without knowing DC parameters, an optimization technique is required to extract the SGPM transit time parameters.

Note, that for HICUM - in contrast to other models and methodologies - DC characteristics such as $I_C-V_{BE}$ and $I_C-V_{CE}$ need to be employed only at the end to extract the remaining model-specific parameters. This sequence has proved to be advantageous, since it avoids undesired iterative fitting and also puts the main emphasis on those parameters that are most important for RF IC design.

### III. Device-Level Results

The methodology is applied to generate model libraries for Conexant’s 0.35μm RF BiCMOS process [6]. Fig. 1 and Fig. 2 show transit frequency $f_T$, unilateral power gain $G_u$, and $y$-parameters over a wide range of bias conditions, $J_C$ and $V_{CE}$, for transistors with an emitter area of 0.4x14μm² and 1.15x14μm². No binning scheme is required to generate scaleable models for the geometry ranges offered by the process: emitter width = 0.4...1.15μm, emitter length = 1.4...21μm, number of emitter fingers = 1...4. Only the smallest transistor (0.4x0.7μm²) requires a few corrections due to lithography reasons.
IV. Circuit-Level Verification

The circuit considered here to demonstrate the model accuracy is a front-end device designed to enable long range (up to 100 meters) communication between Bluetooth devices. The device is manufactured with the process described before. The front-end device contains a PA to raise the transmit power of a class II Bluetooth transceiver from 4dBm to 20dBm. Also an LNA is included to improve the receiver sensitivity.

The PA consists of a class AB output stage and a cascode driving stage. While the output is matched externally to achieve the best compromise regarding output power, linearity, and power added efficiency (PAE), the input and inter-stage matching is done completely on-chip to minimize bill-of-material (BOM).

The LNA is a simple cascode stage with an on-chip balun to convert a single-ended signal to a differential signal at the output, so that it can interface easily with a differential Bluetooth device as well as a single-ended antenna. A cascode stage usually provides higher gain than a simple common-emitter stage. A cascode stage also exhibits excellent isolation characteristics, thereby avoiding iterative matching, which is definitely impossible for on-chip integrated components. However, compared with a simple common-emitter stage, a cascode stage looses precious headroom in favor of its advantages.

Fig. 3 shows the small-signal power gain $S_{21}$ of the PA at various supply voltages and bias/gain settings, i.e. BC00 .. BC11. Fig. 4 shows the small-signal power gain $S_{21}$ and the noise figure NF of the LNA. As shown in both Fig. 3 and Fig. 4, not only the absolute values of $S_{21}$’s and NF but also their tuning over frequencies are well predicted with the generated model. Besides accurate transistor models, accurate models for passive components and the package are also required to achieve such accurate predictions and, therefore, to increase the chance of first-time success.

Fig. 5 shows the distortion characteristics of the LNA which are reasonably well predicted by ADS in contrast to Spectre. As described in [7], the reason for the unexpected gain expansion seen in Spectre simulation at higher $P_{in}$ is due to the fact that the KCL, i.e. current conservation, in the frequency domain is not properly maintained by a pure time-base simulation. This situation can be mildly improved by

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**Figure 1:** Comparison between HICUM (lines) and measurements (symbols) for a 0.4x14$\mu$m$^2$ transistor: $f_T$ (left); $G_u$ (middle); $y$-parameters at $f=2$GHz (right); $V_{CE}/V=0.3$, 0.5, 0.8, 1.5, 3.

**Figure 2:** Same as in Fig. 1, but for a 1.15x14$\mu$m$^2$ transistor.

**Figure 3:** Small-signal gain $S_{21}$ of the PA at various supply voltages and gain setting. Dashed and solid lines represent measurement and simulation respectively.

**Figure 4:** Comparison between HICUM (lines) and measurements (symbols) for a 1.15x14$\mu$m$^2$ transistor: $f_T$ (left); $G_u$ (middle); $y$-parameters at $f=2$GHz (right); $V_{CE}/V=0.3$, 0.5, 0.8, 1.5, 3.
tightened error tolerances, however, at higher computation expense as well as the risk of numerical instability.

The slight offset in the harmonics prediction shown in Fig. 5 is explained as follows: As shown in [7], the nonlinear characteristics of the transistor are well predicted up to several GHz for a wide range of bias conditions and input power levels. However, the transistor in [7] is terminated with 50Ω in contrast to the LNA here, which is a tuned circuit and is designed with a typical narrow-band matching technique; i.e. this resonates at a specified frequency, but reflects the output power at other frequencies. Therefore, in order to precisely predict the higher order harmonic components, accurate prediction is required for not only the distortion characteristics of the transistor, but also the frequency response, i.e. the Q factor of the overall circuit. As observed in Fig. 4, although S21 and NF of the LNA at the 2.4-2.5GHz band is well predicted, the simulated curve deviates from the measured one at higher frequencies, thereby causing the slight offset in the harmonic prediction.

Figure 4: Small-signal gain S21 and noise figure NF of LNA. Symbols and lines represent measurement and simulation, respectively.

Figure 5: Large-signal characteristics of the LNA. As shown in Fig. 6, the maximum output power, the power added efficiency (PAE), and 1dB compression point (P1dB) of the PA are also well predicted to the extent of obtaining the first silicon success.

V. Summary

A scalable model generation methodology for bipolar transistors is presented. The methodology is efficient in generating extensive model libraries for RFIC design. Experimental results for a production RF BiCMOS process are provided, confirming the quality of the model library generated with the methodology. Finally, an example of first-pass design success enabled by this methodology is presented, demonstrating the usefulness of the modeling methodology for RF IC design.

Figure 6: Large-signal characteristics of PA.

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References
