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PLL FM-Modulator Suitable for Mobile and Radio Communication Simulation

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PLL-FM MODULATOR SUITABLE FOR MOBILE AND RADIO COMMUNICATION SIMULATION

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ABSTRACT

This paper shows a new PLL-FM Modulator with rapid acquisition time about 1000 times less than the conventional PLL with less spurs which is suitable in Mobile and Radio communication.

One of the great advantages of the proposed PLL is that it doesn't need LPF(since no spurs coming form the Phase Detector) thus good frequency switching speed and no degradation in transients. The proposed PLL here uses a new technique where the phase detector here acts as a subtractor not between the Ref. Signal and the V.C.O output but between their linear phase time function sawtooth.

1. INTRODUCTION

In radio & mobile communication high speed frequency synthesizer used has to have fast carrier-frequency acquisition speed & lower cutoff modulation frequency.
For high speed frequency synthesizer there are two types, one is the digital frequency synthesizer (DDS) where the switching speed is high but spurs appear is difficult to reject them, also DDS needs high power consumption.
The second type are PLL-synthesizers which are less power consumption & easily implemented in small communication equipment.
One of the main problems of this type of PLL-FM modulators that a low pass filter (LPF) is required to suppress the spurs coming from the phase detector but at the same time the LPF decreases the frequency switching speed thus causes degradation of the transients.
One of the advantages of the proposed PLL-synthesizer in this paper that it doesn't need a LPF where no spurs are generated from the phase detector. The phase detector proposed here is no more than a subtractor between the reference phase & feedback phase coming from the V.C.O.

2. PLL BASIC BLOCK

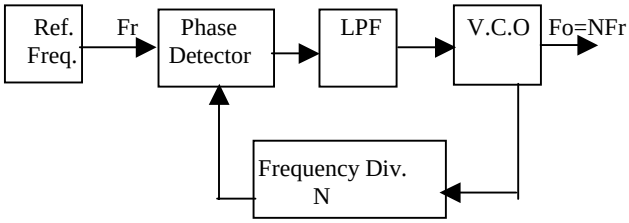


Figure 1

Figure1 shows the PLL basic block describes the normal PLL-synthesizer where the Reference Frequency Fr is applied to one input of the phase detector & the output of the V.C.O which has a central frequency Fo=NFr is applied to a frequency divider (N) & the output of the frequency divider is applied to the other input of the phase detector.
The phase detector generates a phase error where the LPF takes the average signal & adjust it to be suitable applied to the V.C.O which notices the phase error thus increasing or decreasing its output frequency.
The Process is repeated several time until the locking is done where the output frequency of the V.C.O is NFr and synchronized with the input reference frequency Fr. Here the LPF with K(lpf)=(KpKlKv.c.o)/N, where K(lpf),Kp,Kl,Kv.c.o, represents the gains of LPF, Phase detector, Loop gain & Voltage control oscillator, causes degradation in the loop transient time which is not useful in case of mobile communication.
That means for the normal PLL-synthesizer for any small change in N division factor needs a higher locking time which becomes useless in some applications specially in mobile communications.
In the next section, a proposed PLL-synthesizer which doesn't need a LPF will overcome this problem.

3. PLL-FM with fast acquisition time.

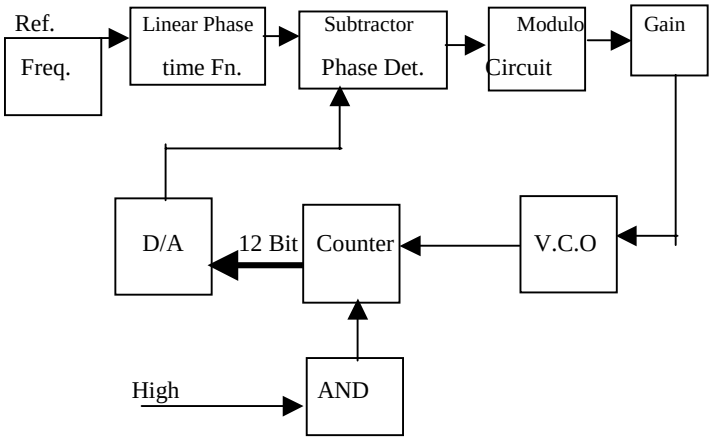


Figure 2

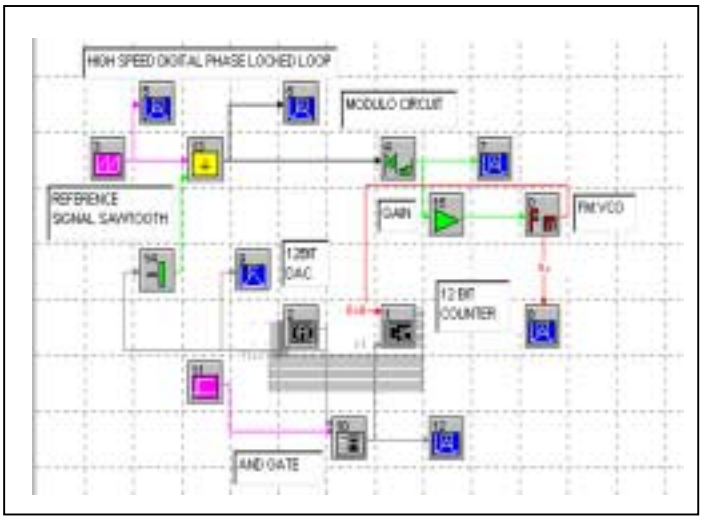


Figure 3

Figure 2 shows a new PLL-FM modulator block diagram and can also be suitable in synthesizer applications. The proposed block diagram is confirmed by a DSP tool "System View". The block diagram design area of System View is shown on Figure 3. The idea of this PLL is that the phase detection is not done directly between reference frequency & V.C.O output frequency but is done between their linear phase time function sawtooth, where for e.g. if the reference frequency is a sinusoidal, therefore its phase time function is a sawtooth with a slope representing the frequency of the reference frequency (e.g. for a sawtooth of freq. 5MHz & 10 V amplitude, that means that the slope of the sawtooth is 10V*5MHz=50 which represents the frequency of the input reference frequency as figure 4.a).

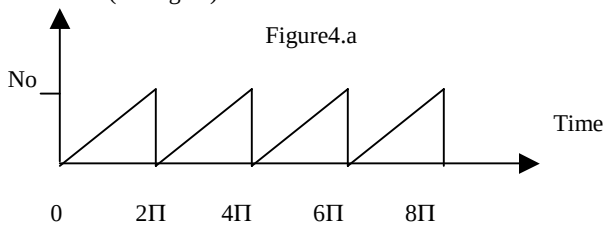
Any change in the reference frequency will be reflected to the slope of the generated sawtooth. This idea is also applied to the sinusoidal output of the V.C.O. as figure 4.b

The role of the DSP phase detector here is to subtract the difference between the two sawtooth's signals as figure 4.c (one representing ref. Signal and the other represents the V.C.O) and the output is gone through a modulo circuit where it gives an average phase difference as figure 4.d, where this phase difference is gain adjusted and applied to the input of the V.C.O where it begin to correct its generated frequency.

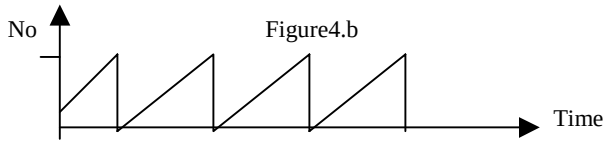
The Role of the Modulus Counter beside the AND gate and A/D to generate the corresponding sawtooth function of the V.C.O & give it to the other phase detector input as figure 4.e. The process is completed several time until locking is realized between the two sawtooth's signals which means locking between initial reference sinusoidal signal & voltage control oscillator output.

Here the spurs generated from the phase detector is minimum thus No LPF is needed. For the phase detector and the linear phase Time function, DSP technique is preferable.

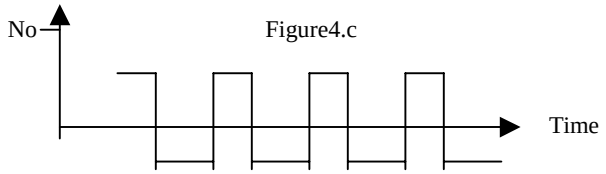
Linear Phase (ref.Signal)



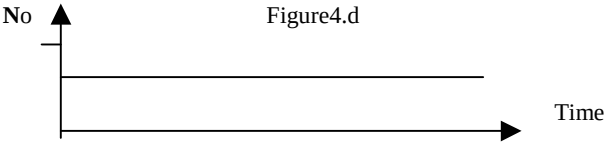
Linear Phase (V.C.O)



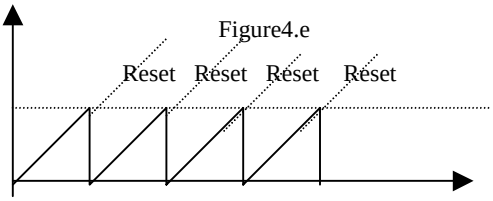
Phase Detector O/PT.



Modulo circuit o/pt.



Behavior of Modulus Counter



In the next section we will show simulation which shows the locking between the two sawtooths signals and how it is realized fastly nearly from the first cycle.

4. Simulation Results

4.1 General Parameters

Reference Sawtooth signal

-10 V amplitude
-5MHz freq. representing 50MHz Sinusoidal Input Signal
-Phase=0 degree.

V.C.O

-Sinusoidal with amplitude 5V, Fo=50MHz
-Sensitivity 3.5MHz/V

DAC

-12 Bit, Threshold=0.5V

Counter

-12 Bit, Threshold=0.5V

Modulo Circuit Value = 10
Gain=3

4.2 Input Signal Frequency & Phase variation.

4.2.1
Reference awtooth signal
-10 V amplitude
-5.1MHz freq. representing 51MHz Sinusoidal Input Signal
-Phase=0 degree.

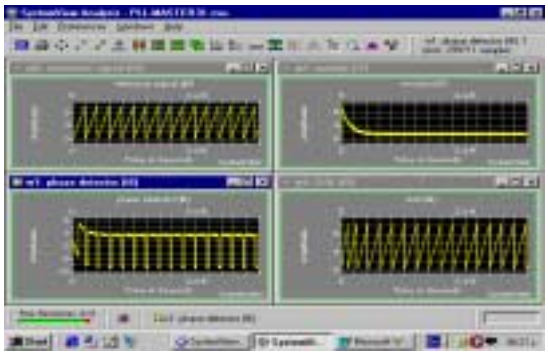
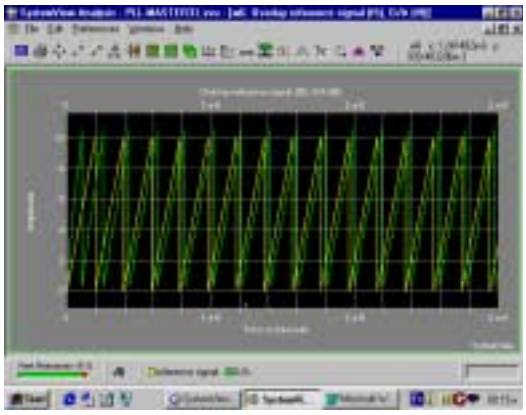


Figure 5



4.2.2
Reference Sawtooth signal
-10 V amplitude
-5.1MHz freq. representing 51MHz Sinusoidal Input Signal
-Phase=90 degree.

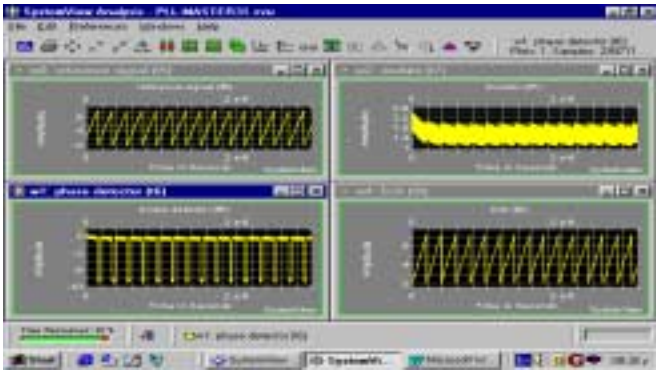
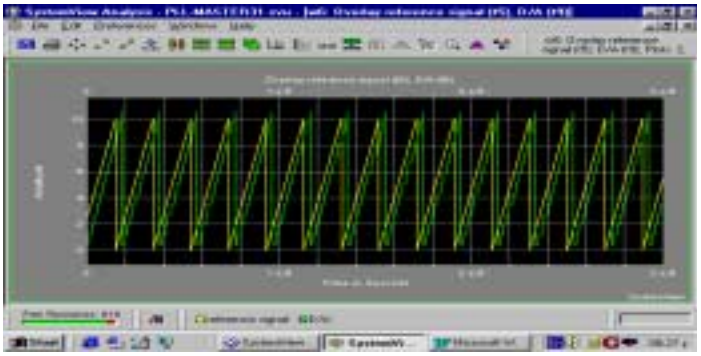


Figure6



4.2.3
Reference Sawtooth signal
-10 V amplitude
-5.4MHz freq. representing 54MHz Sinusoidal Input Signal
-Phase=90 degree.

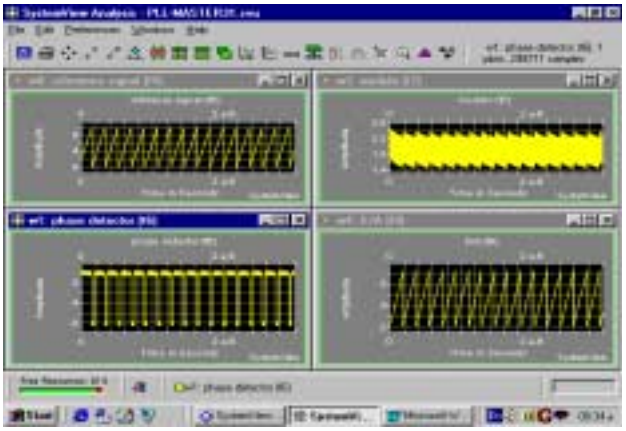
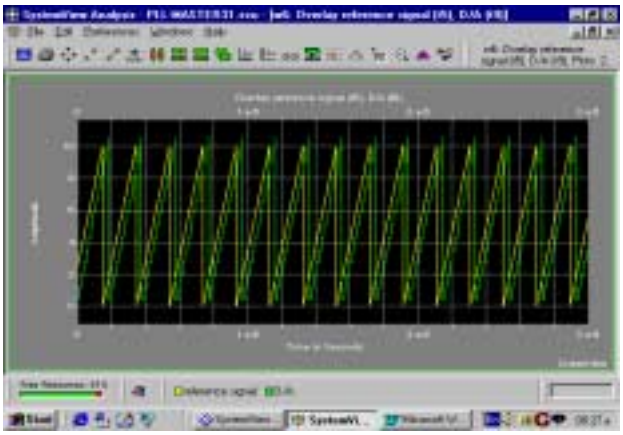


Figure 7



5. Simulation Conclusion

As shown from the above figures when we change the frequency of the input sawtooth from the 5 to 5.1 MHz (means ref. Freq. of 10V*5.1MHz=51MHz with phase error = 0 degree) the locking is realized so rapidly as figure 5 & when we change the phase i/pt of sawtooth to be 90 degree with the same frequency still locking happens rapidly as figure 6 . Also even if the reference Freq. reached 10V*5.4MHz =54MHz reference sine signal still we have rapid locking as figure 7.
That means for any higher change in frequency or phase of the input reference signal still locking happens so rapidly.

Also shown less number of spurs at the phase detector output which make the PLL doesn't need any Low Pass Filter.

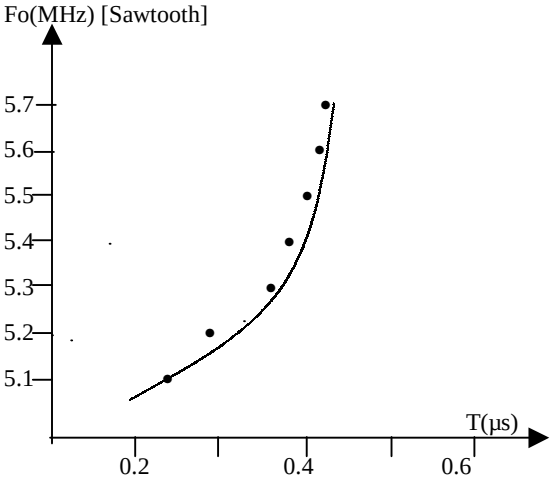


Figure 8

The above Figure 8 shows the relationship between the change of step frequency 1Mhz for the reference frequency and the settling time which is in the range of 0.2µs for locking for the proposed Digital PLL while for normal Digital PLL it is in the range of mseconds. The above figure was deduced from different points by changing input frequency by step of 1 Mhz, where a high locking speed was noticed.

6. References

-IEEE High Speed PLL frequency synthesizer for Mobile communication by Akihiro Kajiwara & Massao Nakagawa 1992
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- Switched Capacitor PLL Frequency synthesizer by M.Abou El-Ela NRSC 99.
-Phase locked loops Theory, Design and applications by Roland Best "Mgcrohill" 1984.

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