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An Integrated EDA-Tools Flow Improves Designers' Productivity

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AN INTEGRATED FRONT-TO-BACK DESIGN FLOW IMPROVES QUALITY AND EFFICIENCY IN THE DESIGN OF A PRESCALER.

An integrated EDA-tools flow improves designers' productivity

DA SOFTWARE IS THE KEY to efficient design of an RF IC. Ideally, designers want to use one software product for every step in the design process—from schematic entry to final layout. However, a complete design flow more likely requires the use of several compatible tools. To demonstrate this more likely scenario, the following design flow of a prescaler (frequency divider) RF IC uses several types of software (Figure 1).

I began the process using Cadence for schematic entry and layout (www.cadence.com). Agilent's RF IC Dynamic Link then allowed me to directly simulate the Cadence schematics within Agilent's ADS (Advanced Design System, www.agilent.com). IBM provided design kits (model libraries) for the IBM 5HP SiGe foundry for both ADS and Cadence. I performed layout verification with Columbus RF from Sequence, and IBM's SiGe foundry service fabricated the prescaler (www.ibm.com, www.sequence design.com). For design-flow verification, I measured a number of samples and compared those results with results from the simulation.

The prescaler design is generic and uses no proprietary circuitry to enhance device performance. It is intended to show what tools are necessary for predictive design, to ensure a single pass through the chosen IBM foundry.

Keep in mind the following points about the design flow:

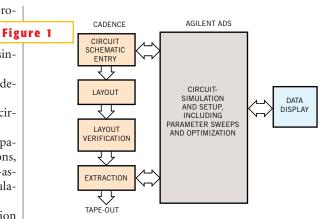
- Cadence is the single point of entry for the circuit schematic.
- ADS is used for simulations, which include parameter sweeps, frequency-domain optimizations, swept-frequency analysis using TAHB (transient-assisted harmonic balance), and phase-noise simulations
- ADS templates are used to speed the simulation set-up.
- Device models are from IBM's 5HP SiGe design kit.

• Layout is done in Cadence, using parameterized cells from IBM's SiGe design kit.

THE DESIGN FLOW

In this project, after entering the schematic of each circuit I simulated into Cadence, I used ADS to carry out the required simulations and incorporated the Cadence schematics as subcircuits via the RFIC Dynamic Link. I used the ADS simulation setups to sweep various parameters and examine their effects. Once the design achieved acceptable performance, I created a layout in Cadence. Using a design rule checker on the layout, I verified that all of the IBM process-design rules were satisfied. I used an LVS (layout-versus-schematic) check to verify that the final schematic matched the layout, then simulated the extracted layout (required for the LVS check) to see whether the prescaler still operates satisfactorily. Finally, I submitted the layout for fabrication.

My approach was to start with simple, ideal circuits, verify that they function, see how performance



The design flow of a prescaler (frequency divider) RF IC uses several types of software, including Cadence and Agilent ADS.

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varies with adjustable parameters, and gradually replace ideal components in the circuit with nonideal elements. As described above, the divide-by-2 frequency cell consists of an edge-triggered D flip flop (comprising a master latch driving a slave latch), with the Q and \overline{Q} outputs connected to the \overline{D} and D inputs, respectively. The main variables to adjust are the bias currents in each latch and the signal am

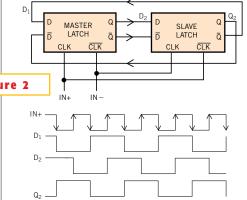
If you are a Cadence user, you may be wondering why you should go to the trouble of running your simulations with ADS. For this application, the main reason is that using ADS's

plitudes at the inputs and outputs of

harmonic balance simulator—which gives you steady-state results—with parameter sweeps, helps you quickly determine which circuit parameters you should change to improve performance. You can also use it to determine the noise performance.

The following steps describe the design sequence and simulations you use to implement the above procedure:

- Simulate the dc current-voltage curves of a single transistor (to verify that the RFIC Dynamic Link is working properly).
- Simulate the S-parameters versus bias voltage for a single transistor.
- Simulate the propagation delay of an emitter-coupled pair versus collector resistance, bias current, and emitter length.
- Simulate a single latch with an ideal current source.
- Simulate a divide-by-2 cell with ideal current sources.
- Sweep divider input frequency, bias current, collector resistance and other parameters to see how high an input frequency the divider will divide.
- Design and simulate a current mirror.
- Repeat the divide-by-2 swept simulations with current mirrors instead of ideal current sources.
- Simulate the divider with a sinewave input signal instead of a pulse-input signal.
 - Use TAHB to simulate phase noise.
- Sweep parameters to determine what affects phase noise, and determine what trade-offs you can make.
- Design and simulate an input amplifier.



In this prescaler block diagram, a D-flip-flop master latch drives a D-flip-flop slave latch, with the outputs of the slave fed back to the inputs of the master.

- Repeat divider simulations with the input amplifier, including tests to verify which range of input-signal amplitudes the divider still divides over; simulate performance with a single-ended input signal.
- Design and simulate an output amplifier.
- Repeat divider simulations with both the input and output amplifiers, and again verify which range of input signal frequencies the divider divides over.
- Simulate phase noise of overall divider circuit, including both amplifiers.
- Readjust parameter values to improve phase noise, and check frequency range of divider circuit. (Assume there will be a trade-off between frequency range and phase noise.)

The first step in the design process is to simulate the current-voltage curves of a single transistor from the IBM SiGe design kit and investigate how S21 varies with bias at a particular frequency. Some might argue that the S-parameters of the device are irrelevant in this application, because you're using the devices in a nonlinear, switching application. However, they are relevant because you're concerned with frequency-domain behavior as well as time-domain behavior.

I created a Cadence schematic for the single transistor and then a Cadence symbol view. ADS uses this same Cadence symbol. **Figure 3** shows the S-parameters of the transistor versus bias at the analysis frequency of 20 GHz.

EMITTER-COUPLED PAIR SIMULATIONS

After simulating a single transistor, the next step is to simulate the basic building

block of a frequency divider, the emitter-coupled pair. I needed to first simulate the dc characteristics of this circuit, then its switching speed. I set up the dc sweep analysis in ADS. You must sweep both the common-mode and differential-mode bias voltages (although you could also sweep other parameters, such as bias current, emitter length, and collector resistance).

I wanted to determine the output-signal voltage swing and the required differential voltage swing to completely switch the current from one device to the other by observing the values of the emitter-coupled pair output voltages and emitter currents versus differential-mode

input voltage. An approximately 200-mV change in the differential-mode input voltage is sufficient to completely switch the current.

After examining the dc transfer characteristics, you can investigate the switching delay speed and what you can do to improve it. For this project, I ran a timedomain simulation and drove the emitter-coupled pair with a differential-mode input step.

Next, I needed to create a "TimeDelta" probe, which measures the propagation delay. Using ADS simulation, I swept the emitter bias current, IEE, while varying the collector resistance, R_{COL}, along with IEE, so the voltage drop across the resistor, which sets the logic "low" level, remained unchanged. To determine how the Q and \overline{Q} output signals vary with bias current IEE, I analyzed the Q and \overline{Q} output signals versus time, in response to a 5-psec differential-mode step in input voltage. I also looked at the high-to-low and low-to-high propagation delays versus emitter bias current. Based on the simulation results, I chose an emitter bias current of 10 mA, although 8 mA would produce about the same performance.

PRELIMINARY DIVIDE-BY-2 SIMULATIONS

Once you investigate the emitter-coupled pair circuit, you are ready to build a basic frequency divider. I used two identical latch circuits, with ideal bias current sources, connected as shown in **Figure 2**. I verified that this configuration operates as a frequency divider and determined the maximum frequency in which it will operate when the input signal is a differential-mode square-wave clock. I also in-

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vestigated how the maximum frequency of operation varies with different circuit parameters, such as bias currents, emitter lengths, collector resistances, and clock signal amplitude.

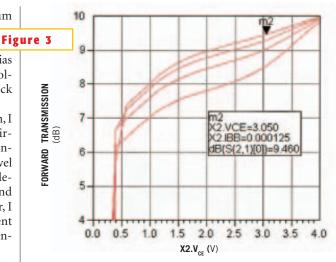
To perform the simulation, I built a preliminary latch circuit. I used transistors connected as diodes as level shifters to keep the input devices of both the master and slave out of saturation. Later, I replaced them with current sources to get higher frequency performance.

Figure 4 shows the ADS setup for simulating the preliminary divide-by-2 circuit. I swept the differential-input clock to determine the highest frequency of operation. Vari-

ables defined on this schematic ($R_{\rm COL}$ and EMITLENGTH) passed into the Cadence subcircuit.

Defining the shape of the input pulse allows you a lot of flexibility. One of the limitations of doing a swept transient pulse is that it can take many clock cycles for the divider to reach a steady state. You have to restart from time=0 every time the clock period changes. With TAHB, this wait for the initial transient to die out is unnecessary.

The simulation results indicated that the frequency divider works to 23.75 GHz. I made a number of iterations to



S-parameters are relevant in this application because you're concerned with frequency-domain behavior as well as time-domain behavior. The graph depicts the S-parameters of the transistor versus bias at the analysis frequency of 20 GHz.

the circuit-parameter values before achieving this performance. However, because the parameters used for the simulations did not include parasitics and because the current sources were ideal, it is unrealistic to expect this level of performance from the fabricated ICs.

PHASE-NOISE SIMULATION

The phase noise that a frequency-divider circuit contributes is an important specification. Designers want to know the predicted phase-noise performance of their circuits, as well as what changes they can make to improve noise per-

formance. Time-domain simulators, such as Spice and its derivatives, do not support phase-noise calculations. However, the ADS 2001 transient simulator supports time-domain noise from and V Noise I Noise sources. In ADS 2002, the (time-domain) transient simulator supports both linear and nonlinear noise sources. Harmonic balance does simulate phase noise, but it needs some help to solve frequency-divider circuits. TAHB enables harmonic balance to solve circuits like these and operates as follows: You run a transient simulation until the circuit reaches a steady state. The simulator computes the

spectra of the periodic node voltages and branch currents, saves them, and uses them as an initial estimate for harmonic balance. In many cases, harmonic balance is then able to converge on the solution. Once harmonic balance converges, you can run a phase-noise simulation or various sweeps.

For more accurate noise simulation, I replaced the ideal current sources that biased the latch circuits with a simple transistor current mirror. As an experiment, I investigated how the phase noise varied with bias current. To make this experiment easy to carry out, I defined a

HOW A PRESCALER WORKS

A divide-by-2 prescaler is a "digital" circuit that outputs a signal at half the frequency of the input signal. In this design, a D flip-flop master latch drives a D flip-flop slave latch, with the outputs of the slave fed back to the inputs of the master. With the connections shown in **Figure 2**, the output signal from the slave will be at half the frequency of the input clock. By combining these connections in series, you can implement division by four, eight, and more factors.

Because prescalers are digital circuits, once you reach the voltage threshold of operation, the

output-signal amplitude is nearly independent of the input-signal amplitude. The input-signal amplitude needs to be only large enough to switch the current in an emitter-coupled pair from one side to the other.

Prescalers are often used in PLLs or multiplexers. They are used in PLLs when the VCO frequency is higher than the maximum operating frequency of a programmable divider. Prescalers are also used for multiplexing signals together in optical transmitters.

The key specifications of a prescaler are the minimum and

maximum input-signal power levels over which the prescaler will operate, the frequency range over which the prescaler will operate, and phase noise (frequency domain) or jitter (time domain). If you were putting a prescaler into production, additional specifications would include the size of the die, the operating-temperature range, power consumption, and other parameters.

Prescalers are difficult to simulate or measure, because the output frequency is not the same as the input frequency, and you must sweep both the input frequency and the inputsignal power level for proper simulation. In addition, the circuits are nonlinear, so you must use a nonlinear simulator. Most specifications of interest describe steady-state conditions, which means that if you use a time-domain simulator, you have to run the simulation long enough for the turn-on transient to die out. This time is multiplied if you are running more than one simulation while varying parameters such as clock frequency or amplitude. To avoid this problem, use harmonic balance simulation.

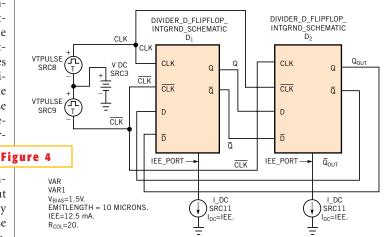
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current multiplicationfactor variable, "Imult-Factor," making the current-mirror resistances and emitter sizes a function of this variable. You can study the amplitude and phase noise at one offset frequency versus the current multiplication factor. This simulation did not include input or output amplifiers, so it is likely that the actual phase noise would be worse. You can easily vary other circuit parameters and see the effect on phase noise.

The input amplifier provides a reasonably good match to 50Ω , handles either differential- or single-ended signals, and converts a reasonably large dynamic range of input signal amplitudes to a signal level sufficient to drive the divide-by-2 circuit. The design is simply an input-stage emitter-coupled pair driving two stages of emitter followers. I looked at the dc transfer curves, small-signal frequency response, and the large-signal gain compression, and varied the bias currents in the different stages. I set the current mirror currents by current multiplication factor variables for ease of experimentation.

To determine the small-signal frequency response, I swept the values of the current in the input emitter-coupled pair and simulated the small-signal differential-mode gain versus frequency with ADS. The simulation results indicated that the gain increases with bias current, as expected.

It is also important to examine the large-signal characteristics of the amplifier to determine the range of input signal amplitudes over which the divider will function. Because it is easier to generate single-ended signals at microwave frequencies, I used them exclusively to test the frequency divider. I developed a setup for simulating the gain compression and dynamic range of the amplifier and plotted the differential-mode output voltage as a function of the input signal power. The plots indicate that as long as the clock power level is greater than -10dBm, the peak-to-peak differential-mode output signal is greater than about 200



The divide-by-2 simulation setup in ADS uses the Cadence subcircuit in each of the two "boxes."

mV. This value is large enough to drive the divide-by-2 core, although there may be some signal degradation when the loading of the divide-by-2 core circuit is connected to the rest of the circuit.

I created an output amplifier with a topology similar to that of the input amplifier, using similar techniques. I needed to test the overall performance of the frequency divider, including both amplifiers. Some degradation occurred in the maximum operating frequency when the output amplifier was connected, but I alleviated the problem by increasing the available drive current at the output of the slave latch. I used TAHB to determine the maximum operating frequency and the fundamental output power versus output frequency response of the frequency divider. The divider worked to a high operating frequency, but as stated earlier, the actual operating frequency was not as high, because of parasitic effects that these simulations did not in-

The next step in the design process was

to create a layout of the IC using Cadence. Before submitting a design for fabrication, it must pass an LVS test. You must remove any elements in the schematic, such as voltage sources and current probes that do not exist in the layout. I replaced all the variables used in the component parameter definitions with constants. Because I had little experience with Cadence and the IBM SiGe design kit, I often ran the design-rule checker, to avoid creating a design

with many design-rule violations. Also, I created the layout in three separate parts: the input amplifier, the divider core, and the output amplifier. Each of these parts had to pass an LVS test before I created the final layout. I minimized trace lengths, especially the feedback path from the output of the slave latch to the input of the master latch, and manually checked trace widths to ensure that they were sufficient to satisfy IBM's current-capacity requirements.

The final chip layout was designed to directly match this schematic "layout" (Figure 5). The long horizontal lines in the middle connect the output of the slave latch to the input of the master latch, using deep trench isolation beneath them to minimize capacitive coupling to the substrate.

The completed layout includes the input and output amplifiers, all the bond pads, pattern fill, and substrate contacts. The chip dimensions are 1.1×0.65 mm. The five bond pads at the top are for the positive supply, and the three at the bot-

FOR MORE INFORMATION...

Readers interested in the details of how to set up transient-assisted harmonic-balance simulations can download the ADS 2001 example file, FreqDivider_prj, from http://contact.tm. agilent.com/tmo/eesof/applications/latest.html.

For more on ADS or the

RFIC Dynamic Link to Cadence, visit www.agilent.com/eesof-eda.

For more information on current mirrors, check out chapter four of *Analysis* and *Design of Analog Integrated Circuits*, by Paul R Gray and Robert G Meyer (John Wiley and Sons, Inc, 1993). For more on IBM's SiGe technology and foundry services, visit www-3.ibm.com/chips/services/foundry/offerings/ and for more info about Agilent's RFIC Dynamic Link to Cadence, visit http://contact.tm.agilent.com/tmo/eesof/products/e8970a-a.html.

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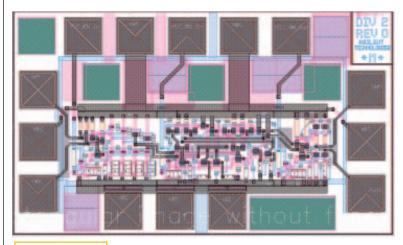


Figure 5

Once the final chip layout is complete, the design is ready for fabrication.

tom are for the negative supply. You can bias the IC with a positive supply, a negative supply, or both. The inputs are at the left (positive signal, positive supply contact, negative signal), and the outputs are at the right.

COMPARISON WITH MEASURED RESULTS

Measurements of the fabricated ICs from IBM revealed performance to be quite consistent. However, at higher frequencies, the simulations—without including any parasitic elements—were overly optimistic. By performing a parasitic extraction from the Cadence layout using the Columbus RF tool and including models for the bond wires used to bias the IC, I was able to achieve close agreement between the simulation and the measurements.

When determining whether there is good agreement, simply comparing the simulated and measured divided signal amplitudes at the fundamental frequencies is insufficient. You need to also compare the waveforms using different input clock frequencies. With a maximum input clock of 12 GHz, the waveforms agree pretty well. At 15 GHz, the shapes of the waveforms still agree, but the measured amplitude is somewhat less than the simulated amplitude. A possible explanation for this situation is that the extraction does not include parasitic coupling to the substrate. At higher frequencies, this coupling has a significant effect, and you should model it.

ADS offers valuable simulation and data-display technology, even when you're designing what could be considered a digital IC. The proposed RFIC de-

sign flow—Cadence for schematic entry and layout, ADS for simulation and data display—does work. But although ideal circuit simulations can provide useful directions to designers, you must include parasitics to accurately predict performance. The IBM SiGe foundry produced ICs with good performance, especially considering that a designer new to this flow used just a single pass through the foundry.

AUTHOR'S BIOGRAPHY

Andy Howard is an applications engineer at Agilent Technologies, where he has worked for 16 years, creating application examples for Agilent's Advanced Design System software. He holds a BS and an MS, both in electrical engineering, from the University of California—Berkeley and has attended intensive courses in Japanese at Cornell University (Ithaca, NY) and Massachusetts Institute of Technology (Cambridge).

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