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Accurate Simulation Models Yield High Efficiency Power Amplifier Design

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Accurate Simulation Models Yield High Efficiency Power Amplifier Design

Sonoko Akamatsu, Charles Baylis, Dr. Larry Dunleavy

Contact: Larry Dunleavy, Dunleavy@eng.usf.edu, (813)974-2574

The design of RF & microwave power amplifiers continues to be somewhat of an art yet to be reduced to a systematic repeatable design practice on a wide-scale basis, despite the many excellent treatments of the subject in the literature, text books (*e.g.* [1]), and a number of courses. The general unavailability of sufficiently accurate and reliable nonlinear models for power transistors has been a major factor in limiting the accuracy of power amplifier (PA) simulation results. Suitable nonlinear models must properly treat the nonlinear and combined DC/AC analysis required for proper power compression and efficiency simulation under varied load and bias conditions. In this paper, an accurate nonlinear transistor model is shown to form the basis for a systematic simulation-based design procedure for a microwave power amplifier. As an illustration of the procedure, a high-efficiency power amplifier was developed with excellent first-pass performance results. This circuit was designed using a nonlinear transistor model and passive component models commercially available from University of South Florida (USF) spin-out company Modelithics, Inc. [2], [3] in combination with Agilent Technologies Advanced Design System software [4]. An 8-Watt power amplifier with 62% efficiency was achieved at 1.3 GHz, without modification of the circuit. This circuit was awarded first place in an IEEE sponsored power amplifier design competition (see related sidebar in this issue).

1. Design Goals and a Simulation-Based Process for Power Amplifier Design

The initial design goals for the power amplifier are shown in Table 1. These goals are thought to be reasonable based upon previously reported achievements in high-efficiency power amplifier design. One push-pull amplifier design detailed in the literature has shown 60.9 percent power-added efficiency at 4.15 GHz with an output power of 28.2 dBm [5], and another push-pull design has been reported to provide 63.8 percent power-added efficiency at 3.55 GHz and 28 dBm output power using harmonic tuning [6]. Such results show that achieving over 50 percent PAE for the targetted single-ended Class AB design should be a reasonable goal.

For the design described herein, a center frequency of 1489 MHz was targeted along with 1-dB compression power (P1dB) goals of 38 dBm output at 25 dBm input power (Pin). The goal was to achieve maximum power-added efficiency (PAE) once the other minimum requirements had been met, and a PAE of over 50% was targeted for Class AB operation. A Fujitsu FLL120MK GaAs FET was selected to achieve these goals. According to its data sheet, this device is capable of 10 W at 2.3 GHz with greater than 40% efficiency [7].

Table 1 Original design goals

Frequency	1489 MHz (1477-1501MHz)
Bandwidth	> 24MHz
P1dB	38dBm
Gain	14dB
Pin	25dBm max
PAE	Maximum (> 50%)

Table 2 shows the systematic design process followed for the developed amplifier. The key to the success of the process was to have suitable models available for all the active and passive components and transmission line structures used. The transistor model provided by Modelithics for the FLL 120MK was an EEHEMT model [4] developed using IV and multiple-bias S-parameter measurements, with the aid of Agilent's IC-CAP extraction software. The model was independently validated at high power with a Maury Microwave ATS load/source pull system. The passive surface mount device (SMD) models for the utilized Coilcraft Air Coil inductors, Toko 0805 Inductors and ATC 0805 capacitors were supplied by Modelithics. The models were developed from S-parameters measured on multiple substrates in combination with accurate effective series resistance (ESR) measurements [2]. These models have as input parameters the nominal component value and substrate properties (including thickness and dielectric constant), allowing for optimization of component values in step 8, while fully addressing parasitic effects. These models were added in Step 6 along with microstrip (MS) transmission line models built-in to ADS, after the initial design was completed using Steps 1 through 5.

Table 2 Design process

STEP 0	Establish Suitable Nonlinear Model
STEP 1	Determine an Optimum Bias Point, and Load/Source Impedances Using Load/Source Pull Simulation
STEP 2	Check S-Parameters and Stability
STEP 3	Design Output Matching Network
STEP 4	Design Input Matching Network
STEP 5	Ideal (Small & Large Signal) Simulation
STEP 6	Accurate Passive SMD models with MS T-Line models (Small and Large Signal Simulation)
STEP 7	Design Bias Networks
STEP 8	Optimize MS T-Line geometries and SMD component values.
STEP 9	Layout (and EM simulation)*
STEP 10	Measurement
STEP 11	Close the Loop (Measured to Simulated Comparisons)

*Post-analysis proved that EM simulation of microstrip geometries is a potentially important step that should be part of Step 9 (See Section 7.)

2. Load pull and Source pull Simulation

Load pull simulations, enabled by the nonlinear transistor model, were used in ADS to select optimum conditions for high efficiency. The optimal load impedance was determined by initially setting the input impedance to a conjugate “gain” match. This was done using a 50 ohm simulation using the aforementioned nonlinear model for the Fujitsu FLL120MK [3]. The load pull simulation results are summarized in Table 3. A source pull simulation was then performed, focusing on high efficiency tuning. Based on iteration of results from load and source pull simulation at several different bias conditions, a bias condition $V_{ds} = 10V$, $V_{gs} = -2.0V$ and an optimum load impedance were selected. These initial simulations indicated that 59.8% PAE was possible with a source impedance of $2.19-j6.25$ and a load impedance of $3.40-j6.48$. A separate harmonic balance (HB) power simulation was performed under the same source/load impedances to confirm the simulation result of PAE=59.8 % and $P_{out}=39.3$ dBm at an input power of 25dBm.

Table 1 Load pull simulation result –freq 1.49GHz (I must have missed: explain that Pdel is defined as maximum power delivered from source to load)

Vds (V)	Vgs (V)	Source	Load (ohms)	Pin (dBm)	PAE (%)	Pdel (dBm)
10	-1.80	1.561-j8.595	3.400-j6.480	25	57.45	39.28
	-2.00	1.650-j8.435			59.11	39.09
	-2.20	1.918-j8.031			60.71	39.01
8	-2.00	1.703-j8.389			61.06	37.53
	-2.20	2.035-j7.830			62.94	37.47
	-2.30	2.287-j7.182			64.21	37.50

Table 2 Source pull simulation result –freq 1.49GHz

Vds (V)	Vgs (V)	Load (ohms)	Source (ohms)	Pin (dBm)	PAE (%)	Pdel (dBm)
10	-2.00	3.400-j6.480	2.189-j6.248	25	59.82	39.29
		3.481-j7.747	2.189-j6.248	27	59.65	40.61
				28	59.22	40.71
10	-2.20	3.400-j6.480	2.189-j6.248	25	59.09	39.06

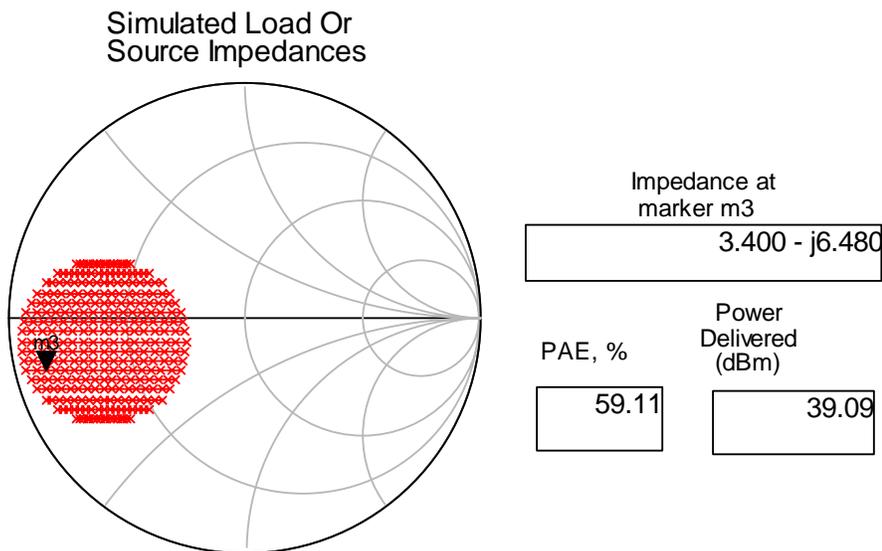


Figure 1 Loadpull simulation in ADS with the input set to 1.650-j8.435 ohms. Input power is 25dBm at 1.49GHz. Vds=10V, Vgs=-2.0V

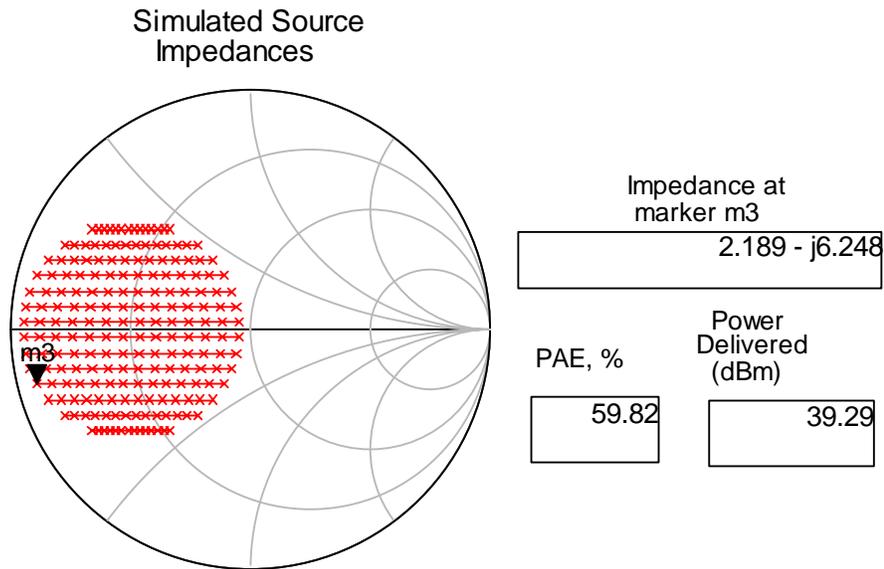


Figure 2 Source pull simulation in ADS with the output set to $3.40-j6.48$ ohms. Input power is 25dBm at 1.49GHz. $V_{ds}=10V$, $V_{gs}=-2.0V$

3. Design and Simulation of Matched Amplifier Using Ideal Components

The ADS DesignGuide tool “Lumped Multi-Element Z-Y Matching Networks” was used to determine lumped element output and input matching networks [4] that transformed 50 ohms into the desired optimum load and source impedance values. Figure 3 through 5 show the ideal matching networks (MNs) and results.

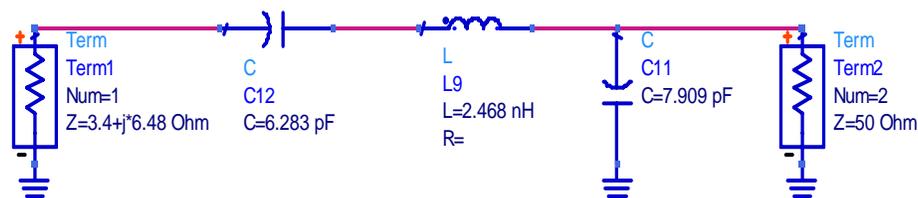


Figure 3 Schematic of ideal MN for matching the load impedance ($3.40+j6.48$ Ohms) to 50 Ohms.

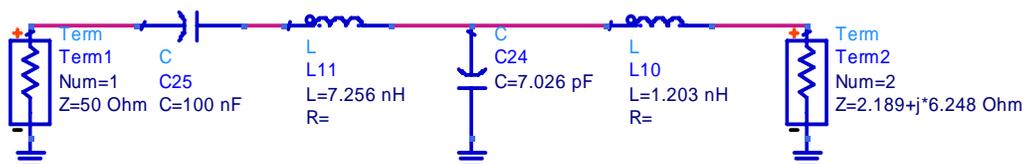
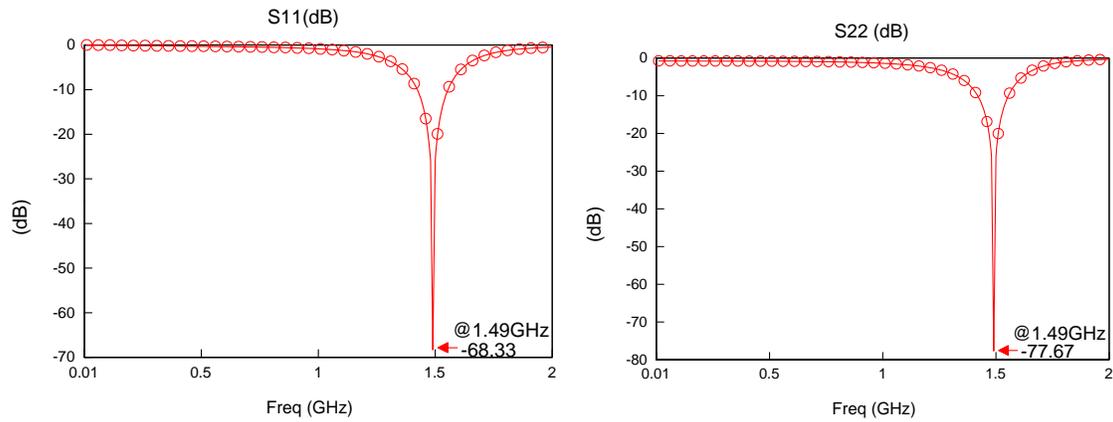


Figure 4 Schematic of ideal MN for matching the source impedance ($2.189+j6.2480$ Ohms) to 50 Ohms.

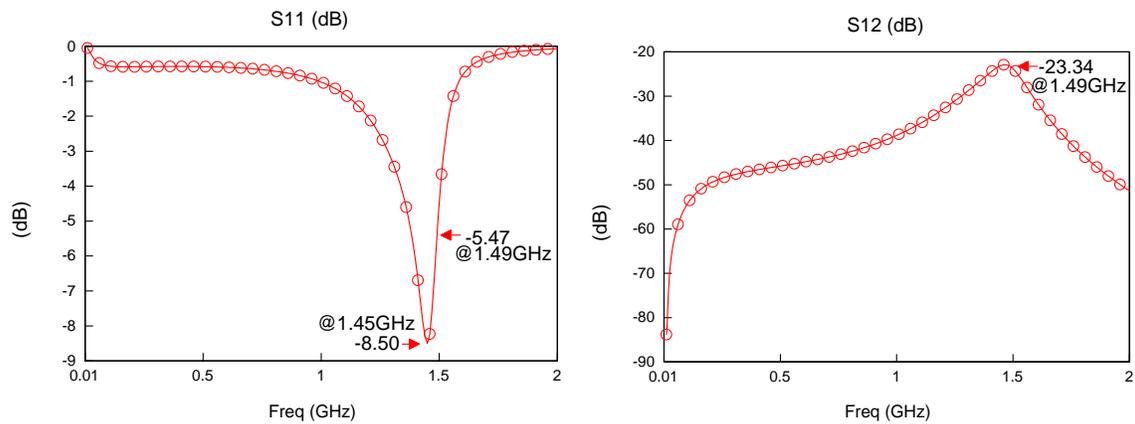


(a) Output MN result

(b) Input MN result

Figure 5 Simulation of the ideal MNs shown schematically (a) in Figure 3 and (b) in Figure 4. These results validate that the narrow-band transformation to the desired input/output matching conditions has been achieved.

Both small signal and large signal simulations were next performed with ideal passive components used to realize the required matching. A 10-V drain-source voltage and a -2.0V gate-source voltage were used for the initial transistor bias. Figure 6 shows the small signal simulations. The result shows 16.2 dB Gain at 1.49GHz, which satisfies the design goal in Table 1.



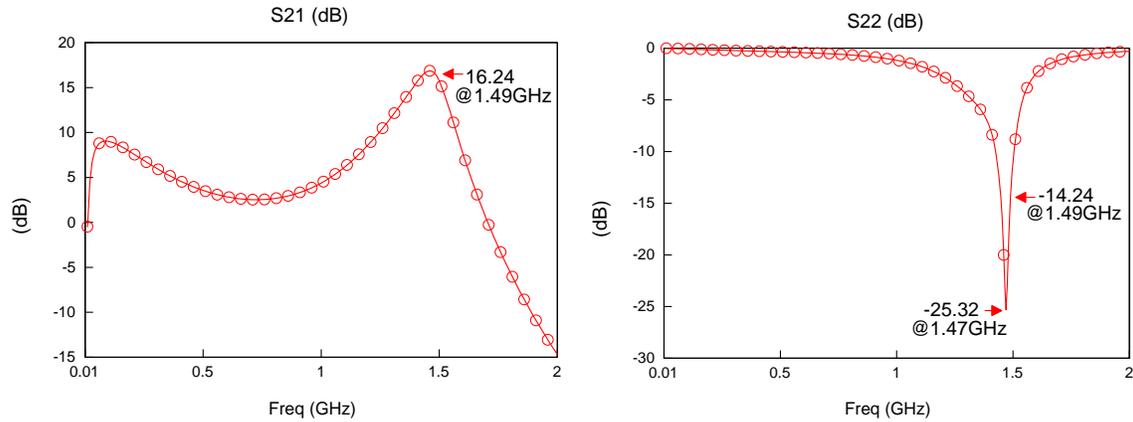


Figure 6 Class AB amplifier results using ideal lumped elements for matching. Results show good gain and impedance matching at the originally targeted 1.49 GHz.

Large signal simulation was performed using a template under the “DesignGuide” from the ADS schematic window. Figure 7 shows the ideal large signal simulation schematic. The result in Figure 8 shows 62.2% PAE, output power 39.38dBm with input power 25dBm. These results are slightly better than that achieved under the initial load/source pull simulation.

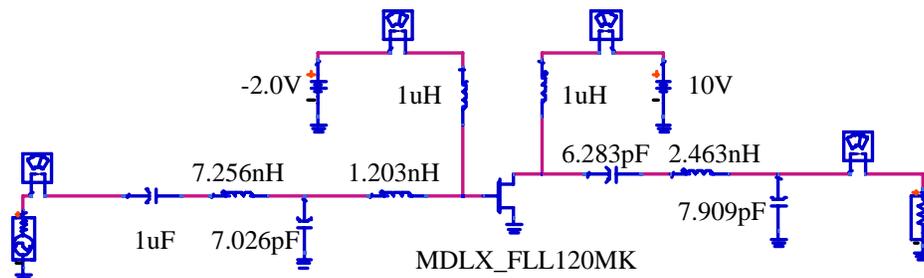


Figure 7 Ideal large signal simulation schematic used for harmonic balance simulations in ADS. This network combines the ideal lumped matching networks from Figures 3 and 4 with the non-linear transistor model and ideal bias T network and was used to generate the large-signal simulation results of Figure 8.

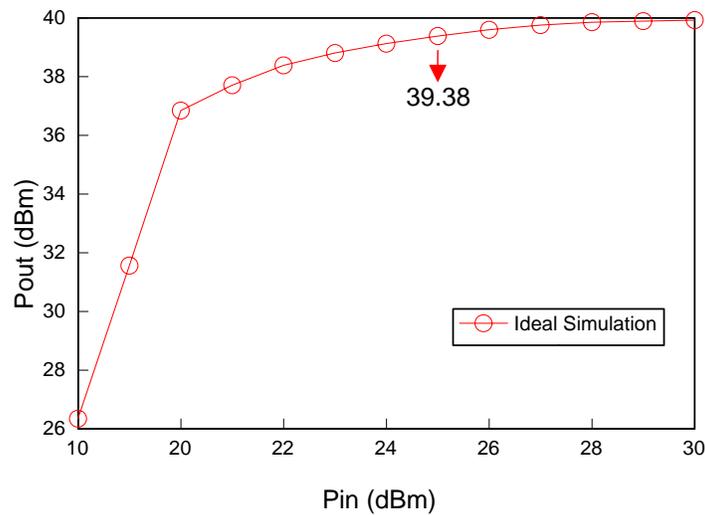
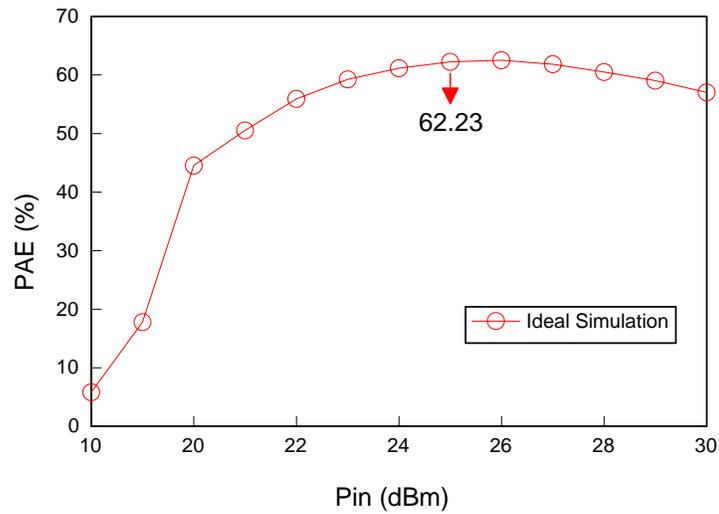


Figure 8 Large signal simulation results for transistor with ideal matching networks at a bias condition of 10V, V_{ds} and -2 V, V_{gs} .

The substrate-scalable and part-value scalable SMD models were next combined with transmission line models using built-in ADS elements, microstrip line (MLIN), microstrip step (MSTEP) and Microstrip TEE (MTEE). The 50-ohm width for microstrip line was calculated by the ADS transmission line calculator, LineCalc, to be 2.86mm. These calculations were based on 59mil thick FR4 substrate information ($\epsilon_r = 4.3$).

4. Optimization Using Scalable Parasitic Models

Optimization of component values and microstrip line geometries is necessary to achieve the required performance in a fabricated amplifier. Optimizations and goals were selected under the component pallet list of ADS. The input and output matching networks were separately optimized based on the optimum load and source impedances (see Figures 1 and 2). The width and length of the microstrip transmission lines and SMD component values were both tuned to achieve the required impedances.

Figure 9-12 show the optimized schematics for the output and input matching networks. Both small signal and large signal simulations were performed after optimization. Simulated results indicated 56% PAE at 38.6dBm output power was achievable at 25dBm input power. This corresponds to 14.9dB small signal gain for these simulations that were performed at $V_{ds}=10V$, $V_{gs}=-2.0V$ condition. (Further on, we'll see that some adjustment of bias condition will lead to even better efficiency on the bench.) Layouts were then generated automatically from the schematic using ADS, producing the layouts of Figures 11 and 12. These layouts were used directly to fabricate the circuit using an LPKF milling machine at the USF. Figure 13 and 14 show the nonlinear simulations of the optimized design.

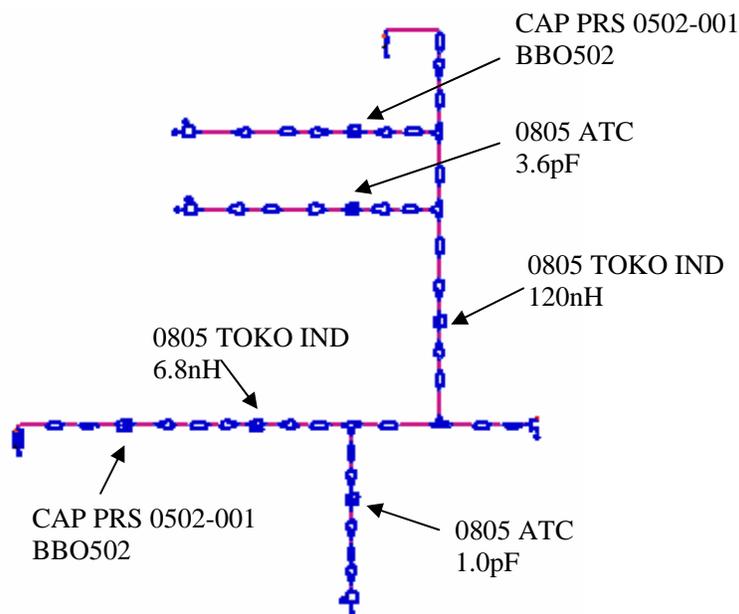


Figure 9 Optimized input schematic (of what?--be more descriptive so that the reader can just scan the figures and get a nearly complete idea of everything you did)

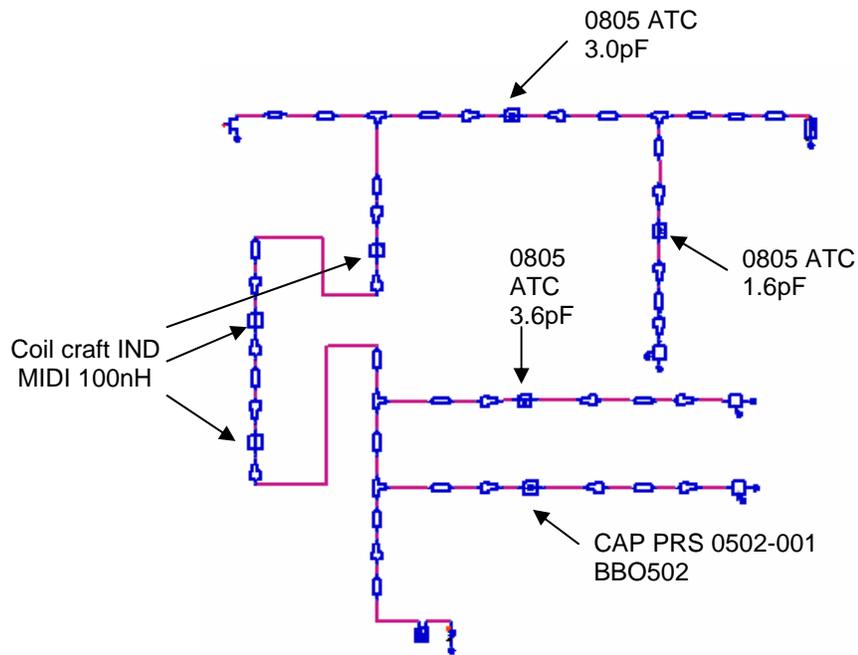


Figure 10 Optimized output schematic (more descriptive)

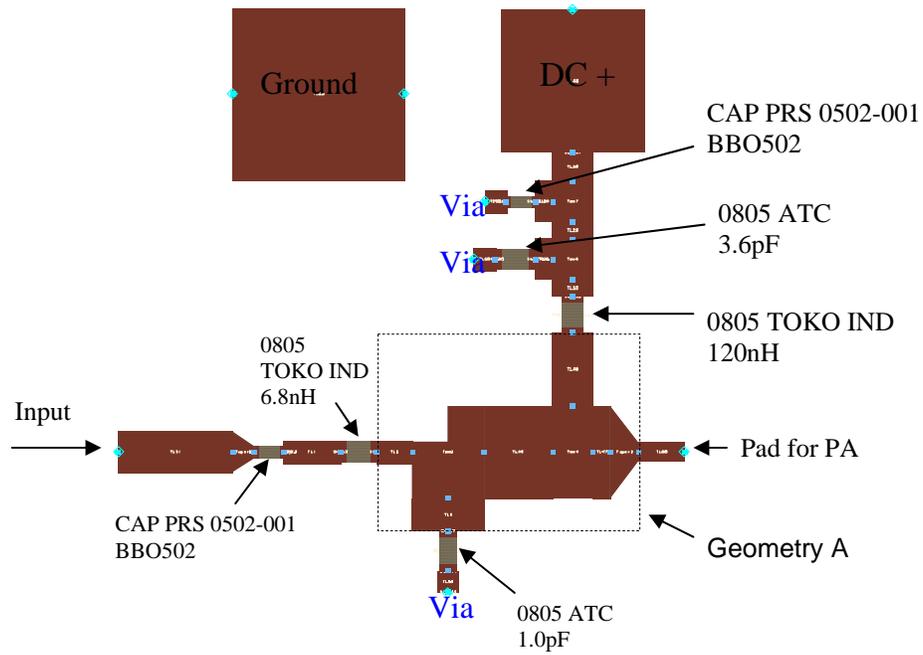


Figure 11 Layout (generated automatically in ADS) of the input MN whose schematic is shown in Figure 9

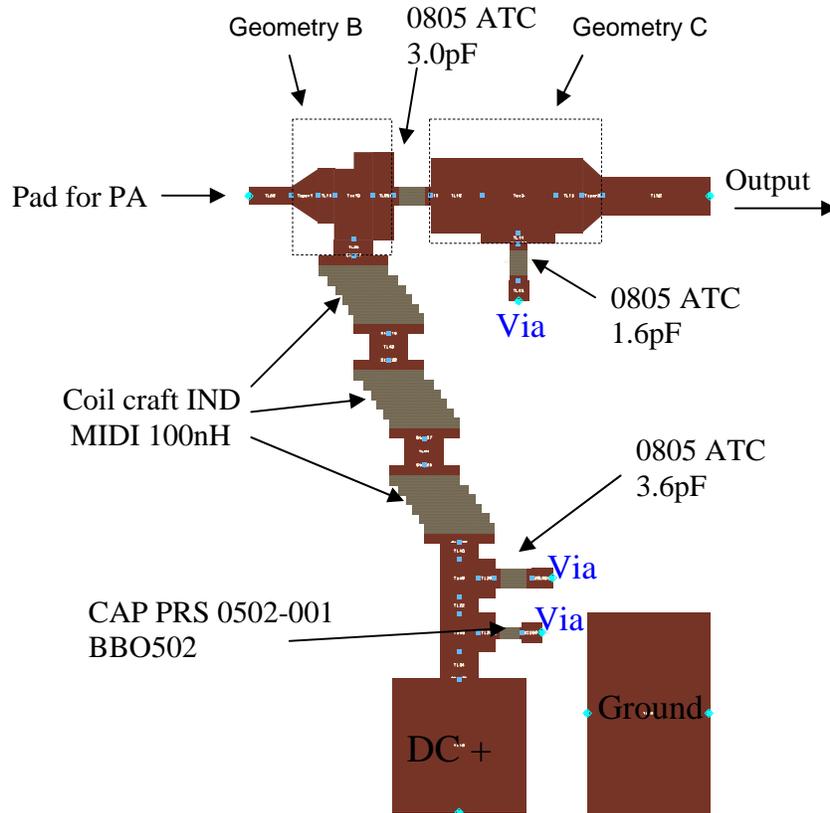
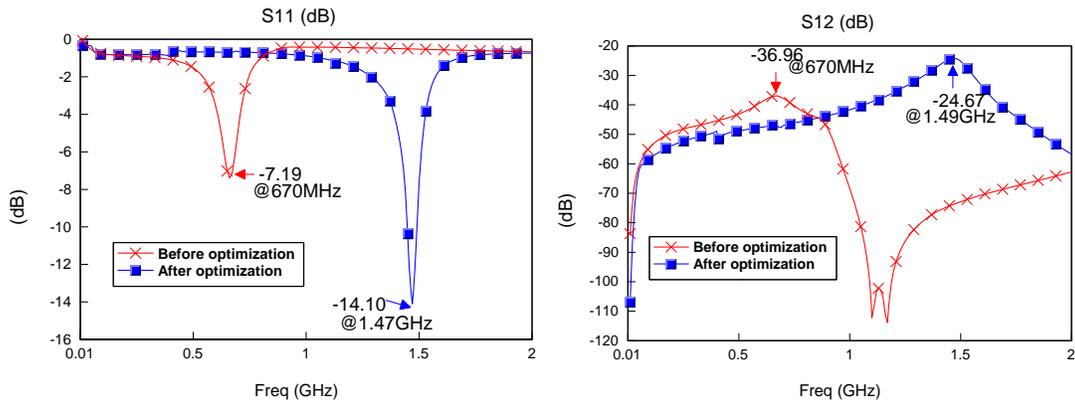


Figure 12 Layout (generated automatically in ADS) of the output MN whose schematic is shown in Figure 9



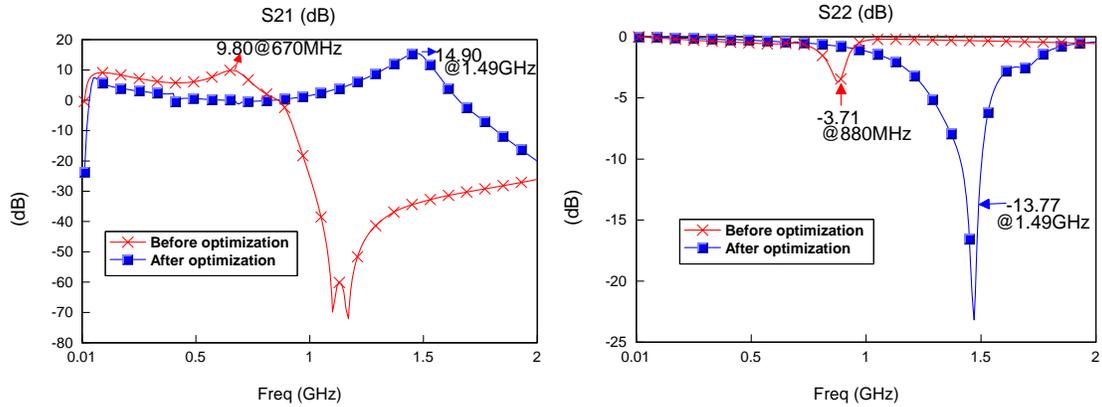


Figure 13 Small signal simulation results using passive SMD models along with ADS microstrip models before and after optimization

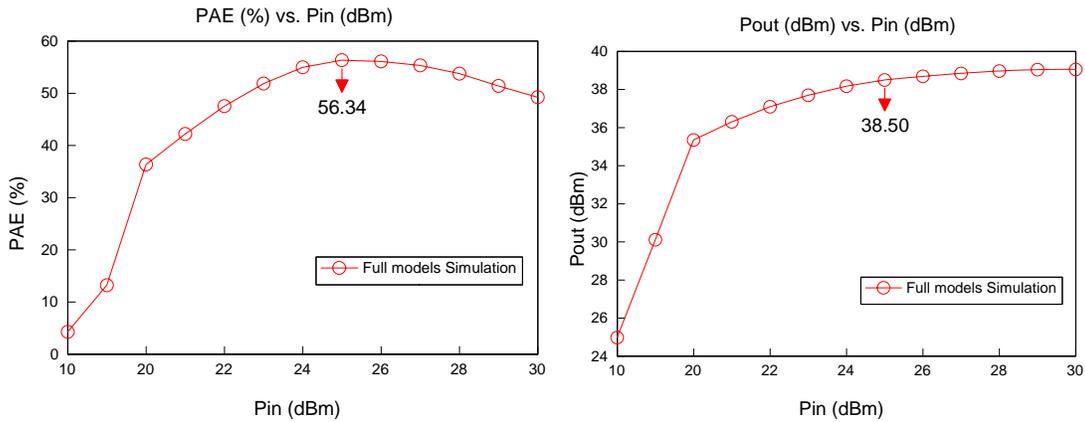


Figure 14 Large signal simulation results for optimized circuit

5. Measurement Results

The completed assembled class AB power amplifier was shown in Figure 15. Metal epoxy was used to create the via grounding and connection between the circuit board and heat sink. The small signal and large signal measurement results showed the peak gain frequency was shifted down around 200MHz. Further analysis is shown in the later section that fully explain this shift, but all other goals, including power added efficiency, the required power level and gain were achieved without bench tuning.

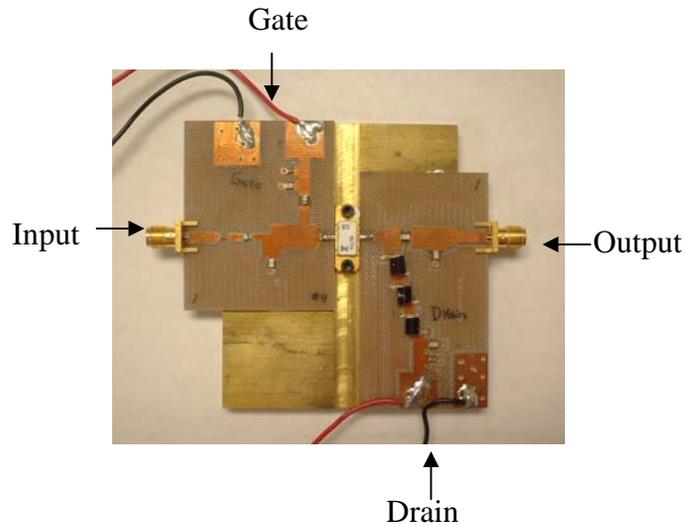


Figure 15 Power amplifier assembled from the fabricated input and output circuits whose layouts were shown in Figures 11 and 12, respectively.

S-parameters were measured using an Anritsu 37397C Vector Network Analyzer calibrated with a K-connector SOLT calibration kit. The S-parameter results showed 13.6 dB gain at 1.29 GHz. *As explained below in Section 6, the frequency shift (to 1.29 GHz) observed for the measured amplifier as compared to the initial design center frequency was found to be due to a misinterpretation of the reference plane location on the transistor model. Correcting for this effect produced excellent simulation to modeled agreement for all parameters. (See Section 7)*

Figure 16 shows the measurement test configuration used at USF for power measurements. A Maury Microwave Automatic Tuner System (ATS) was used to facilitate the power sweep measurement. In this nonlinear test, 54.5% efficiency was achieved at 25dBm input power (10V V_{ds}, -2.2V V_{gs}), however the voltage drop due to the drain bias cable was not taken into account in this initial measurement. By using an adjusted bias condition, V_{ds}, an efficiency of 61.7% was measured at the 2005 IEEE MTT-S Symposium in conjunction with the power amplifier design competition.

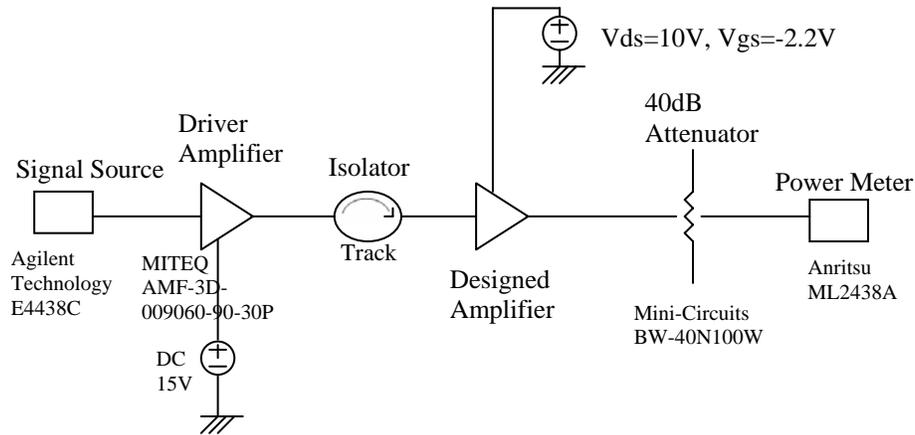


Figure 16 The USF power amplifier measurement test configuration

6. Closing the loop – Post Measurement Analysis

A careful analysis was performed to understand the 200MHz frequency shift observed in the measured vs. simulated amplifier. Exploration included careful examining of via hole models and more accurate representation of microstrip matching elements using electromagnetic (EM) analysis, however, a careful review of the interface between the microstrip circuit and the transistor revealed that the main problem was a misinterpretation of the reference plane location on the transistor model. The modeled transistor measurements were made with the device embedded between small sections of 50 ohm line on a 10mil GTEK FR4 substrate ($\epsilon_r=3.8$). The amplifier was fabricated on a 59mil FR4 substrate ($\epsilon_r=4.3$).

The result using the corrected schematic, with the 10mil GTEK line sections properly de-embedded, shows the resonant frequency shifted down to 1.33GHz. Further improvement in measured to simulated agreement was achieved with the aid of EM analysis using Sonnet EM simulator [8]. The EM analysis S-parameter results of geometry A, B, C shown in Figure 12 and 13 were implemented into the ADS simulation schematic. Combining the EM simulation for these microstrip portions of the input and output matching sections, centered the simulated gain at 1.29GHz. Figure 17 shows the comparison result including the EM simulation.

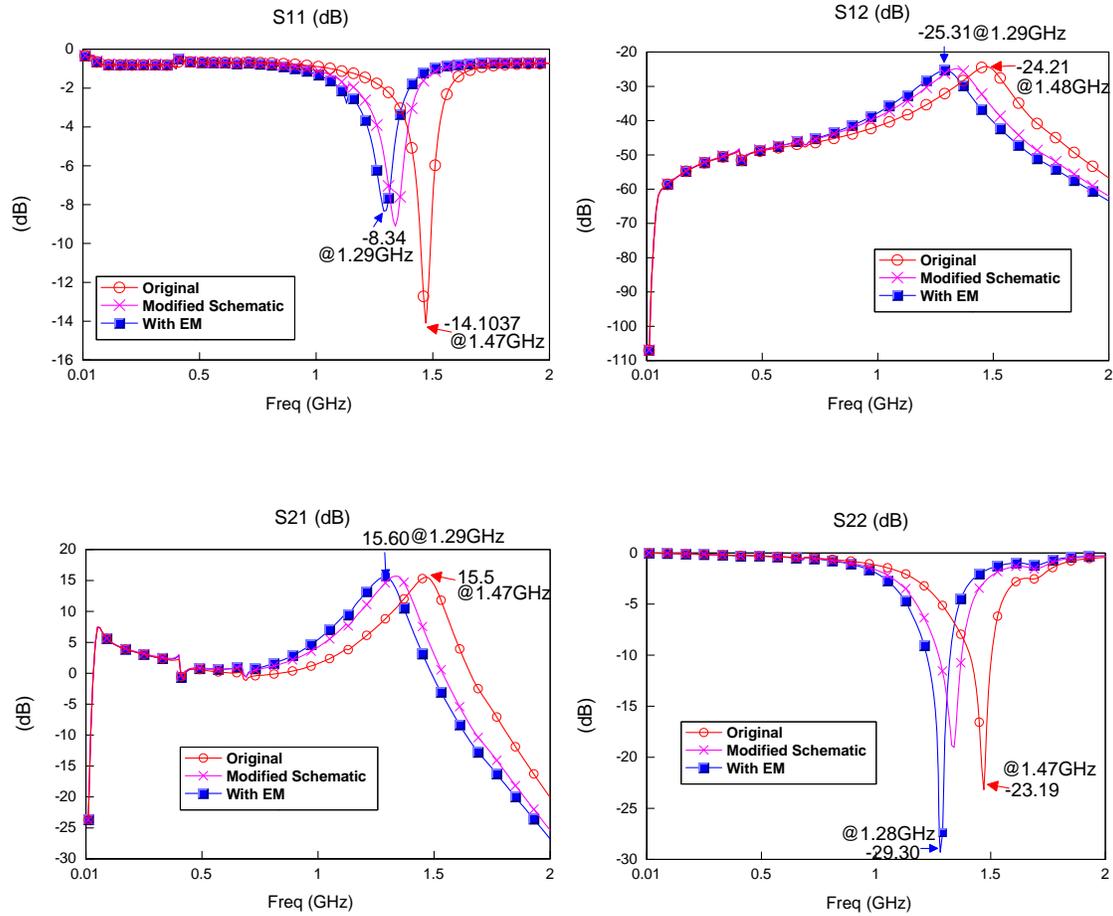


Figure 17 S parameter result comparison including the EM simulation of the amplifier shown in Figure 15. (Bias condition is 10V, Vds and -2.0 V, Vgs).

7. Final Comparisons –Simulation and Measurement Converge at Multiple Bias Conditions

Figure 18, 19 and 20 show the comparison result between the measurement and simulation using the original design bias condition (10V Vds, -2.0V Vgs). The small signal comparison in Figure 18 shows good agreement is seen for all four S-parameter magnitudes. The gain is slightly lower which could in part be due to the fact that connector loss was not de-embedded from the measurements and there could be some radiation loss due to the microstrip elements. Also, the via holes were epoxy filled, vs. whereas the models used were for plated through holes.

Figure 20 shows excellent measured to simulated agreement for the power and efficiency. Figure 21 and 22 show 59% PAE is achieved for both simulation and measurement, with a bias condition closer to that used at the competition. Excellent agreement was again observed between and simulated large-signal results. The difference between the 62% observed at the competition and this result is attributed to differences in

the test setup and possible differences in the exact bias condition achieved at the device terminals.

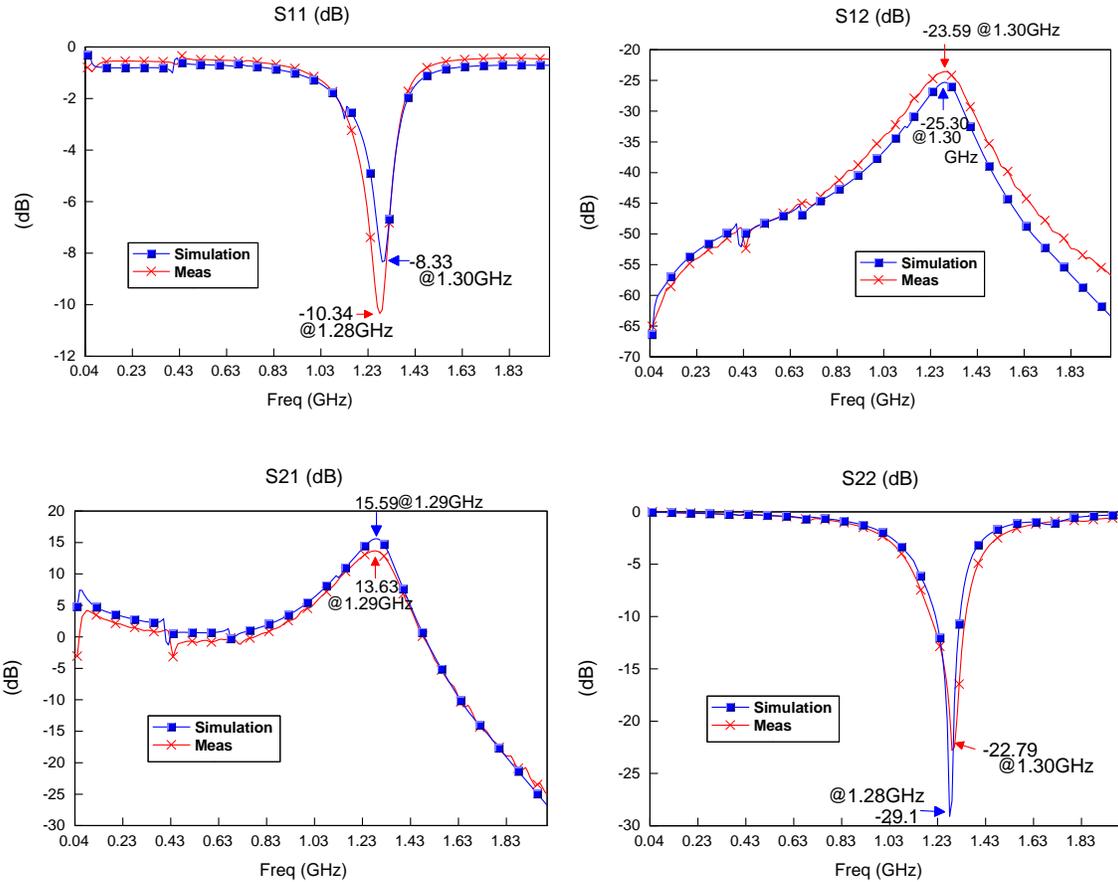


Figure 18 S parameter result comparison for amplifier in Figure 15 at bias of 10V Vds, -2.0V Vgs (700 mA Ids)

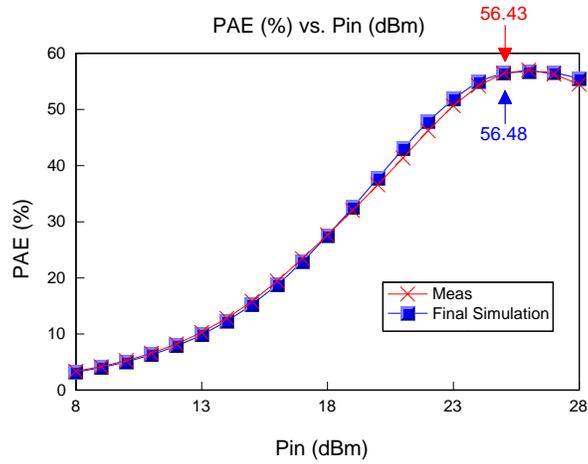


Figure 19 Measured PAE Result for amplifier in Figure 15 at bias points of $-10V$ V_{ds} , $-2.0V$ V_{gs}

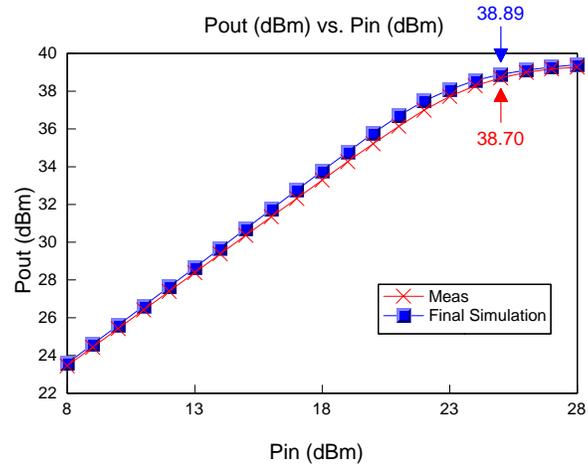


Figure 20 Pout vs. Pin Measurement Result for amplifier in Figure 15 at biases of $-10V$ V_{ds} , $-2.0V$ V_{gs}

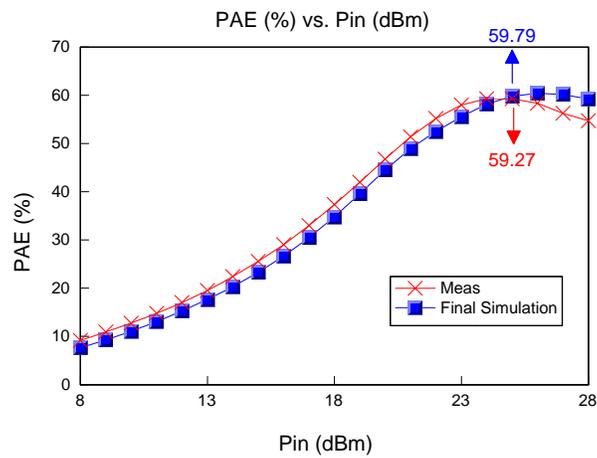


Figure 21 Measured PAE for amplifier at $-8V$ V_{ds} , $-2.2V$ V_{gs}

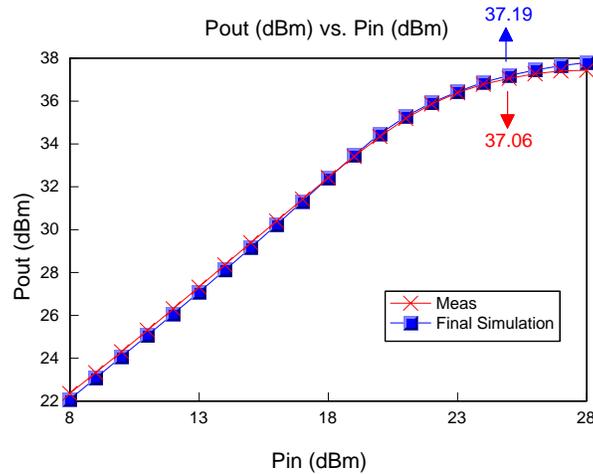


Figure 22 Measured Pout vs. Pin for amplifier at -8V Vds, -2.2V Vgs

8. Summary

A Class AB Power Amplifier application circuit targeting 1.5 GHz was introduced and benchmarked a systematic design procedure enabled by use of high accuracy models for active and passive circuit elements. A Fujitsu FLL120MK GaAs FET device was chosen to satisfy the power, efficiency and gain design goals. Loadpull and sourcepull simulations by were performed using a customized non-linear model for the transistor within Agilent Advanced Design System (ADS) to find an optimum bias condition, along with a load and source impedance that enabled high efficiency at the required 25 dBm power input level. The nonlinear transistor model and passive surface mount device models from Modelithics were used, along with built-in microstrip line models in ADS to accomplish the design optimization and simulation. 60 % Power Added Efficiency (PAE) and 37.06 dBm output power with input power 25dBm were obtained at 1.29GHz. This measurement result showed that the frequency shifted around 200MHz. A misinterpretation of the transistor model reference plane location caused the frequency shift. After including the corrected schematic and adding EM simulation for the microstrip matching sections, excellent agreement was obtained between the simulation and measurement at the two different bias conditions analyzed. This work sets the stage for a more efficient simulation-based design flow for PA design that relies on accurate models. It also underlies the importance of attention to detail in setting up simulations and proper use of the various simulation, measurement and model extraction tools available.

9. Acknowledgement

The authors would like to acknowledge Bill Clausen, John Capwell and Rick Connick of Modelithics for their various suggestions and assistance with the use of the supplied models. We would also like to thank Alberto Rodriguez, Jiang Liu, and Nigel Brown at

the University of South Florida WAMI Center for their support in the fabrication and testing aspect of the project.

Reference

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Student High Efficiency Power Amplifier Design Competition

To promote student interest in microwave engineering the Microwave Theory and Techniques High Power Microwave Components Committee (MTT-5) is sponsoring a new competition. Contestants are required to design and construct a microwave power amplifier (PA) with the highest possible efficiency. The first competition took place at IMS2005. Students and graduate students from all educational establishments were encouraged to enter. The PA had to operate at a frequency above 1 GHz but less than 20 GHz, and have an output power level of at least 5 watts, but less than 100 watts into a 50 ohm load. The winning entry was the PA that demonstrated the highest power added efficiency (PAE) during testing at IMS2005. The contest took place in the Interactive Forum (IF) area, and the results were on display during IF session hours. The winner received a prize of \$1,000 and was invited to submit a paper describing the design for the MTT Microwaves Magazine.

The 2005 competition attracted entries from five universities (Ecole Polytechnique de Montréal; Sogang University, Korea; University of California, Davis; University of California, San Diego; and University of South Florida) plus a sixth demonstration only entry (Postech University, Korea). The PAs were fabricated and tested prior to the contest and carried to IMS2005 by team members. The test equipment used to evaluate the PAs was provided by Agilent Technologies and centered about a PNA Vector Network Analyzer programmed to display PAE. Special thanks must be given to the Agilent volunteers headed by Ken Wong for their assistance with the measurements. Each team was given time to optimize their amplifiers for the best efficiency. Most of the PAs operated near the minimum frequency of 1 GHz where high efficiency should most easily be achieved. The winning entry came from the University of South Florida and was designed by Sonoko Akamatsu advised by Professor Larry Dunleavy. It produced an efficiency of 61.7% and operated near 1.5 GHz. The highest measured efficiency of 69.2% was actually produced by Postech's PA, but it was not part of the official competition. The entry from Ecole Polytechnique de Montréal, which used a Doherty design and achieved a PAE 50.4% is also worthy of note. Its unique design allowed this efficiency to be produced at a higher power backoff with higher linearity than the other entries.

MTT-5 will be again sponsoring a Student High Efficiency Power Amplifier Design Competition at IMS2006. The rules are essentially the same as in 2005.

PA Competition rules:

1. The power amplifier (PA) design may use any type of technology, but must be the result of student effort both in the amplifier design and fabrication.
2. The PA mechanical design should allow for internal inspection of all relevant components and circuit elements. The RF ports should be standard coaxial connectors, type N or SMA.
3. The PA must operate at a frequency of greater than 1 GHz but less than 20 GHz, and have an output power level of at least 5 watts, but less than 100 watts.
4. All amplifiers should require less than 25 dBm of input power to reach the output level required for maximum efficiency.
5. The PA should require no more than two external dc supply voltages for operation.
6. Amplifier entries should be submitted with measured data, including dc supply requirements, frequency, RF drive and output power, and PAE. PAE will be defined as $(RF_{out} - RF_{in})/dc$. Measurements will be under CW operation at room ambient conditions into a 50 ohm load. Only the power at the fundamental CW frequency will be included in the measurement of output power.
7. The decision will be based solely on the amplifier's power added efficiency measured during official testing at IMS2006. The judges reserve the right to give favorable consideration for special awards to performance characteristics of special merit, such as higher bandwidth or exceptional workmanship. The decision of the judges will be final.
8. Contestants must notify the MTT-5 committee by e-mailing to Kiki Ikossi ikossi@ieee.org of their intention to compete in the contest before April 1, 2006. This notification should include information on the University or educational affiliation of the entry, the faculty advisor and the PA's approximate power level, dc voltage requirements and frequency of operation. (Questions about the contest can also be addressed Kiki Ikossi.)

The “Real world” (Nonlinear)Time-Line for the USF Design Entry

Jan-Mar

Professor encouragement to first author to enter contest
Student performs some preliminary work and information gathering

Apr

Entry in the MTT-5 IMS PA design competition (Apr6)
Investigated Class E and AB designs
Started Class AB design

May

Worked on the simulation process for a high efficiency design meeting power/gain goals

June(schedule compression!)

(June 1) Panic sets in
(June 2-3) Preliminary design/ layout completed
(June 4-8) Simulation iterations/optimizations continue.
(June 9) Simulation and layout finalized.
(Jun 10-11) Board fabrication
(Jun12) Assembly
(Jun12, night) Measurement (grounding problem)
(Jun13, morning) Redo metal epoxy between heat sink and substrate
(Jun13, afternoon) Measurement
(Jun13, night) Prepared presentation
(Jun14, morning) PA brought to the competition by the second author
(Jun14, afternoon) Competition

July

Start 1st paper draft

July/August

Post measurement analysis –“closed the loop”

September

Finalize and submit paper

Advisor (3rd author) comment: As a student project, and the most complete nonlinear simulation/circuit fabrication exercise of its kind yet done at USF, the systematic design procedure proposed in the paper was not in place at the outset. Now that it has been benchmarked, we expect a much more efficient design flow for future PA design projects, with the caveat that the importance of attention to details cannot be overemphasized.

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