

DDR Probing for Physical Layer and Functional Testing

Tutorial

Probing is the key to accessing signals and validating your designs. Although you may normally probe at signal vias or designed-in probe points, for DDR these do not always provide good signal integrity. Furthermore the Joint Electronic Devices Engineering Council (JEDEC) specification requires compliance at the hard-to-reach Fine Ball-Grid Array (FBGA) package ballout on the Dynamic Random Access Memory (DRAM) chip.

When you are using an oscilloscope to perform parametric characterization, you must consider the impact of your probes on the DDR signals. Probing can generate a significant impact on signal integrity, including slowing of the signal edge rate, signal distortion, ringing and other undesirable effects. These impacts become especially critical when you are characterizing a new DDR design. You cannot predict the design performance, so you need complete confidence that probing is telling you exactly how your signal is behaving.

The main consideration for your probing system is flatness of the frequency response. Probing should equally amplify the various spectral components of your signal. A frequency response with bumps can over-attenuate or amplify frequency components, creating pre- or overshoot conditions and even ringing of the waveform. In addition, you should use adequate bandwidth but no more, so that the high-frequency noise components from the oscilloscope and probe are not coupled into the measurement.

Probing location can present challenges

Probing directly at the 0.8-millimeter DDR BGA ball-pitch package is difficult since: the signals are hidden beneath it. The next best location to probe is at the signal vias on the back of the circuit board, because they are located closest to the DRAM ballout. But if components are laid out on both sides of the circuit board, no signal vias will be available.

Probing must then be done at other locations: the signal trace or surface mount components, such as the termination resistors and capacitors. Although this may seem straightforward, signal integrity could be compromised by probing here. First, probing at these locations often causes signal reflection, resulting in non-monotonic edges, overshoot, ringing and other issues. Rather than seeing true signal performance, you see a signal that includes the effect of the reflection at the components. This can cause errors on slew-rate and setup and hold-time measurements.



In addition, probing at the trace or component can create other problems. The time required for the signals to travel to the probing location may vary, resulting in timing skew. This, in turn, causes signal skew, due to incorrect timing information.

Two types of timing skew can affect your signals. In the first type, intra-timing skew, the positive and negative pair of a differential signal, such as the clock, are not aligned when you probe them. Intra-timing skew creates false measurement errors, such as duty cycle distortion and crossing point offset, even though the signal is fine. In the second type, inter-timing skew, two different signals, such as the clock and address signals, are not aligned. Again, the setup or hold-time measurement between the signals might be misinterpreted as a violation.

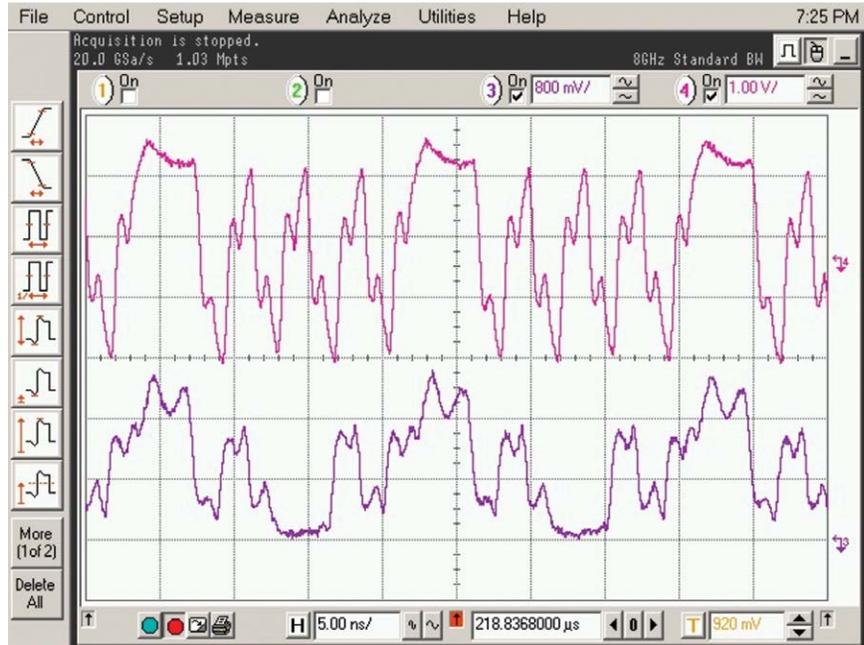


Figure 1. Probing at mid-bus creates artifacts on the measured waveform such as non-monotonic edge and signal ringing that do not occur if the signal is probed at the BGA package.

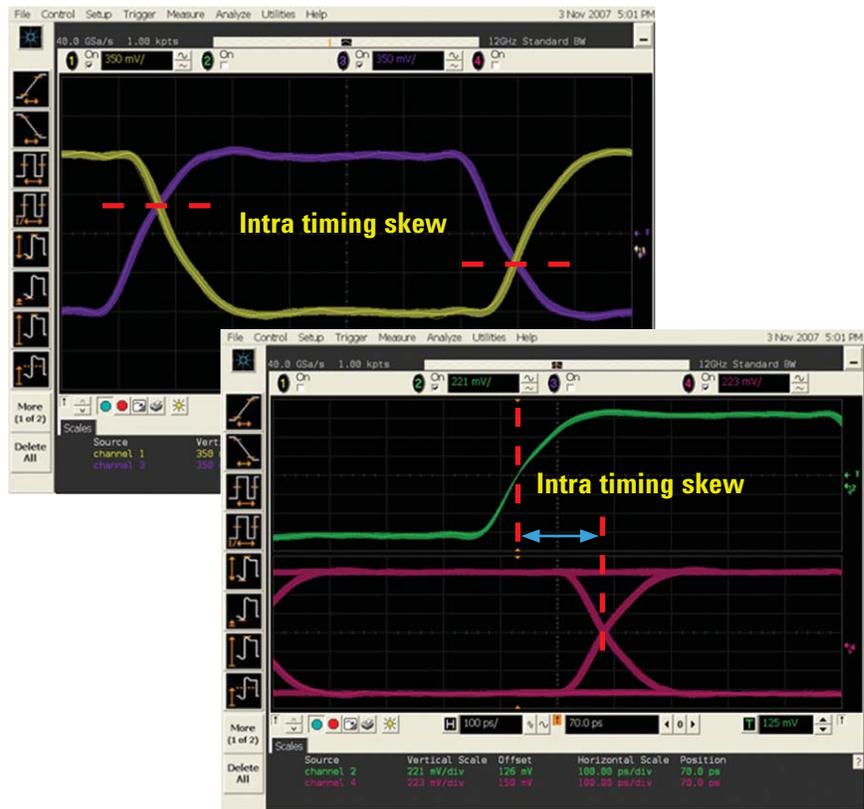


Figure 2. Probing at the wrong locations can result in measurement errors due to intra- and inter-timing skew.

Although some engineers choose to lay out a probing footprint on the circuit board, not all final product designs allow room for a footprint. Many engineers end up laying out the product on a reference design. In this case, much of the characterization work done does not correlate well with the final released product because the layout of the signal traces and components is different. Moreover, you still face a critical issue: How can you troubleshoot a problem on the final released product? This is a primary concern many product designers face.

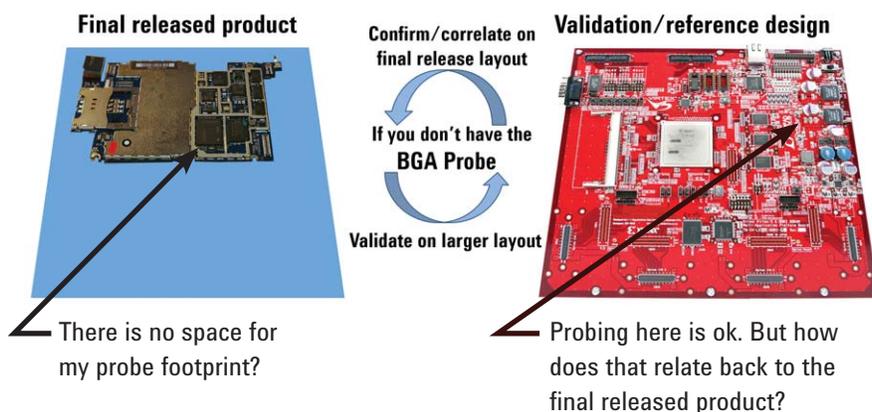


Figure 3. Probing on a reference design may not translate to the final product and leaves open how to troubleshoot a problem in the released device.

Solving probing challenges with the BGA probe adapter

To optimize DDR probing, you may need specialized tools. One such tool is the BGA probe adapter, a thin fixture that can be attached between the DRAM chip and circuit board with a compatible footprint on the top and bottom side. The signals at the DRAM ballout are then routed to the top side of the BGA probe adapter, so the oscilloscope and logic analyzer probes can access them. This method provides a direct signal access point to the DRAM ballout for true compliance with the DDR specification. Since it's compatible with oscilloscopes and logic analyzers, you can perform parametric and functional measurements with the same BGA probe.

The traces on the BGA probe adapter are the same length, eliminating skew between the signals. Embedded or buried resistors placed near the signals inside the BGA probe adapter ensure probe loading effect does not interfere with the DDR signals. The adaptor minimizes the capacitive loading of the stubs and probe heads, effectively preserving the high-speed DDR interface operation. Furthermore, the waveforms obtained through such probing will be closest to the real signal performance.

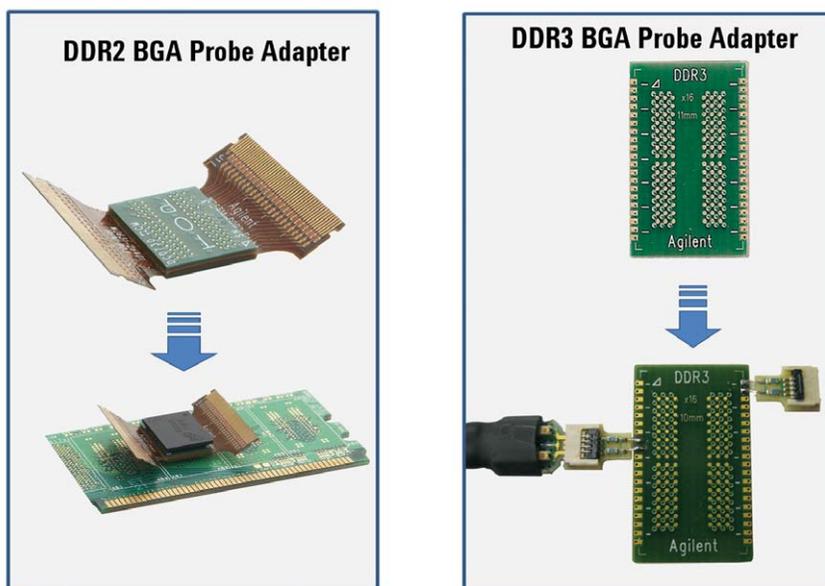


Figure 4. DDR2 and DDR3 BGA probe adapters provide a direct signal access point to the DRAM ballout for compliance with the JEDEC specifications.

During signal probing, you need to use adequate bandwidth to ensure good signal integrity measurements – but no more. For DDR2, you may need up to 4 GHz; for DDR3, up to 6 GHz. Because the signals are susceptible to noise, however, limiting bandwidth will help ensure the measurement is not affected by the oscilloscope’s noise. Agilent Infiniium Series oscilloscopes offer bandwidth reduction features to provide just sufficient bandwidth for the most accurate and repeatable measurements.

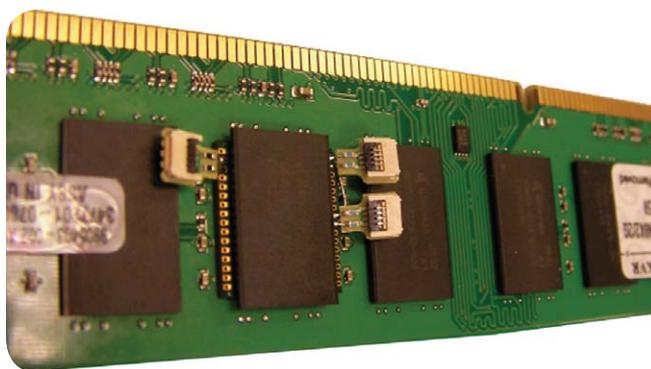


Figure 5. Embedded resistors in the BGA probes isolate probe loading from the signal to maintain signal integrity

In addition, probe loading must still be taken into consideration. A good indicator of the loading is its capacitive rating. A probe tip is a complex microwave circuit, which means that it inherits capacitive loading effect at the probe lead wire. If you select a probe with a large capacitive loading, it can slow down the edge of the signal or, worse still, change the true characteristics of the waveforms. Some of today’s state-of-the-art differential active probes offer up to 13 GHz of measurement bandwidth with less than 0.21 pF of capacitive loading, which is highly recommended for DDR signal probing.



Figure 6. InfiniiMax probes offer low capacitive loading for DDR signal probing

Other probing alternatives include a design-in probing method with a soft-touch, connectorless footprint. These probes enable easy access to chip-to-chip links. For DIMM or SODIMM testing where a slot connector is available, a slot interposer would be a preferred method for easy access to a full memory bus in a DIMM or SODIMM slot.

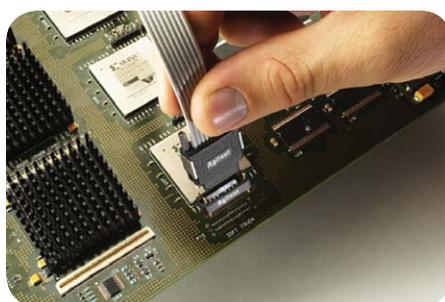


Figure 7. Design in the soft touch connectorless footprint to capture chip-to-chip activity

By selecting the right probe for DDR validation, probing in the right location and following a few key recommendations, you can ensure accurate repeatable measurements that give you a clear view of signal behavior and confidence in your designs.

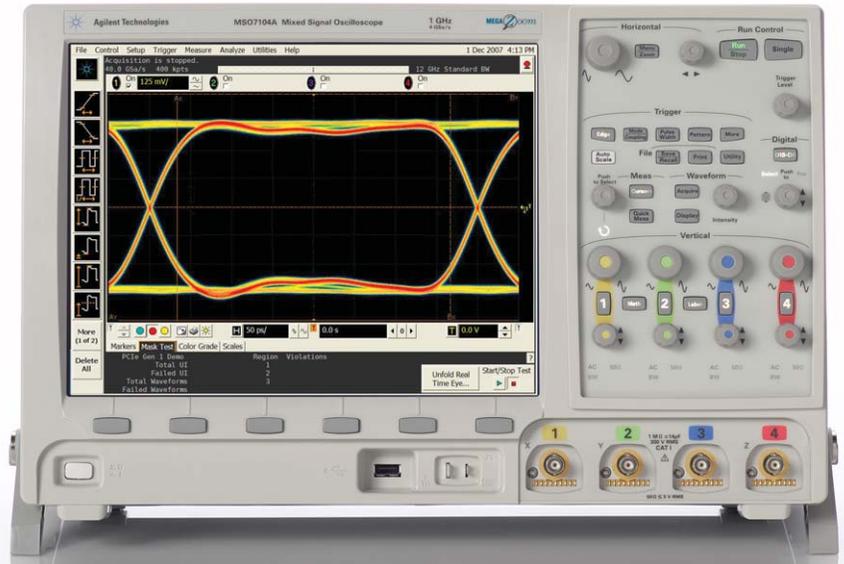


Figure 8. To verify the performance of your probing system, make sure the signals measured through the probe track closely with the surface mount assembly direct connection for maximum measurement accuracy.

Publication title	Publication type	Publication number
<i>DDR Memory Overview, Development Cycle and Challenges</i>	Tutorial	5990-3180EN
<i>DDR Design and Verification through Simulation</i>	Tutorial	5990-3317EN
<i>Debugging Signal Integrity and Protocol Layers on DDR Designs</i>	Tutorial	5990-3189EN
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