

Ensuring Compliance and Interoperability in DDR Designs

Tutorial

Automating compliance measurements

The Joint Electronic Devices Engineering Council (JEDEC) specification requires a large number of test parameters to be verified for DDR compliance – a time-consuming exercise if you make the measurements manually. In addition to characterizing every test parameter, you must record the measurements and format them into a test report. To improve productivity, engineers need a way to automate measurements.

You can reduce the amount of time and effort spent characterizing your device against the JEDEC specification with automated DDR compliance test applications for oscilloscopes and logic analyzers. Using automated routines, you can repeat measurements of every test parameter many times to analyze the signal thoroughly and provide complete statistical results. You can also acquire screen captures of worst-case results. Many applications automatically generate comprehensive test reports for archiving or sharing. (See Figure 1.)



Figure 1. Agilent DDR compliance software provides a familiar and user-friendly interface to streamline test, debug and characterization of DDR designs.



For example, Agilent's DDR compliance test software lets you quickly perform automated measurements for low power DDR, DDR1, DDR2 and DDR3 specifications, review pass, fail and margin analysis results summarized in an HTML report, and check acquired data for protocol and timing violations. The analysis tool also executes several performance measurements.



Figure 2. Quickly perform automated measurements for low power DDR and DDR1, 2 and 3 specifications.

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Figure 3. Review pass, fail and margin analysis results summarized in HTML format.



Figure 4. Check acquired data for protocol and timing violations. The analysis tool also executes several performance measurements.

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Figure 5. Timing analysis to detect data width that doesn't match specification.

DDR Compliance Test Features and Capabilities

What features and capabilities will help you be the most productive when testing your devices for compliance with the JEDEC specification? Here's a checklist:

- Wizard-based user interface for quick setup, configuration and testing
- Automated clock, electrical and timing measurements based on JEDEC specifications
- Automated eye-diagram analysis with user-configurable mask testing
- Automated derating table analysis based on signal slew rate for setup and hold time measurements
- Multiple RANK testing built in to the application
- User-customizable speed for testing embedded design

- User-configurable signal threshold settings (for example: Vref, Vih and Vil parameters)
- Ability to repeat measurements based on user settings and receive results with statistical analysis of all runs and worst-case screenshots
- Results summary that includes results, specifications and margin analysis
- HTML test report automatically generated, including screenshots for easy sharing and archiving

Automating measurements provides the quickest way to characterize and validate integrity for DDR signals – and lets you shift your focus from making measurements to using the results to improve your designs.

Related Literature

Publication title	Publication type	Publication number
DDR Memory Overview, Development Cycle and Challenges	Tutorial	5990-3180EN
DDR Design and Verification through Simulation	Tutorial	5990-3317EN
DDR Probing for Physical Layer and Functional Testing	Tutorial	5990-3182EN
Debugging Signal Integrity and Protocol Layers on DDR Designs	Tutorial	5990-3189EN
Identifying the Causes of DDR Data Corruption and Elusive Failures	Tutorial	5990-3183EN
Separating Read/Write Signals for DDR DRAM and Controller Validation	Tutorial	5990-3187EN
Agilent DDR Memory Solutions	Brochure	5990-3324EN

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