Boundary-Scan Testing of Power/Ground Pins

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Boundary-Scan Testing of Power/Ground Pins

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Abstract

Most integrated circuits today possess large numbers of power and ground pins in addition to signal pins. Boundary-Scan technology will adequately test the signals, but in general does not address open defects on the power/ground pins. Some ICs could get at least partial coverage on some of these pins due to their internal power/ground distribution structure. Thus Boundary-Scan could be used to test, diagnose and claim coverage for these defects. What is needed is an extension to BSDL to support this capability.

1 Introduction

A paper in 1989 [Lage89] first noted the fact that integrated circuits (IC) have a growing proportion of power and ground pins as a fraction of their total pin counts, and that Boundary-Scan technology [IEEE01] did not address testing for open-pin defects on these pins. The paper made some proposals for adding testability to such devices and making such defects observable in the Boundary Register, but the ideas did not gain traction. A 1996 paper [Tege96] noted that the fraction of untestable pins would soon exceed 50% and that these opens have demonstrable negative effects on board performance. A 2000 paper [DeJo00] demonstrated the idea of placing on-chip current sensors at power/ground pins with Boundary Register observation of their results. While this result was considered economic, it still has not gained traction in industry. With the interest in defect coverage measures growing [Hird02][Park03], people have become more aware of major coverage holes and more concerned about filling those holes.

In private discussions with IC designers, it has been noted that power and ground pins were added largely in an Ad-Hoc fashion and conservatively over-designed as noted in [Tege96]. Today’s design practice is becoming more deliberate and the number and distribution of power/ground pins is now an engineered process. Designers are trying to optimize these pins.

There seems to be two schools of thought in this engineering. One school says you absolutely must strap all the power/grounds together inside the IC package and also on the IC die itself. This will minimize parasitic resistance and inductance which are enemies of performance. It also makes detecting a single open pin virtually impossible. The second school says you must be careful to isolate portions of the power/ground distribution so as not to conduct noise from (say) powerful driver circuits to sensitive, high performance clock distribution networks. Indeed, simple experimentation with an ohmmeter will show, for some ICs, that there is no internal strapping of some power or ground pins within the IC package or die. Some IC designs carefully partition I/O buffers into independently powered blocks. In these cases, a single open may indeed cause an observable failure. But typical IC datasheets give virtually no information about power/ground distribution.

It is the second IC category that offers us a chance to improve opens coverage. If we can show that a given power/ground pin open will cause some form of Boundary-Scan test failure, then we can relate that failure to that open defect, offer a diagnosis, and credibly claim that defect is covered by our Boundary-Scan test. Today, these same tests will fail, but for undecipherable reasons that do not lead to a diagnosis and can result in ambiguous repair instructions. Worse, devices may be returned as defective, but will have “no trouble found” when they are re-tested by their manufacturer.

2 Power/Ground Opens Testing

First we start with a model of IC circuitry and power/ground distribution shown in Figure 1. This is generalized to circuitry subsets with low and high rails of distribution, and simplified where there are just two rails per subsystem. (The same principles would work for multiple rails.) Subset A has just one package pin per rail, while subset B has two package pins per rail, and subset C has many package pins per rail. If either the low-rail pin or the high-rail pin for subset A is open, we would expect
the circuitry inside that subset would fail to operate correctly. For subset B, both the low-rail pins, or both the high-rail pins would have to be open simultaneously for the circuitry to fail. This case is less probable if one assumes defects are relatively rare and equiprobable. Finally, for subset C, all the low-rail or all the high-rail pins would have to be open simultaneously for subset C to fail. This is very unlikely to happen.

It should be possible for an IC designer to describe an IC as circuitry subsets with this level of power/ground distribution. Note that if one subset was unpowered due to a defect that would likely cause the other subsets to fail as well, at least in the designer’s mind, because transactions between subsets would be affected.

Figure 1: IC with power/ground distribution.

We are only looking for a very basic concept of “fail” here and are restricting it to the 1149.1 functionality. This may be best illustrated with an example. Let’s say that subset A contains the 1149.1 TAP, instruction register and bypass register. Let several instances of subset B contain a small number of I/O pad circuits (drivers and receivers). Then let subset C contain all the rest of the IC’s circuitry, including the parallel load-shift stages of the Boundary Register. Now, if subset A is unpowered, we would not expect the 1149.1 TAP integrity tests to pass. If instead one of the subset B instances failed, then some number of IC I/O pins would not work, even though the rest of the 1149.1 circuitry was functional. This would impact a small number of pins during Boundary-Scan Interconnect testing. The likelihood of subset C failing is low, but if it did, much of the TAP integrity test would pass, until we got to the part where the Boundary Register is checked.

This leads us to try to describe the effects of power/ground distribution in a series of “triples”. Each triple would contain three pieces of information.

1) the low-rail pins
2) the 1149.1 functionality enabled by these pins
3) the high-rail pins

We also want to include this information in BSDL (Boundary-Scan Description Language [IEEE01]) so that tools that read BSDL can learn about power/ground pins that can affect Boundary-Scan tests.

A hypothetical IC is depicted in Figure 2, with power and ground distribution shown as routed from six different sets of power/ground pins. The first group (Pwr1, Gnd1) supplies power to three output drivers (pins 4-6). The second group (Pwr2, Gnd2) supplies output drivers on pins 1-3. The third group (Pwr3, Gnd3) supplies input receivers for pins 21-23. The fourth group (Pwr4, Gnd4) supplies the TAP along with the Boundary-Scan Instruction register, the Device ID register and the Bypass register. The fifth group supplies input receivers for pins 24-26. The sixth group (Pwr6, Gnd6) supplies the Boundary register cells and the system circuitry of the device. However, two more pins (Pwr7, Gnd7) also supply the Boundary register cells and the system circuitry. They are wired in parallel with group 6 inside the IC. This is summarized in Table 1.

Table 1: Summary of circuit subsets for Figure 2.

<table>
<thead>
<tr>
<th>Subset</th>
<th>Low rail</th>
<th>Powered Features</th>
<th>High rail</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Gnd1</td>
<td>Owt4, Owt5, Owt6</td>
<td>Pwr1</td>
</tr>
<tr>
<td>2</td>
<td>Gnd2</td>
<td>Owt1, Owt2, Owt3</td>
<td>Pwr2</td>
</tr>
<tr>
<td>3</td>
<td>Gnd3</td>
<td>Inn1, Inn2, Inn3</td>
<td>Pwr3</td>
</tr>
<tr>
<td>4</td>
<td>Gnd4</td>
<td>TAP, Instruction, Device_ID, Bypass,</td>
<td>Pwr4</td>
</tr>
<tr>
<td>5</td>
<td>Gnd5</td>
<td>Inn4, Inn5, Inn6</td>
<td>Pwr5</td>
</tr>
<tr>
<td>6</td>
<td>Gnd6, Gnd7</td>
<td>Boundary</td>
<td>Pwr6, Pwr7</td>
</tr>
</tbody>
</table>

Notice that subset 6 has two pin members for both the low rail and the high rail powering the Boundary register. This implies that if the Boundary register fails, at least two pins of either the low or high rails had to be open since there are redundant pins carrying power.

Note also that the system circuitry is powered by these pins but nothing is stated about this in the table. Boundary-Scan does not in general test the system circuitry. If this IC implemented a RUNBIST instruction which tested the system circuitry, then a keyword “System” could be added to subset 6 to denote this.
3 BSDL Description of Power/Ground Opens Effects

BSDL as specified in [IEEE01] is used to document the Boundary-Scan features of an IC which is compliant with the standard. The device in Figure 2 is described in Figure 3. BSDL allows for extensions which can be used for the private purposes of a given device vendor. It is also used to describe features that may be added to a device in support of additional standards such as 1149.6 [IEEE03]. BSDL-based test tools that understand certain extensions will read and utilize their content. Those that do not will simply ignore the information they contain. In this paper we offer an extension that would be used to describe power/ground features (those triples) that can be used to improve Boundary-Scan diagnostics during testing and to more completely document the test coverage of a Boundary-Scan test. This extension could some day be standardized as an addition to the 1149.1 document.

Figure 2: A hypothetical device with power/ground distribution shown.

Note: Pwr4 and Gnd4 supply the TAP, Instruction Register, Bypass and Device ID Registers.
entity PwrGnd is
  generic (PHYSICAL_PIN_MAP : string := "Dip");

  port (Owt:out bit_vector(1 to 6);
       Inn:in bit_vector(1 to 6);
       Gnd, Pwr:linkage bit_vector(1 to 7);
       TDO:out bit; TRSTn, TMS, TDI, TCK:in bit)

use STD_1149_1_2001.all;  -- Get Std 1149.1-2001 defs
use POWER_GROUND.all;      -- Get the BSDL Extension definition for Power/Grounds

attribute COMPONENT_CONFORMANCE of PwrGnd : entity is
  "STD_1149_1_1990";  -- This is an older IC
attribute PIN_MAP of PwrGnd : entity is
  PHYSICAL_PIN_MAP;
constant Dip:PIN_MAP_STRING:=
  "Owt:(1,2,3,4,5,6), " &
  "Inn:(21,22,23,24,25,26), " &
  "Gnd:(8,11,20,16,27,29,30), Pwr:(7,13,19,13,28,10,9), " &
  "TDO:12, TMS:15, TCK:17, TDI:18, TRSTn:14";
attribute TAP_SCAN_IN of TDI : signal is true;
attribute TAP_SCAN_MODE of TMS : signal is true;
attribute TAP_SCAN_OUT of TDO : signal is true;
attribute TAP_SCAN_CLOCK of TCK : signal is (20.0e6, BOTH);
attribute TAP_SCAN_RESET of TRSTn : signal is true;
attribute INSTRUCTION_LENGTH of PwrGnd : entity is 6;
attribute INSTRUCTION_OPCODE of PwrGnd : entity is
  "BYPASS (111111, 100010)," &
  "EXTEST (100000), PRELOAD (000010), SAMPLE (000010)";
attribute INSTRUCTION_CAPTURE of PwrGnd : entity is
  "100010";
attribute BOUNDARY_LENGTH of PwrGnd : entity is 12;
attribute BOUNDARY_REGISTER of PwrGnd : entity is
  -- num cell  port  function safe [ccell disval rslt]
  "11 (BC_1, Inn(1), input, X)," &
  "10 (BC_1, Inn(2), input, X)," &
  " 9 (BC_1, Inn(3), input, X)," &
  " 8 (BC_1, Inn(4), input, X)," &
  " 7 (BC_1, Inn(5), input, X)," &
  " 6 (BC_1, Inn(6), input, X)," &
  " 5 (BC_1, Owt(6), output2, X)," &
  " 4 (BC_1, Owt(5), output2, X)," &
  " 3 (BC_1, Owt(4), output2, X)," &
  " 2 (BC_1, Owt(3), output2, X)," &
  " 1 (BC_1, Owt(2), output2, X)," &
  " 0 (BC_1, Owt(1), output2, X);"

-- This is where the BSDL_EXTENSION for power/ground description would appear.
end PwrGnd;

Figure 3: BSDL for the device in Figure 2.

Just before the end of this BSDL is a comment indicating the place where a descriptive extension for power/ground would be placed. The use of a new BSDL package (called “POWER_GROUND”) is referenced in the eighth line of this BSDL. The BSDL package is described in Figure 4. This package would reside in the file system where the other BSDL packages (such as STD_1149_1_2001) reside. 

The extension alluded to by the comment will next be described by example, saving a discussion of rigorously formal syntax for a later time.

Of the triples of information we need to describe, two are used to describe the low and high rails of the power distribution, and should thus have identical syntax. The powered features will have their own syntax.
A power/ground description must be able to describe an arbitrary number of subset triples as a list. So the basic high-level syntax could be:

\[
\text{Attribute Power\_Ground of entity PwrGnd is } "\langle\text{triple list}\rangle"; \\
\langle\text{triple list}\rangle ::= \langle\text{triple}\rangle \mid \langle\text{triple list}\rangle; \langle\text{triple}\rangle
\]

Next we need to describe the content of a triple. It has two basic elements, a rail description and a Boundary-Scan resource description.

\[
\langle\text{triple}\rangle ::= \langle\text{rail}\rangle:\langle\text{resources}\rangle:\langle\text{rail}\rangle
\]

A rail description may describe a single pin for one voltage, multiple pins for one voltage, or several voltages and pin sets.

\[
\langle\text{rail}\rangle ::= \langle\text{voltage pins}\rangle \mid \langle\text{rail}\rangle, \langle\text{voltage pins}\rangle \\
\langle\text{voltage pins}\rangle ::= ( ) \mid (\langle\text{pin list}\rangle) \\
\langle\text{pin list}\rangle ::= \langle\text{pin}\rangle \mid \langle\text{pin list}\rangle, \langle\text{pin}\rangle \\
\langle\text{pin}\rangle ::= \langle\text{BSDL signal name}\rangle
\]

Here are some examples of rail descriptions, from simple to multi-rail.

\[
\langle\text{Gnd1}\rangle \quad \text{-- One pin for one rail} \\
\langle\text{Pwr1,Pwr2}\rangle \quad \text{-- Two parallel pins, 1 rail} \\
\langle\text{Pwr1,}\langle\text{Pwr2}\rangle \quad \text{-- Two one-pin rails} \\
\langle\text{Pwr1,Pwr2},\langle\text{Pwr3,Pwr4}\rangle \quad \text{-- Two 2-pin rails} \\
( ) \quad \text{-- Empty list}
\]

The empty list is used to handle the case where there are so many pins connected in parallel that it is unreasonable to document them all since the probability of them all being open simultaneously is nil.

Next there are the Boundary-Scan resources powered by the rails.

\[
\langle\text{resources}\rangle ::= \langle\text{resource}\rangle \mid \langle\text{resources}\rangle, \langle\text{resource}\rangle \\
\langle\text{resource}\rangle ::= \langle\text{TAP}\rangle \mid \langle\text{BYPASS}\rangle \mid \langle\text{BOUNDARY}\rangle
\]

Thus, for the fictional device in Figure 2 the BSDL extension would be as follows:

\[
\text{Attribute Power\_Ground of entity PwrGnd is } "\langle\text{Gnd1}>:\langle\text{Owt4}, \text{Owt5, Owt6:(Pwr1)}\rangle; \ "& \\
"\langle\text{Gnd2}>:\langle\text{Owt1, Owt2, Owt3:(Pwr2)}\rangle; \ "& \\
"\langle\text{Gnd3}>:\langle\text{Inn1, Inn2, Inn3:(Pwr3)}\rangle; \ "& \\
"\langle\text{Gnd4}>:\langle\text{TAP, Instruction, Device\_ID, Bypass:(Pwr4)}\rangle; \ "& \\
"\langle\text{Gnd5}>:\langle\text{Inn4, Inn5, Inn6:(Pwr5)}\rangle; \ "& \\
"\langle\text{Gnd6, Gnd7}>:\langle\text{Boundary:(Pwr6, Pwr7)}\rangle;"
\]

The resources map onto potential failures during Boundary-Scan testing as shown in Table 2.

<table>
<thead>
<tr>
<th>Resource</th>
<th>Failure</th>
</tr>
</thead>
<tbody>
<tr>
<td>TAP</td>
<td>Failure of TAP data shift (TDI-to-TDO)</td>
</tr>
<tr>
<td>Bypass</td>
<td>Failure of Bypass register readout</td>
</tr>
<tr>
<td>Instruction</td>
<td>Failure of Instruction register readout</td>
</tr>
<tr>
<td>Device_ID</td>
<td>Failure of Device_ID readout</td>
</tr>
<tr>
<td>Boundary</td>
<td>Failure of Boundary register readout</td>
</tr>
<tr>
<td>Signal</td>
<td>Failure of I/O pin to drive or capture data</td>
</tr>
</tbody>
</table>

Table 2: Resources and potential failures.

When these failures are observed, then the related rails can be indicted as possible open defects that should be examined during repair. When several resources are indicted within a single triple, the reporting algorithm can check to see if all the resources exhibited failing behavior before indicting the associated rails. For example, in the description above, if Owt4, Owt5 and Owt6 all fail during a Boundary-Scan interconnection test, then there could be three simultaneous defects on their associated pins, and, there is a chance that one or both rail pins are defective.

4 A Real Example of a Xilinx Device

We consider a real-life example of a modern FPGA device, the XC5VLX110 [Xili08a]. This device comes in an 1153-pin package (referred to as the FF1153) which is basically a 34x34 square of ball joints. Three corner balls are missing for orientation marking. Figure 5 (at the end of this paper) shows a map of the power and ground pin layout in colors: Ground(197 pins) = black, V Batt(1 pin)
= orange, VCCAux(12 pins) = magenta, VCCInt(53 pins) = green, and then there are 23 “bank” power pins called VCCO<n> which are all in yellow. Each yellow bank pin is labeled with its bank number <n>. All the VCCO<n> bank supply voltages have only 2 or 3 pins.

Within each supply pin type, all those pins are connected together. Thus, if open pins are not a very common occurrence, it would be unreasonable to expect, for example, all 197 ground pins to be open at the same time, when opens occur in a somewhat random fashion. Thus we would not bother to describe how “open ground” would affect the Boundary-Scan behavior of the device. Similarly, we would not describe the effects of VCCAux and VCCInt due to their large numbers. However, VBatt and the VCCO<n> pins are candidates for description.

It turns out that the solitary VBatt supply pin only powers the storage memory encryption key, so if that pin is ever open, the key that unlocks the ability of the memory content readout is lost. This is not a typical Boundary-Scan function (per IEEE Std 1149.1) so we will not describe the VBatt connection. It could be argued that Boundary-Scan (via IEEE Std 1532 [IEEE00]) could determine the effect of this open supply pin, but we leave that for future discussion.

This leaves us with the 23 VCCO<n> supplies. They supply signal output drivers and are always 2 or 3 pins in relatively close proximity. In particular, look at VCCO0 (bank 0 supply) pins at locations AD13 and AG14. All of the 26 pins that are supplied by VCCO0 are shown in blue. If these two pins are open, which we deem a possibility worth considering, then all of these 26 pins may be affected, for example, not being able to drive proper levels. Indeed, it turns out that the TAP signals (TCK, TMS, TDI and TDO) are also powered by VCCO0 so we would expect a massive TAP integrity failure if VCCO0 was compromised. Investigation into the actual detailed design implementation of the TAP input pins TCK, TMS, TDI also showed that while VCCO0 powers them, there is a level conversion stage on their outputs that is powered by VCCInt. We did not code for these three pins being subject to a VCCInt open due to the large number of VCCInt pins.

Further research into power and grounding revealed that the TAP state machine is powered by VCCInt, as is the Boundary Register, Bypass Register, ID register and numerous private registers. The IEEE 1532 controller and associated registers are also powered by VCCInt. The 1532 configuration memory is powered by a combination of VCCInt and VCCAux.

The BSDL for this device is available [Xili08b] and we reference it (for consistency of names) to write a power/ground description. Here is a portion of the BSDL extension we would need to describe the VCCO<n> signals:

```
Attribute Power_Ground of entity
XC5VLX110_FF1153 is
 "()::PROG_B, 
 & -- In, compliance en
  HSWAP_EN_N22,"$-- In
  D_IN_N13, " & -- In
  DONE_N14, " & -- Inout
  CCLK_M13, " & -- Inout
  INIT_B_L13," & -- Inout
  CS_B_M23, " & -- In
  RDWR_B_N23," & -- In
  TCK, " -- In, TCK
  MO_AD21, " & -- In
  M2_AD22, " & -- In
  M1_AC22, " & -- In
  TMS, " & -- In, TMS
  TDI, " & -- In, TDI
  DOUT_BUSY_AD14,"& -- Out
  TDO, " & -- Out, TDO
  TAP:(VCCO0); "& -- TAP keyword
-- Done with VCCO0, begin VCCO1
 "()::IO_L20, " & -- Inout
  IO_L19, " & -- Inout
  IO_K17, " & -- Inout
... <many more>
 " :(VCCO1); "&
-- Done with VCCO1, begin VCCO2
... <more VCCO<n> supplies>
 " :(VCCO6) ";
```

Note in this description for VCCO0 we have omitted linkage signals and just described those that are type In, Out and Inout. The “Prog_B” signal is a compliance enable input. It this pin is inoperable because of a VCCO0 failure, that may also cause a massive TAP integrity failure.

5 Conclusions

For at least some IC devices in existence today, it is possible to gain additional pin open defect coverage on supply rails using Boundary-Scan. This paper has provided a simple syntax for a BSDL extension that would document these opportunities such that test-time diagnostics could indicate these defects when they occur. Further, a board test coverage measurement tool could also claim new power and ground pin coverage based on this information.
Figure 5: Power and Ground mapping for the XC5VLX110 FPGA in the FF1153 package.
6 References


[Xili08b] Get zipped download (requires login) from http://download.xilinx.com/protected/generics/bsdl/xc5v.zip