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Abstract

Sockets used for complex CPUs or System-on-a-chip (SOC) devices present extraordinary challenges for In-Circuit test. They usually have a large number of pins packed into a very small area. Additionally, a large percentage of the pins in the socket are power and ground pins that have limited or no discernible test coverage. Test industry solutions for these challenges have included functional test, inserted custom silicon test chips, and vector-less test. These solutions typically have one or more tradeoffs of time, complexity, cost, or coverage. This paper presents an extension to Network Parameter Measurement technology that allows vector-less test methodologies to overcome many of the challenges that sockets present.

1 Introduction

The increasing prevalence of sockets in many large-scale motherboards and servers often results in diminished test coverage in critical sections of those designs. These sockets present extraordinary test challenges because the increased circuit integration and functionality in the socket target device commonly means there will be many pins packed into a very small area. For example, current generation CPUs not only contain multi-core architectures but they also consolidate functionality such as direct memory access, multiple communication protocols, and IO control that was held in external chips only a few years ago. Thus, sockets, like the one shown in Figure 1, with more than 1000 pins and a pin pitch of 1mm or smaller are not exceptions any more.

In addition to the leap in pin density, a higher percentage of the pins in the sockets is being reserved for use as “fixed” power and ground pins. With modern processors capable of operating at 3 GHz and dissipating more than 100W, these fixed pins are responsible for helping maintain the signal integrity of off-chip IO and the quality of the power distribution. These pins have traditionally been the hardest to test because of parallel redundancy which leads to detection ambiguity.

2 Pin Functionality

All socket pins are not created equal – at least as far as most test technologies are concerned. Some pins are harder than others to get any coverage for without even mentioning diagnostic separability. In some cases this is OK as long as you understand the trade-offs you are making with respect to test time, test coverage, and test
cost compared against statistical probability of failure, warranty costs, and customer satisfaction.

2.1 Pin Classification for Test Purposes

For test technologies that make some physical contact to the socket or the PCB (non-inspection based methods), it is insightful to classify the pins in the socket being tested by function. This lends an understanding of potential shortcomings of the test methods.

2.1.1 Signal Pins

These socket pins connect to pins in the target silicon device that can change state during normal board usage. Opens defects on signal pins usually lead to outright failures that prevent the design from functioning at a basic level. Address bus lines, data bus lines, and RAM control lines are examples of signal pins.

2.1.2 Fixed Pins Used for Signal Integrity

Unlike signal pins, a “fixed” pin is a socket pin that connects to a target pin held at a constant or fixed voltage level when the board is powered up. This set of pins encompasses power pins, ground pins, and voltage reference pins. Fixed pins can further be subdivided into those pins which are critical for signal integrity aspects of the board level design.

Recent papers have discussed the importance of test coverage for fixed pins as they relate to High-Speed Signal Propagation (HSSP) [PaHi07, Park05]. Opens defects resulting from coverage gaps on certain fixed pins used for signal integrity can result in loss of signal margin, increased bit error rate, and increased Electromagnetic Interference (EMI) [JoGr93]. Examples of signal integrity fixed pins would be ground pins interspersed throughout a group of signal pins for the purposes of providing each with low inductance return current paths.

2.1.3 Fixed Pins Used for Power Distribution

The target devices that are inserted into sockets certainly contain a fair number of fixed pins used for signal integrity but they also contain a set of pins whose primary use is for power distribution. Opens defects on these pins lead to uneven power distribution across the target devices and a higher than desired impedance connection between power and ground planes [JoGr93]. Power distribution fixed pins are usually the power and ground pins that appear clustered together in the center of large silicon devices.

2.1.4 Inaccessible Pins

Beyond signal and fixed pins for which some electrical test access exists, there almost always exists a set of pins which cannot be accessed by a test fixture. It doesn’t matter if these “inaccessible” pins are fixed or used for signaling because they are not observable by the tester. These pins can become inaccessible for several reasons:

1. PCB density doesn’t allow for a probe access testpoint.
2. Probe access may be blocked in the fixture by other probes.
3. The complexity of the PCB may consume all of the available tester resources preventing 100% probe access.

Figure 2 shows an example pinout for a fictitious socket. A fair majority of the pins are allocated for usage as signal pins as expected. The center of the chip contains a cluster of pins that are power and ground fixed pins that are responsible for general power distribution. Signal integrity fixed pins typically are ground pins that are distributed throughout the device in a checkerboard type arrangement in order to provide low inductance return current paths. Also shown in the fictitious example are a few pins that are inaccessible to a probe access on the PCB.

Figure 2: Example Pinout of Fictitious Socket

3 Socket Test Methods

Some popular methods for testing sockets include non-contact observation with x-rays, advanced functional testing using the target silicon device, customized testing using a specially designed ASIC, and vector-less testing using technologies such as NPM. There may not be one particular solution that meets all needs for everyone’s
socket test situation. It is up to the test engineer to weigh the advantages and disadvantages of each for the specific manufacturing process.

3.1 Automated X-Ray Inspection

The exception to the earlier statement on pin equality is automated X-Ray inspection (AXI). AXI doesn’t care about how the pins in the socket are used because it doesn’t make any physical contact to the pins in the socket. It simply exposes the board being tested to x-rays and then re-constructs 3D images to determine the goodness of the solder connection between the socket and the printed circuit board (PCB). For some manufacturers, though, AXI may not be an option due to cost, space, manufacturing beat rate, or existing manufacturing line configuration.

3.2 Functional

Functional testing of the socket and the target silicon device at the same time is another option that test engineers may choose. The circuit design is powered up during one of the latter phases of the test process, presumably after passing gross unpowered shorts and opens tests and powered validation of the voltage rails. Then some design specific software is used to functionally exercise features of the target silicon device and also implicitly test the socket connections as well.

While this approach has the benefit of providing some test coverage through somewhat realistic application software, it also can have some painful drawbacks. Most notably, the software might take the test engineer significant time to develop and debug and require intricate knowledge of the circuit design if appropriate application software isn’t available to leverage from. Secondly, one must understand the potential test escapes and try to mitigate them with a comprehensive software strategy in addition to robust observation. Defects on signal pins are obviously easiest caught if the software can force each to change state. Fixed pin defects are much more nefarious since they often don’t result in hard test failures but instead are observed through advanced diagnostics such as bit-error rate (BER) monitoring.

3.3 Silicon Surrogates

A specially designed ASIC inserted into the socket during manufacturing test solely for the purposes of test is an alternative to using the original target silicon device to functionally validate the socket. This special chip could have FET switches that are dynamically controlled to make contact with individual pins. The obvious advantage over the afore mentioned functional testing is complete and customizable stimulus and response by the test engineer. This can lead to better coverage, improved diagnostic capability, and better observability. The primary disadvantages to spinning your own silicon solution are time (design, layout, fabricate, test) and financial justification of somewhat significant ASIC design costs. These factors make the ASIC test solution less attractive especially when you also consider that the ASIC is unique to the target socket.

3.4 Vector-less Test with NPM

Capacitive Leadframe testing techniques such as “TestJet” are widely popular for testing connectors and sockets during the ICT step of a manufacturing process because they are “vector-less”. A substantial amount of coverage is gained for considerably little effort and little to no knowledge of the design being tested. The test engineer didn’t have to create any vectors since the analog AC stimulus is inherently the same for every pin. The expected response picked up by a sense plate proximally close and above the connector or socket is a capacitive value measured in femtofarads. The sense plate recognizes opens defects as changes from the nominally learned value of femtofarads on a known-good-board (KGB).

TestJet has not been without its own limitations. [PaHi07] describes in detail the ineffectiveness of TestJet for coverage of fixed pins on connectors and sockets. Redundant fixed pins and large external capacitances to other nodes are discussed as the obstacles to complete coverage. The [PaHi07] paper introduces Network Parameter Technology as an innovative approach to extending the test coverage of capacitive leadframe testing to further cover many fixed pins on connectors and sockets. NPM improves upon TestJet technology by not considering pins under test to simply be singular entities, but instead part of a larger electrical system. Pin electrical models like the one shown in Figure 3 are collectively analyzed in order to provide additional insight into defects present on connectors and sockets.

![Figure 3: Four Pin Electrical Model](image)

1 “TestJet” is a registered trademark of Agilent Technologies.
Examples of real production designs containing multiple PCI Express and DDR2 connectors and CPU sockets demonstrated comprehensive coverage on the connectors and greatly improved but not perfect coverage for the CPU sockets.

4 An Engineered Interposer

NPM furthered TestJet technology by recognizing the relationships amongst pins when viewed as a collection. This has been shown to work well as long as these relationships exist. Sockets stretch the capability of NPM because visible relationships don’t exist across all of the pins in the entire socket. Located in the center of the fictitious example socket of Figure 2 are a set of fixed pins that are seemingly redundantly connected. The visibility of the electrical network parameters utilized by NPM is clouded. Smaller socket geometries also can reduce the visibility of the pins as viewed from the sense plate. Modern land-grid array (LGA) sockets like the one shown in Figure 1 can easily have pin contacts that are 1mm or shorter as compared to a PCI Express socket with pins measuring about 10mm in length.

The goal for the engineered interposer is to achieve maximum socket test coverage not only on signal pins but also on fixed pins and inaccessible pins. Basic design constraints for the engineered interposer are:

1. Low cost
2. Minimal design effort
3. Low false call rate

The interposer design described in this paper accomplished these goals within the stated constraints by advancing the effectiveness of NPM technology. To do this, parametric relationships between pins in the socket had to be created where they previously didn’t exist and the capacitive coupling to the sense plate had to be boosted for optimal measurements.

4.1 Mechanical Considerations

Choosing to insert anything into a socket solely for the purposes of test can be a hard decision for many test engineers to make. Will the act of insertion cause damage? Where in the test process will the insertion step take place? Who or what will do it? How will this affect manufacturing cost and line beat rate? Some of these questions can only be answered by the test engineer when the specific test process is evaluated and the trade-offs are compared against the added benefits of higher test coverage and ultimately lower warranty cost. Manufacturers who have successfully instituted either a functional or ASIC centric test approach for sockets often combat these questions through operator training and/or mechanical insertion mechanisms. Sometimes the insertion step is not an issue because processes are already in place to remove or install shipping slugs and the target device.

An alternative to manually inserting the interposer into the socket is to have it hover in close contact to the top of socket with position controlled by opening and closing the test fixture. This is concept is well understood by fixture vendors who have implemented TestJet sense plates in ICT fixtures.

Figure 4 shows an interposer design that is manually inserted into the CPU socket of Figure 1. It was decided to go with manual insertion instead of a hovering style plate because this particular LGA socket has a lid which clamps the target silicon device snugly into place. The mechanical datasheet for the target CPU device was studied and the interposer dimensions, mechanical keying, and land grid pads were made to match that of the CPU. Doing this helped to mitigate concerns of damage and also helped provide a reliable connection to the pins in the socket. Once the interposer was inserted and the socket lid closed, a capacitive sense plate could descend over the top of the interposer as would normally be the case for most TestJet tests involving connectors.

4.2 Electrical Design

4.2.1 Low Cost

To keep the cost of the solution low, it was decided to fabricate the interposer using standard FR4 PCB technology. Compared to spinning a ASIC, a PCB design was fundamentally lower cost because it was cheaper to layout and produce. Additionally, the turn-around time is measured in days rather than weeks.

4.2.2 Engineering Relationships

Gaining test coverage on socket pins by enhancing NPM meant improving the visibility on those pins for which the relationships didn’t exist or were too weak. Refer back to the simplified electrical model of the 4 pins shown in Figure 3. If the system parameters are so small that they are non-existent when viewed from the sense plate or ambiguous with other pins in the network then NPM coverage will not be optimal. The interposer design
engineered artificial relationships through general trace routing between pins whose electrical parameters were visible to the sense plate and those that weren’t visible, essentially “piggy-backing” coverage.

The GERBER format view depicted in Figure 5 shows how a parametric relationship between pins can be engineered. One layer of the GERBER file is shown for a set of 4 pins. Pads 1, 2, 3, and 4 are on the bottomside layer of the interposer and make direct physical contact to the socket pins when the interposer is inserted. Vias A, B, C, and D each traverse all layers of the PCB and are connected to a similar pad arrangement on the topside of the interposer. Doing just this will immediately have benefits to capacitive leadframe sensing because the short pins in the LGA which were probably on the order of 1mm have been lengthened and the sense plate now “sees” a spacious pad on the top of the interposer. Also shown in the single layer GERBER view is a trace that physically connects to the B via for pad 2 and horseshoes over to pad 3. The socket pin that connects to pad 3 may not have been visible to NPM before the interposer but it now has a new relationship engineered to the socket pin contacted to pad 2. The electrical model of Figure 3 which originally was just based on spatial relationships has now been augmented.

4.2.3 Minimal Design Effort

Designing an engineered interposer for a socket design with over a 1000 pins would be too cumbersome if the designer had to sit down and consider each of the 1000 pins individually to determine how to route the PCB. Fortunately a standard cell methodology can be adopted to prevent the design from becoming intractable. To achieve this, upfront knowledge of the pinout of the socket needs to be known before beginning the design. This allows the designer to know in advance which pins need to have relationships engineered to other visible pins. The designer also needs to have simulated one or more methods (such as the horseshoe) for engineering relationships that end up becoming the standard cells placed in the PCB layout. Lastly, to complete the turnkey approach, it is helpful for the interposer designer to have an automatic method for generating the net list given a list of pins that need to have engineered relationships and another list of visible candidate pins to engineer the relationships to.

An additional benefit can be gained from the engineered interposer if the test engineer has done some board test development before the engineered interposer is designed. Running the development through the probe-placement step and assignment of ICT resources tells the engineer which nodes attached so socket pins are inaccessible. The engineered interposer design can then take this into account so make sure that coverage on these pins is not lost at the last minute.

4.2.4 Low False Call Rate

One last optional ingredient to the engineered interposer design is redundancy. It is possible to engineer more than one parametric relationship for each pin such that NPM has additional information to analyze when diagnosing the goodness of the socket connections. The obvious benefit is minimization of false calls and test escapes – two important metrics for every test engineer.

5 Experimental Test Case

As with many new ideas, the viability of an engineered interposer could not be determined with paper analysis alone. Manufacturing environments are not likely to be well behaved with respect to the many practical unknowns that they can introduce. The concept of an engineered interposer and its potential customer value needed to be “road tested” to confirm the paper theory, quantify system variables, and validate algorithm methods.

5.1 The Socket F 1207

The Socket F 1207 CPU socket provided a golden opportunity to examine the various feasibility aspects of the interposer. This BGA socket contains a 35 by 35 matrix of 1207 pins (18 intentionally missing) in an area of about 1.5 square inches with a pin pitch of 43.3 mils and nominal pad size of 33 mils. The PCB test vehicle
was a quad server board featuring 4 AMD Opteron² processors in these F 1207 sockets.

The target Opteron processor has roughly 600 of its 1207 pins allocated for use as fixed pins such as VSS, VTT, or VDD. With 4 of these on the board and assuming that traditional vector-less test covered all of the remaining signal pins, that leaves about 2400 pins that are not tested by traditional in-circuit test methods.

5.1.1 Probe Access for Stimulus

Vector-less test methods require some measure of nodal access for the purposes of applying a test stimulus. This interposer design was no exception since it was predicated upon creating electrical relationships between signal pins that it could stimulate and fixed pins that couldn’t be stimulated. The engineered coverage on the fixed pins required stimulus to be applied to at least some of the signal pins.

By the time the interposer design was considered for an evaluation, the quad server board was well into its design cycle. Test point access for the in-circuit test was already set in stone and the back mounting plate for the F 1207 CPU socket was already designed. Fortunately, the test point access for the signal nodes on the 4 sockets wasn’t too bad. There were, however, a set of nodes that had their test points blocked by the backside metal backing plate. A special backing plate was designed for the purposes of the interposer experimentation so as not to give up test coverage. This new backing plate had some of its metal removed in the regions of the test points. It was installed during the in-circuit test.

5.2 Design

5.2.1 Interposer Design

The design of the interposer PCB began by looking at the datasheet for the Opteron chip that goes inside of the Socket F 1207 socket. Specifically, the datasheet included dimensions of the chip and pin functionality. Chip dimensions, perimeter key cutout shapes, and bottom side pad locations and dimensions were the first design constraints for the interposer since it had to fit snugly inside of the socket just as the CPU would without damaging the socket pins. Pin functionality was important because it described whether each pin was to be classified as a fixed or signal pin for the purposes of test.

Ideally, chip dimensions and pin functionality would have been enough to begin the design but they weren’t in this case because the test point access to the signal pins was already set. If this wasn’t the case then the interposer design could have proceeded along concurrently with a design-for-manufacturing (DFM) discussion with the PCB layout and test engineers to negotiate appropriate test point access. It is unrealistic to demand 100% test point access on complex PCB designs because of circuit density and ICT fixture cost. In the ideal DFM situation, the interposer design could prioritize the importance of access on certain nodes thus allowing for optimum test point decision making that not only achieves maximum coverage but also saves the time and expense of test pointing every node.

With interposer dimensions, pin functionality, and ICT nodal access known, the nuts and bolts of the interposer design could begin. The large number of socket pins (1207) would have made a custom schematic design time-prohibitive and error prone. So, a proprietary software tool was developed to automate the creation of a schematic net list which was then fed into a PCB layout tool. Standard routing methodologies that were simulated in advance made the creation of this software possible. Simulations of pre-defined, engineered relationships such as the one in Figure 5 were performed using available industry tools for extracting interconnect parasitics of resistance, capacitance, and inductance. The net list generator software used the rules developed through simulation to create a design that would fit into the available routing space and even incorporate diagnostic redundancy for each pin.

5.2.2 Diagnostic Software Design

The fundamental idea behind obtaining coverage with the interposer design is based upon engineering known relationships between pins which can and can’t be stimulated. In addition to a net list used to create the interposer PCB, the net list generator software also creates a model describing the network of relationships between the pins. This model is essential for the diagnostic software when doing an analysis to determine if manufacturing faults exist for the CPU socket. NPM technology was used as the foundation for the interposer diagnostic software since it also relied on parasitic model relationships (although implicit to the connector) to diagnose faults. The algorithm had to be augmented to compensate for traditional complexities inherent to the manufacturing environment along with some new variables related to the interposer system.

Board-to-board variation and measurement uncertainty are familiar opponents to a stable test in a manufacturing environment. Measurement uncertainty is easiest to control by characterizing a good hardware design and incorporating guard-banding techniques. Board-to-board variation is much more nefarious because it encompasses the multiple unknowns that influence measurement readings and make board comparison difficult. The algorithm accounts for this variation using statistical normalization against auto-learned values from a KGB.

New uncertainties for the interposer software algorithm to deal with included variation between interposer

²“Opteron” is a registered trademark of AMD.
PCBs and variation due to interposer insertion. PCB tolerances for copper etching, copper thickness, stackup thickness, and dielectric constant could have some effect on the parasitics that each interposer introduces to a measurement. For the purposes of the experiment and in the essence of time, these were not characterized. This variable was largely avoided by auto-learning a given interposer to particular socket location in the design. Then subsequent runs for a different board would take the same interposer and put it in the same location on the next board.

Interposer insertion variation, however, was an unavoidable variable because the interposer had to be removed and installed with the testing of each new board. Similar to many LGA sockets today, the Socket F 1207 has a mechanical clamshell locking mechanism which holds the CPU inside with an amount of force designed to ensure good contact with the socket pins. Insertion variation would be noticeable if the interposer dimensions didn’t also ensure the same snug fit or if the interposer was haphazardly inserted. As such, this was a main focus of data collection during experiments. The software dealt with this variation by first recognizing it and then taking advantage of diagnostic redundancies that were engineered into the interposer for each pin.

5.3 Results

On paper, the theory and simulations behind the design of the hardware indicated that interposer solution would increase coverage on the Socket F 1207 by testing an additional 600 fixed power and ground pins that weren’t covered with other traditional ICT methods. Theory would not be enough, though, to determine the viability of the interposer solution in a manufacturing environment testing actual sockets on PCBs. The Socket F 1207 on the quad server board provided a golden opportunity to examine the interposer as a means to increasing coverage on sockets.

Testing of the interposer hardware and software was broken up into two parts: focused internal testing in a controlled lab environment and external “alpha site” testing in a manufacturing setting. For consistency and expediency, the same quad server board was used for both internal and external testing.

5.3.1 Internal Testing

The primary focus of lab testing was theory confirmation. Did the interposer hardware work as it was intended? Could it catch opens on fixed pins for a complex socket? Defects had to be seeded to answer these questions.

Seeding a defect on a BGA land grid array component is not an easy, quick thing to do even if you have convenient access to a BGA re-work machine and stencil. Moreover, how do you know that the defect you have seeded is indicative of a real-world defect? Given that and the desire to make the most of the precious time for experiments, it was decided to seed defects directly at the point where the socket pin makes contact with the bottom side of the interposer. This was done by placing a small, thin, non-conductive piece of tape over selected interposer pads in order to create opens in the path.

Figure 6: Socket F 1207 Pin Functionality and Seeded Defects

Locations of the seeded defects were chosen so as to confirm that they could be caught on multiple locations of the socket landscape regardless of placement or distribution. Figure 6 shows the pin functionality of the pins in the Socket F 1207 and the locations of the defects that were seeded. Twenty-six total (but not unique) defects were seeded on combinations of different interposers. Using an early stage software algorithm, 16 of the 26 defects were caught with ease, 7 were apparent but not obvious, and 3 were not flagged. These results were not perfect but they did show that the fundamental theory behind the interposer had merit.

The imperfect results also showed that the software algorithm couldn’t simply be built around the engineered electrical model without incorporating some statistics and heuristics to manage variables that couldn’t be modeled. This was most apparent with rev 1 prototype interposers that didn’t fit into the socket properly and introduced insertion variation that obscured the measurements in some cases.

5.3.2 External Testing

Manufacturing demands for the quad server boards with the 4 Socket F 1207 sockets and the prototype nature of the interposer solution didn’t allow for an open-ended, limitless evaluation of the interposer on the actual
manufacturing floor in real time. There was an opportunity, however, to still do a “mini-alpha” production run of 11 boards outside of the time pressures of the manufacturing setting. These boards had passed basic shorts and unpowered testing and didn’t exhibit gross pin contact problems.

One of the 11 boards was set aside to use as a KGB reference leaving 10 boards and 40 unique sockets for the alpha evaluation. Some of the 10 boards were run multiple times to quantify effects of fixture actuation and interposer insertion. In total, 88 individual socket test runs were analyzed.

No defects were intentionally seeded on any of the boards tested again due to the practicality of time. The expectation was that 40 sockets with 600 fixed pins each would most likely give one or more without any effort. Catching defects wasn’t the only objective for the testing. An enhanced version of the initial algorithm needed to also show that it could withstand manufacturing variations while keeping the false fail rate to an acceptably low level.

At the completion of testing for the alpha production run of 10 quad server boards, 2 fixed pins on one socket were classified as bad. The software didn’t indict any other failures. It could not be confirmed that the 2 fixed pins were truly defective since verification with a 3D x-ray wasn’t available. An unsuccessful attempt was made to try and validate with a simple ohm meter but directly probing the socket pin was too difficult. Subsequent post-processing of the data back in the lab supported the analysis by the algorithm with some confidence. The redundancy designed into the interposer hardware makes it statistically likely that the 2 pins were indeed defective in some way. Some possibilities include open BGA solder joints, faulty socket, or bent pins. Fixture contact was deemed unlikely when a re-test of the board yielded the same results. Oxidation on the mating pad of the interposer was also considered but the same interposer PCB was used for testing other sockets without flagging failures.

All of the 88 runs of socket data was post-processed in the lab, not just the socket with the suspected defects. The analysis was looking for any test escapes that the software may have missed. None were found.

6 Realistic Expectations and Considerations

Assuming that only the 2 indicted pins from the run of 10 boards were defective, the interposer hardware and software combination couldn’t have had better results. It successfully found the defects without erroneously flagging good pins. This shouldn’t imply that the evaluation of the interposer is complete. Results for the small sample of boards were promising but the rigors of mass production testing will still be needed to gain more confidence.

It is also not expected that the design effort is entirely complete. There are still concerns over the system variables that the interposer hardware and software can’t control such as mechanical insertion. The algorithm seemed to adequately recognize and adapt to data that wasn’t well-behaved and thus avoided making false calls. A larger production dataset is needed to know that this didn’t come at the expense of test escapes.

All defects may not be able to be caught. The interposer PCB is engineered to do so but invariably there might be a small subset of pins that the software doesn’t flag due to a confidence threshold that balances aggressiveness versus reporting false calls. More data ultimately will lead to better algorithm refinements.

Lastly, a couple considerations for the manufacturing use model of the interposer solution have to be understood and accepted. Coverage for inaccessible pins can be designed into the interposer but some nodal access for ICT stimulus is still needed. The quad server board used for this validation already had its access defined ahead of the interposer design resulting in the creation of a special backing plate for purposes of getting test point access. Installation and removal of this during the manufacturing stages can be avoided with upfront DFM.

The other manufacturing consideration is the insertion step of the interposers into the sockets. The obvious trade-offs of manually inserting interposers versus a more custom automated approach need to be thought through. In the end, the test engineer ultimately weighs these types of trade-offs against the added value of coverage for socket fixed pins – 2400 additional pins of coverage for the case of the Socket F 1207 sockets on the quad server board in this case.

7 Conclusion

The advancements in socket technology coupled with the large scale integration of more circuit functionality into single chip solutions and the importance of high-speed signal propagation have made test coverage on sockets more important than before. An engineered interposer solution can substantially increase socket test coverage by including fixed power and ground pins that existing test methodologies often miss or don’t test cost-effectively.

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