Finding Power/Ground Defects on Connectors – Case Study

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Abstract

As printed circuit boards are steadily becoming faster, existing test technologies leave significant holes in coverage. In 2007 we presented a new approach to detecting power and ground defects using “Network Parameter Measurements”. This paper analyses the effectiveness of this technique in a high volume manufacturing environment.

1 Introduction

In this paper the “Network Parameter Measurement” (NPM) technique is evaluated by a high volume Contract Manufacturer to determine the prevalence of power and ground defects, whether they can reliably be detected at in-circuit test, and the benefits if any of detecting these defects at in-circuit test. A paper presented at the 2007 International Test Conference [PaHi07] demonstrated this new method for detecting power and ground defects on connectors.

2 Background

A paper given at the 2005 International Test Conference discussed High-Speed Signal Propagation (HSSP) and how boards that support such technology are becoming commonplace in the electronics industry [Park05]. Serialize/Deserializer technology (SerDes) was once used in high-end systems to form high-speed serial links between subsystems. Now we can pack multiple SerDes channels (both transmit and receive) into a single IC and use them to transmit serialized data with embedded clocking between ICs on a single board. SerDes technology is now becoming prevalent in low-end consumer products. PCI-Express [PCIE04] in the personal computer world is a prime example of this trend. The first wave of this standard started with serial data rates of 2.5 Gigabits/second, and will move up to 5 even 10 Gbps. Simple connectors and sockets are no longer “simple”. They become something more like a waveguide as frequency and data rate rise. Through-hole attachments common for sockets and connectors will be forced to change to ball-grid attachments. Multiple power and ground pins will continue to be important, and not simply for the mitigation of ground-bounce but also to ensure signal integrity.

3 Network Parameter Measurements

The [PaHi07] paper introduced a new method for detecting power and ground defects on connectors using existing TestJet hardware. TestJet was developed for unpowered testing for open signal pins on ICs, connectors and sockets. Figure 1 shows the basic TestJet setup. The ICT has access to the signals attached to the connector pins. All but the pin-under-test are grounded and the tested pin is stimulated with an AC signal. A sense plate is suspended above the connector so that there is a small capacitive coupling between the tip of each pin in the connector to the sense plate. (The sense plate is not inserted into the connector.) A defect-free pin will couple its AC signal into the sense plate where a buffer boosts the signal and sends it to the tester. If there is an open between the connector pin and board, then the AC signal is significantly attenuated as seen at the sense plate, indicating a defect.

Figure 1: The basic TestJet setup for testing connector pins for opens.

The [PaHi07] paper expanded this technique to...
include ground pins. When a ground pin is open due to a solder defect, as shown in Figure 2, some of the signal energy in the left hand leg is transferred to the right-hand leg where $C_{\text{Sense}2}$ can transmit it to the sense plate buffer. Depending on the various circuit element values, the buffer will see a signal that is larger than the case where the ground pin is properly attached. In some cases, it may indicate a value approaching twice the normal reading. So we have this result: a “normal” reading indicates no defect is present. A low reading indicates that the signal pin is open, and a high reading indicates the ground pin neighboring the signal pin is open.

![Figure 2: A model for the case where the ground pin is open.](image)

### 4 Open Power/Ground Defects

The [Park05] paper examined the effects of open ground pins in connectors but what does this really mean in a manufacturing environment? What does this mean to the OEM board provider? Would this defect have been caught at ICT, at functional test, or perhaps not at all? Would the defect have escaped the entire test suite and become a warranty return?

Here we will follow the production of a high volume board through the manufacturing test process to get a glimpse of the prevalence of power and ground defects and to determine the detectability of these defects using NPM. When an open ground defect is detected, the board is flagged but the defect is not fixed. We track these defective boards through the test process to determine how this defect might be detected by subsequent test steps, typically Functional Test.

#### 4.1 Functional Test

There is one other opportunity to test for open power/ground pins in connectors and sockets and this is during functional test. Functional test often occurs in a dedicated area after In-Circuit test, but before final system integration. “Hot Mockups” are often used to house a board, where it can receive power and interact with whatever backplanes, cables and plug-in boards it might encounter in real life. In this environment, special diagnostic routines are exercised that may stimulate any hidden defects still within the board. As reported in [Park05] it is possible that an open ground pin in a connector or socket could pass these functional tests and ultimately be shipped. If indeed a functional test does show a failure for this type of defect, the question becomes, where is the defect? Diagnostic resolution may be quite poor during this type of testing, leading to an inventory of suspect boards that cannot be easily fixed.

### 5 Case Study

This case study was performed by a Contract Manufacturer (CM). This CM is high volume manufacturer producing boards of varying complexity. The evaluation was performed on 459 boards. A description of the board is provided in Table 1. We note that a significant majority of the connectors were through-hole technology.

<table>
<thead>
<tr>
<th>Number of Components</th>
<th>~2000 Total</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>- 60 Connectors</td>
</tr>
<tr>
<td></td>
<td>- 1566 Analog Devices</td>
</tr>
<tr>
<td></td>
<td>- 81 Digital ICs</td>
</tr>
</tbody>
</table>

| Number of Nodes       | 3577          |
| Number of Solder Joints | ~17,000 |
| Pins NPM Testable     | 249 (of 257, 97%) |

**Table 1: Evaluation Board Description**

The board flow including yield and repair times for ICT and Functional Test are shown in Figure 3. Repair times in ICT are lower than Functional Test due to the better diagnostic accuracy of ICT.
5.1 Results

An additional 114,290 power and ground pins on 459 boards were tested as a result of using NPM. The added coverage resulted in 3 defects being detected in ICT and not passed on to Functional Test. NPM indicted an additional 3 pins that were deemed to have no defects (false calls). The false call rate of NPM is proportional to the number of pins analyzed (typically about 100 ppm) and independent of the actual defect rate. The \cite{PaHi07} paper explains how NPM determines a ground pin is defective if a neighboring signal pin reads high by approximately 3 times the per pin standard deviation. This results in a false call rate of approximately 100 ppm. Further verification of the defects were done by the troubleshoot technician either electrically or visually.

Of the three ground defects that were passed on from ICT, two were detected by the Functional Test. The Functional Test diagnosis was confirmed when the test passed after repairing the defect. One of the defects was not detected by Functional Test. Table 2 shows the results of the Case Study.

<table>
<thead>
<tr>
<th></th>
<th>ICT</th>
<th>Functional</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pins Tested</td>
<td>114,290</td>
<td>114,290</td>
</tr>
<tr>
<td>Pin Failed</td>
<td>6</td>
<td>N/A</td>
</tr>
<tr>
<td>False Calls</td>
<td>3</td>
<td>N/A</td>
</tr>
<tr>
<td>Good Calls (ICT)</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>Ave Isolation Time</td>
<td>3 min</td>
<td>15 min*</td>
</tr>
<tr>
<td>First Pass Yield (FPY)</td>
<td>49%</td>
<td>85%</td>
</tr>
</tbody>
</table>

* Insufficient data exists so a typical value was used

Table 2: Results of case study.

If we assume that the In-Circuit isolation time for a false call, to verify there is no defect, is the same as that for isolating an open, then this experiment consumed 18 minutes of repair time (6x3) while if we had not done NPM testing, 2x15=30 minutes of repair time would have been spent at Functional Test, with one defect escaping. Functional Test repairs often require a higher skilled (higher paid) technician than repairs done in ICT, so we get reduced repair costs with fewer escapes.

Were the open power and ground defects not detected in Functional Test unimportant to the proper functionality of the product, or would they have manifested themselves as warranty returns? The \cite{Park05} paper shows that the answer would be it depends on how the connector gets used. A typical PCI Express connector is shown in Figure 4.

![PCI Express x4 Connector Top View](image)

**Figure 4: PCI Express pin assignments.**

This connector has 29 pins of the 64 total pins that are not devoted to signaling, but are there to provide power and ground connections. Of these 29 pins, 18 are devoted to creating HSSP signal return paths, and are ground pins found on the right-hand side of the keyway. The other 11 pins on the left-hand side of the keyway are devoted to supplying power current at several different voltages.

The signal return path ground pins are essential to the design of the board, to assure signal integrity of the high-speed differential data signal pairs. If there is a continuity problem on a signal return ground pin, then several problems may result.

1. Loss of signal margin.
2. Increased Bit Error Rate.
3. Increased Electromagnetic Interference (EMI).

Board designers create circuits with some level of signal margin to assure that by the time a signal propagates from its source to its destination, there is sufficient signal still present to reliably transfer infor-
If a connector was (for example) rated to drive a USB cable of several different lengths, the defect might hamper the use of a 3 meter cable, but a 1 meter cable might still have sufficient signal margin to operate correctly.

6 Conclusion

The Case Study proved that NPM technology effectively detects open power and ground defects. The false call rate of NPM suggests that a second form of defect verification may be required prior to removing or repairing a part. For many parts a simple visual inspection could be used to confirm the defect but BGA type sockets might require X-ray or another type of verification.

Due to time constraints, we were unable to run a larger sample size. Since there were only 3 real defects in a sample of 114,290 power and ground pins (~26 ppm) we did not gather a lot of data on defects and NPM effectiveness. We speculate that the low open defect rate observed in this experiment was due to the large fraction of pins that were through-hole rather than surface-mount technology. We surmise that for through-hole devices, solder wetting failure is nearly non-existent. If this is true, then a test engineer may choose to not test through-hole connectors and concentrate on surface-mount connectors.

A larger case study is being planned to get a more statistically significant sample size of defects and to gain insight on some unanswered questions including: How many power and ground defects escaped NPM test? X-ray inspection of the devices under test would give us a good indication of the pin coverage of NPM. Were the defects that were not caught at Functional Test unimportant to the proper operation of the product? Further analysis should be done to determine how these defects might have manifested themselves in product quality.

7 References


[PCIE04] Search the web for “PCI Special Interest Group” or PCI-SIG. To get full details, you must be a member of PCI-SIG.