Dramatically Accelerate Debug of FPGA-based Systems using Agilent Mixed Signal Oscilloscopes

Application note 1611

Introduction

A large percentage of today’s embedded designs contain FPGAs as well as a wide variety of technologies that interface with the FPGA, including devices with analog, parallel, and serial circuits.

Using FPGA’s, enable faster and more accurate in-system debug and validation than exhaustive simulation methods and allow designers to uncover problems that are difficult to simulate.

In order to effectively debug complex systems, debug tools tailored for FPGAs are in high demand. Mixed Signal Oscilloscopes (MSOs) extend the measurement capability of an oscilloscope by adding logic timing channels to the debug environment thus enabling rapid debug of FPGA-based systems. Agilent invented MSO technology over a decade ago, as a validation tool to give engineers the ability to measure analog and digital signals simultaneously within the same oscilloscope.

This document will discuss the advantages of using an Agilent MSO with the FPGA dynamic probe application as a way to dramatically reduce validation time versus the traditional rout-out approach.
Using MSO for FPGA Functional Validation

When performing functional validation, engineers rely on the oscilloscopes logic timing channels for insight on the behavior of their FPGA design in the context of the surrounding system. A common approach is to take advantage of the programmability of the FPGA to route internal nodes to a small number (typically 8-16) of physical pins. This approach has limitations due to the fact that FPGA’s are an expensive resource and they have a relatively small number of pins available to access all the internal signals inside the FPGA. When internal signals need to be accessed that are not routed out to the available pins, the design must be changed and the node names from the FPGA must be manually mapped to the oscilloscope labels in order to keep track of the signal pathways inside the design, as shown in figure 2. This process is very time consuming and can require several iterations to complete full validation of the system.

Figure 2: Shown above is the manually mapping of the FPGA pins to the MSO
Using FPGA Dynamic Probe Application for Functional Validation

To dramatically speed up the process, Agilent Technologies has developed the FPGA dynamic probe application as an innovative approach to debugging FPGAs with an MSO. It incorporates technology that speeds instrument setup for a rapid 1st measurement, and makes successive internal measurements in seconds.

The FPGA Dynamic Probe application starts with an assessment of the internal nodes of the FPGA that can benefit from measurement access. The user then selects the appropriate core (from a list of options developed by Agilent and incorporated into either the Altera or Xilinx FPGA development system), and inserts it into the design. The inputs to the core are the potential internal nodes that can be probed by the MSO, and the outputs are routed to a set number of physical pins dedicated for debug. The debug pins are physically connected to the MSO using any of Agilent’s MSO digital probes. The debug core can be thought of as a MUX that is controlled via the JTAG connection to the FPGA offered through the standard JTAG cable used to download and program the FPGA. This whole system is controlled via software that runs on the MSO or a PC connected to the MSO. Figure 3 below illustrates how Agilent’s FPGA dynamic probe application is used in conjunction with a Xilinx ATC2 core and an MSO for FPGA debug.

Figure 3: Overview of Agilent Technologies FPGA dynamic probe Application using the ATC2 core from Xilinx.
In this section we will discuss a validation example using the Xilinx ATC2 core. The core, designed jointly by Agilent & Xilinx, is optimized for debug. It consumes minimal FPGA resources and has very little impact on device timing. The user can parameterize the core with a few or many groups of input signals. One of these input banks, selected via JTAG, will be routed to the MSO for measurement. Switching to a new group of signals is done via the FPGA dynamic probe application.

The ATC2 core was designed so that it can be placed into the design either before or after the design phase. The only requirement is the availability of a few pins in the design dedicated for debug. An overview of the application is shown in figure 4.

*Figure 4: Shows a Xilinx FPGA Example Using the Agilent Trace Core (ATC2)*
Using FPGA Dynamic Probe Application for Functional Validation

There are two key benefits when using the FPGA core that allow you to dramatically accelerate your debugging process. First, the FPGA dynamic probe application allows you to quickly setup up the MSO for an initial measurement. Second, being able to rapidly switch between signal banks allows you to measure sequential groups of signals in seconds versus hours. Because FPGA debug is iterative in nature, design teams using FPGA dynamic probe application can save up to weeks of debug time.

Figure 5: An example of functional debug using an ATC2 core by defining how many banks of signals will be needed with a Xilinx FPGA. Specify signals for each bank, and assign which pins will connect to MSO logic channels.

In the example shown in Figure 6 below, the MSO provides an effective method of viewing both the analog and digital signals of a DAC. Here we see from the capture on the oscilloscope that a glitch manifests itself on the logic channels at the height of the analog waveform. This would have been impossible to see using just the oscilloscope channels. Using the FPGA dynamic probe core-based approach to validation, the design team was able to quickly find that the design itself had a ROM load defect that caused the processor to load the wrong sine value.
Both major FPGA vendors offer royalty-free MSO debug cores that were originally designed for logic analyzers. Since MSOs have logic channels, the debug cores make a great fit for an MSO to increase debug productivity and can save up to weeks of time. It does this by having the ability to quickly setup up the MSO for an initial measurement and by being able to rapidly switch between signal banks to measure sequential groups of signals in seconds versus hours.

The Xilinx core, for example, comes as a standard component in Xilinx ChipScope Pro and can be added to a design using Core Inserter without modifying the original HDL code. Altera offers LAI core as a standard part of their Quartus 2 development environment. Most functional debug using an MSO is done with a state core. The ATC2 core outputs data flow and control signals on each clock cycle. The MSO captures this using the digital channels. To trigger on an event, for example, the MSO can be set to trigger on the desired pattern and ATC2 clock edge. LAI and ATC2 can be parameterized as either state cores or timing cores.
State core

Figure 7 shows how the ATC2 state cores minimize impact to device timing by implementing multi-stage pipelining. The thick lines show the flip flops and routes added by ATC2. Since there is a flip flop “in the fabric” in addition to one at the I/O buffer, the router can use timing solely within the ATC2 core to move across the chip.

Timing core

Timing cores are used less frequently, and are intended as a method for making measurement across multiple time domains, or for searching for internal glitches. Timing cores create paths from measured signals to IO using just routing paths with no flops. The load added to a signal is simply a wire and hence in most cases the change in device timing is negligible. If two or more signals were shown on this diagram, each would typically have a different path length. This skew can be found in a timing report and is not compensated for by the MSO. For this reason, state cores are better for functional debug.

Figure 8. Shows the thick lines that represent the routes added by ATC2 timing cores.
Because of the low development costs and reprogrammability of FPGA-based systems, they have become the centerpiece of embedded design. Using FPGA's enable more precise and faster in-system debug validation than traditional methods. In order to keep pace with the needs of design teams using FPGAs, Agilent MSOs incorporate powerful features by extending the capabilities of a digital scope with logic channels to display control signals, state machine behavior, and data flow. The FPGA dynamic probe application gives designers the ability to make effective use of MSO logic channels over a few debug pins and yields rapid debug results of FPGA-based systems. This innovative application allows you to access signals internal to the FPGA, unlike the traditional method of being limited to signals at the periphery of the FPGA. This allows for more flexibility in the debug process and reduces the amount of time needed for functional validation. By having the ability to make multiple measurements in seconds versus hours of code changes and rerouting of signals, you can easily measure different sets of internal signals while keeping the timing of the system constant. This allows you to leverage the work done in the design environment by mapping internal signal names from your FPGA design tool to the Agilent MSO, whereby eliminating unintentional mistakes. The FPGA dynamic probe application used in conjunction with an Agilent MSO provides an efficient and effective solution for debugging systems incorporating Xilinx and Altera FPGAs.

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