Agilent EEsof EDA

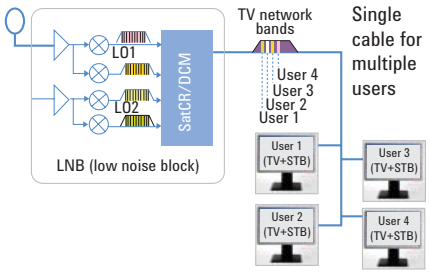
STMicroelectronics, Home Division "1-GHz Digital Channel Multiplexer for Satellite Outdoor Unit Based on a 65-nm CMOS Transceiver"

Case Study

At both ends of the silicon provider chain, Agilent SystemVue accelerates mixed-signal behavioral model and silicon validation

"With Agilent SystemVue 2008, we were able to create our system architecture quickly and then begin verifying the C-code implementation. It was easier than with other ESL software environments, and the easy licensing and configurations allowed our distributed team to share results to meet this challenge quickly. Agilent's new environment has a bright future. "

Pierre Busson
Advanced AMS architecture expert, digital communications, STMicroelectronics



The Company

STMicroelectronics makes commercial ASICs that enable high-volume consumer applications.

The Challenge

A single building may have multiple satellite antennas and cabling for each end-user. A single satellite transponder with a digital channel multiplexer (DCM) system can reduce the cost and complexity of this user equipment, but requires wide frequency bandwidth and high-performance signal processing capable of overcoming physical distribution effects. Due to the high development investment for custom ASICs, STMicroelectronics needed to quickly assess the real-world coded performance of PHY architectures, including the physical channel, and parameterize the effect of impairments on the system to ensure robustness of both the architecture and its proposed implementation.

The Solution

Agilent SystemVue was used to design the DSP channel filtering and, evaluate and validate overall system performance. SystemVue was also used to verify hand-generated algorithmic code against GUI blocks in the front end of ST's model-based design flow. Other CAD tools were then used to complete the overall ASIC floorplanning and hardware design flow.

The key features of SystemVue 2008.12 that enabled this include:

- Ease in combining GUI-based blocks with math-language and C++ algorithmic blocks
- Polymorphism, to easily verify implementations
- Envelope-based dataflow simulation with RF effects
- Direct links to Agilent test equipment

Agilent Technologies

The Results

A high-performance system was architected across a distributed multi-site team, and passed to hardware design with high confidence. The results were presented at the ISSCC 2009 conference in February 2009, available through IEEE.

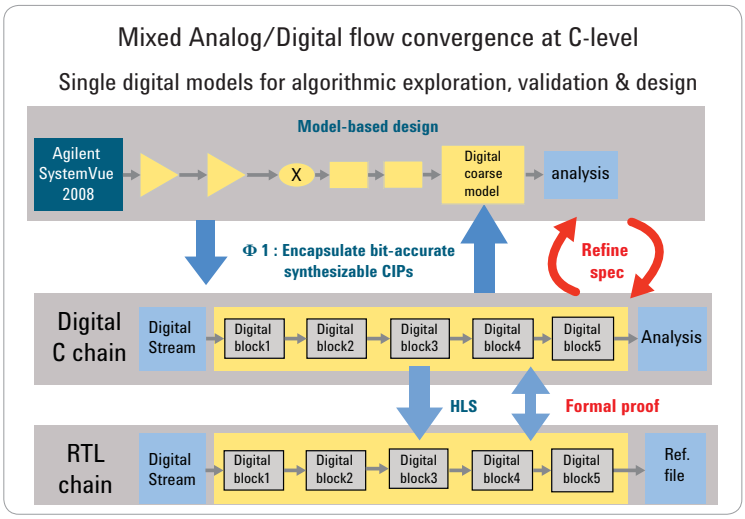


Figure 1. Using Agilent SystemVue in a model-based design flow, based on C

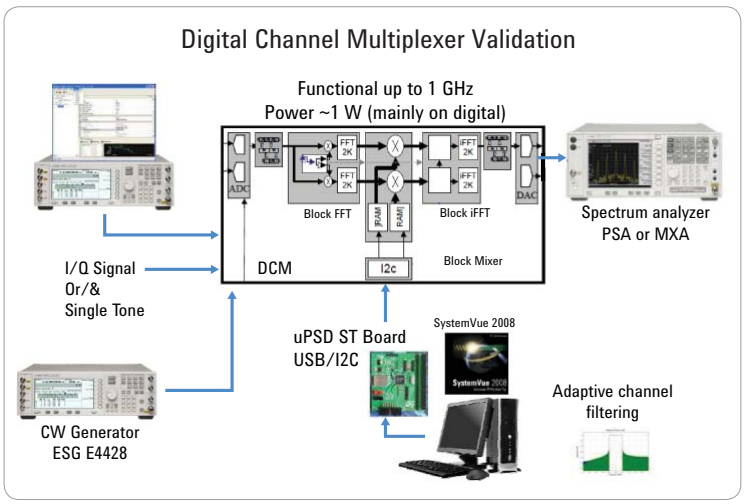


Figure 2. Agilent SystemVue within an Agilent-based hardware PHY verification suite

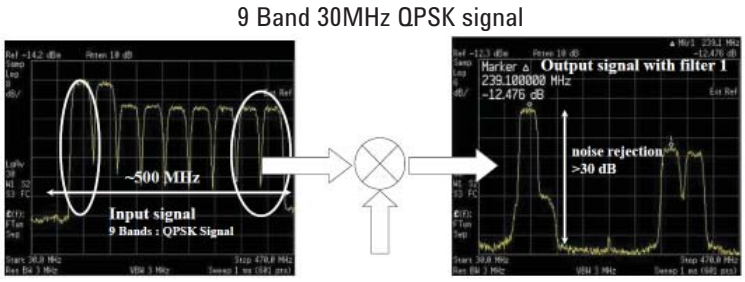


Figure 3. Measured performance of channel filtering, designed with Agilent SystemVue

CUSTOMER:
STMicroelectronics, Crolles, France

CHALLENGE:
To rapidly evaluate and prototype real-world effects on a high-performance wideband PHY architecture for satellite communications

SOLUTION:
SystemVue from Agilent EEsof EDA

RESULTS:
- Validated baseband design before hardware was available
- Saved valuable R&D development time
- Achieved early digital RF partitioning

Web Information

For more information about STMicroelectronics, visit www.st.com

For more information about Agilent Technologies SystemVue, visit our Website:
www.agilent.com/find/eesof-systemvue

Product specifications and descriptions in this document subject to change without notice.

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