

IEEE 1588v2 Precision Time Protocol Emulation Software N5568A

Data Sheet

The most comprehensive solution for verifying the IEEE 1588v2 Precision Time Protocol (PTP).

Rapidly test the operation, performance, and scalability of Transparent, Boundary, Master, and Slave Clock devices and systems to ensure frequency and time-of-day synchronization.

Key Features

- Verify PTP implementations to IEEE 1588v2 with emulated Masters and Slaves
- Test scalability with thousands of Slave Clocks
- Measure Transparent Clock Correction Factor accuracy under load
- Validate Best Master Clock algorithm & failover
- Stress multicast/unicast and End-to-End/Peer-to-Peer behavior
- Check PTP packet prioritization under traffic loads



Product Overview

Agilent N2X is the industry's most comprehensive test solution for testing the development and deployment of network services for converging network infrastructures. Network operators, network equipment manufacturers (NEMs), and component manufacturers can verify service attributes of entire networks End-to-End, while also isolating problems down to individual networking devices and subsystems. Agilent N2X delivers unparalleled test realism to verify the ultimate performance, scalability and resilience of carrier grade services and infrastructure.

The N5568A IEEE 1588v2 Precision Time Protocol Emulation software complements the N5566A Synchronous Ethernet ESMC Emulation software and the N2X G.8261 Traffic QuickTool to make N2X the most comprehensive Timing-over-Packet (ToP) test solution available.

The N5568A software is also one component of the N2X Carrier Ethernet test solution, which includes emulation and conformance testing of technologies such as Synchronous Ethernet, CFM, Y.1731, Link OAM, LACP, STP, RSTP, MSTP, BFD, L2oMPLS, VLANs, MEF 9, MEF 14 and MEF 21.

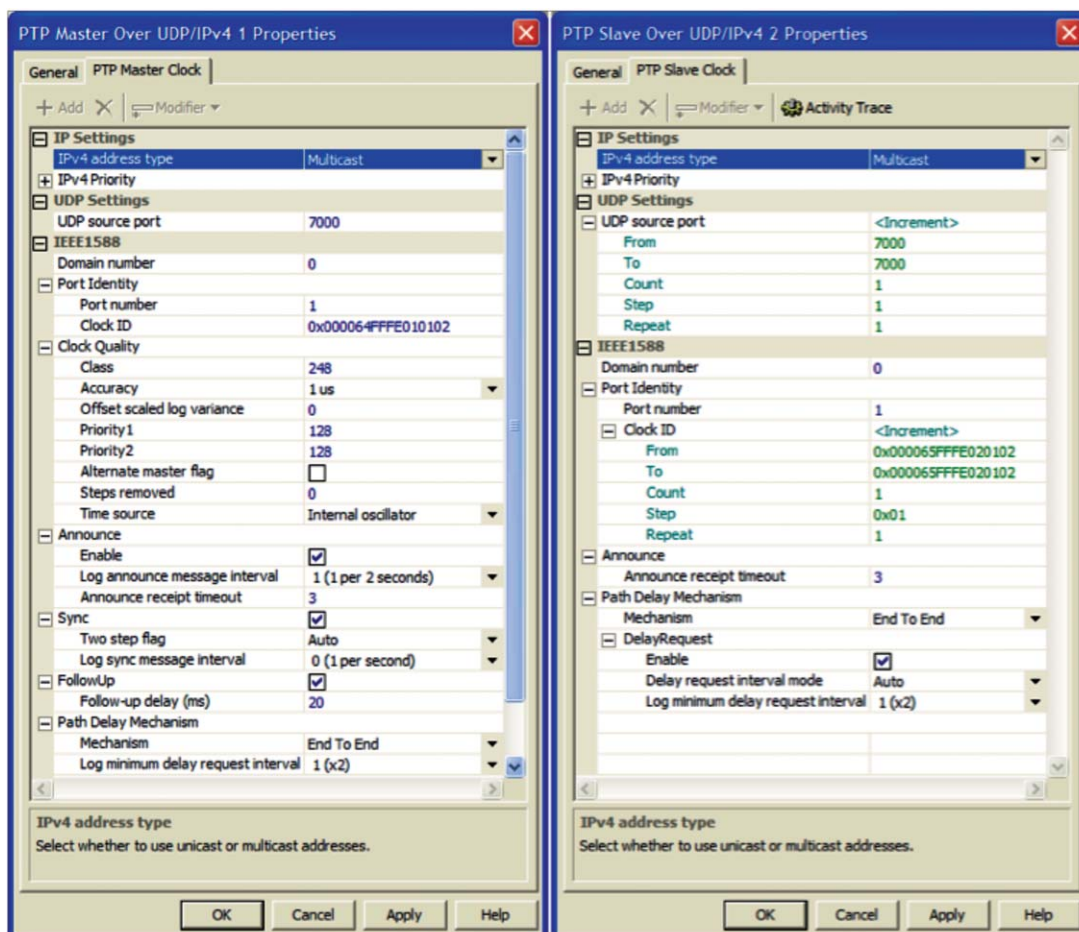
The N5568A application enables interactive testing of the IEEE 1588v2 Precision Time Protocol that underpins timing synchronization in applications such as wireless backhaul and industrial automation where distribution of a frequency-locked and/or time-locked reference clock is vital. N2X enables flexible simulation of Master Clock and Slave Clock devices to measure device or system performance under load, to quantify system scalability, and to fully stress and characterize behaviors such as Best Master Clock selection.

Product Features

Verify PTP implementations to IEEE 1588v2 with emulated Masters and Slaves

The N2X N5568A PTP software emulates Master Clocks and Slave Clocks, facilitating rapid and easy testing of devices and systems against the IEEE 1588v2 Precision Time Protocol standard.

- Validate proper PDU encoding (message encapsulation)
- Verify PTP state-machine behavior interactively
- Load the system with multiple Masters and Slaves, across multiple domains, with low and high message rates (Sync, Follow-Up, Delay-Request, Delay-Response, Peer-Delay-Request, Peer-Delay-Response) to quantify scalability
- Scale tests to a large number of ports simultaneously to verify system behavior and performance under real-world and extreme loads



Comprehensively test IEEE 1588v2 devices using normal and abnormal emulation parameters

Full control of the N2X PTP Clock emulations enables comprehensive functional, performance and scalability testing of devices and systems that support IEEE 1588v2.

- Emulate and mix one-step and two-step Master and Slave Clocks;
- Control Emulation performance behaviors, such as Follow-up delay, to emulate immediate or highly delayed Follow-up messages – this can have a huge impact on system performance;
- Fully configure Master Clock and Slave Clock pool/instance properties including Unicast/Multicast modes and addresses, one-step/two-step behaviors, Unicast negotiation, QoS levels, domains, Clock IDs, Reported Clock Quality parameters, E2E and P2P parameters, Announce/Sync/Delay-Request message intervals, and message timeouts;
- Interactively change parameters (such as message rates) while the test is running;
- Independently use the traffic generator on the same ports to load the data plane of the system-under-test (SUT);
- Track PTP state and statistics (such as received clock identity and quality attributes) in real time without having to setup complicated capture filters or manually examine PTP PDUs in the capture buffer;
- Emulate a Master clock and multiple Slave clocks across multiple ports and domains, and vary message rates to quantify behavior under PTP load;
- Measure critical performance parameters in real-time, such as Correction Factor error (CF error), Offset from Master, and Mean Path Delay;
- Monitor PTP time values (T1, T2, etc) for detailed troubleshooting.

Test scalability with thousands of Slave Clocks

N2X emulates many Slave Clocks across multiple domains and multiple ports simultaneously, with different Delay-Request and Peer-Delay-Request message rates that can be mixed and interactively varied in groups known as device pools. This enables you to fully load and test the ultimate scalability of Master, Boundary, and Transparent Clocks, and measure their performance under realistic and extreme conditions.

For network designers, the selection and placement of Boundary and Transparent Clocks and the specification of the GrandMaster are critical decisions that must balance timing performance and reliability, cost, and flexibility for future network expansion. N2X enables clock scalability to be fully tested and quantified, allowing network designers to have complete confidence in their product selection and network topology.

N2X also emulates Master Clocks across multiple domains and ports at the same time – and on the same ports as emulated Slave Clocks – to fully surround and load a Boundary or Transparent Clock or to comprehensively test a Slave Clock that must operate in a single- or multi-domain network.

Name	Count	State	Action Control	Tester IPv4
Port 6501/1 (Ethernet-GbE) - 1 device				
<input checked="" type="checkbox"/> PTP Master over UDP/IPv4 1	1	-		100.1.1.2
<Double-click here to add Routing/Access protocol emulations.>				
Port 6501/2 (Ethernet-GbE) - 500 devices				
<input checked="" type="checkbox"/> PTP Slave over UDP/IPv4 2	200	-	-	100.2.2.2 -
<input checked="" type="checkbox"/> PTP Slave over UDP/IPv4 3	300	-	-	100.2.3.2 -
<Double-click here to add Routing/Access protocol emulations.>				
Port 6501/3 (Ethernet-GbE) - 500 devices				
<input checked="" type="checkbox"/> PTP Slave over UDP/IPv4 4	500	-		100.3.4.2 -
<Double-click here to add Routing/Access protocol emulations.>				
Port 6501/4 (Ethernet-GbE) - 500 devices				
<input checked="" type="checkbox"/> PTP Slave over UDP/IPv4 5	500	-		100.4.5.2 -
<Double-click here to add Routing/Access protocol emulations.>				

Emulate Master Clocks and pools of hundreds of Slave Clocks per domain and port to test system scalability

Measure Transparent Clock Correction Factor accuracy under load

Agilent's "Correction Factor Error" (CF Error) measurement methodology is used by leading vendors to characterize and benchmark Transparent Clock performance. For a white paper about the CF Error test methodology and example results, please visit www.agilent.com/find/n2x.

N2X allows you to rapidly measure and monitor the Correction Factor Error of a single or chain of Transparent Clocks. The reported Correction Factor associated with each and every PTP Sync Message is compared against the actual PTP residence time (packet forwarding delay) using N2X hardware timestamps, enabling per-packet and aggregated CF Error statistics to be measured across each and every Slave Clock device pool, domain and test port.

Because the N2X emulated Master and Slave Clocks use the same backplane clock and time base, CF Error measurement does not require the connection of additional cabling between N2X test cards or chassis.

Correction Factor Error	
Minimum	000:00:00.000000850
Average	000:00:00.000002200
Maximum	000:00:00.000007320

Interactively measure Correction Factor Error to rapidly quantify Transparent Clock performance

Once the baseline Correction Factor Error is measured, the test can be repeated under a huge range of extreme and realistic traffic, control-plane and PTP stresses to quantify Transparent Clock performance under load.

Validate Best Master Clock algorithm & failover

N2X comprehensively tests the correct operation, speed, and scalability of the Best Master Clock (BMC) algorithm implementation within Transparent, Boundary, and Slave Clocks, and verifies that Master Clocks perform correctly in the presence of other emulated Master Clocks that are on the same and/or different clock domains.

Key BMC test scenarios:

- Selection: Test the accuracy and speed of Best Master selection.
- Failover: Emulate a failing Master, verify that the next-best Master is selected accurately, and measured the failover speed.
- Flapping: Interactively shutdown and bring up an emulated Master Clock by stopping and restarting Announce or Sync messages to simulate the Best Master going in and out of service rapidly and repeatedly, to test time-outs and verify the operation and stability of the BMC algorithm within a single clock or a system of clocks.
- Quality Variation: Vary any of the reported Clock Quality attributes of an emulated Master interactively to verify conformance to the subtle BMC behaviors specified in IEEE 1588.
- Resilience: Inject incorrectly formed Announce messages to verify the resilience and stability of Best Master selection.
- Domain Interaction: Emulate Masters on multiple domains and change the reported quality of the Master on a reference domain, to ensure that Clocks correctly distinguish between domains and are able to process multiple domains at the same time.
- User, Control, and PTP Load: Repeat the above tests with three types of load: user-plane traffic load; control-plane load (such as Rapid Spanning Tree Protocol flapping); and PTP message load (by emulating hundreds or thousands of Slaves, with different rates of PTP Delay-Request messages) – all on the same port(s) at the same time.
- Correction Factor Accuracy during failover: Monitor the Correction Factor Error of the Transparent Clock Device-Under-Test during a BMC failover, and verify that the Transparent Clock performance does not suffer.

N2X tracks and displays the current Best Master in each domain in real time (by source IP address, clock ID, class, accuracy, priority, time source, etc) and time-stamps the last change, to enable instant identification of Best Master changes and interactive measurement of BMC performance.

Best Master Clock	
Source address	100.1.2.2
Last change	000:10:24.096
Grandmaster clock ID	0x000064FFFE020102
Class	248
Accuracy	1 us
Offset scaled log variance	0
Master priority 1	128
Master priority 2	128
Steps removed	0
Time source	InternalOscillator
Source port clock ID	0x000064FFFE020102
Source port number	1

Interactively test Best Master Clock performance by observing BMC identify and last-change timestamp

Stress multicast/unicast and End-to-End/Peer-to-Peer behavior

N2X supports a wide variety of PTP operational modes that can be mixed on the same test port(s) to verify different user profiles and network configurations, to help uncover unwanted behaviors and system interactions:

- Emulate unicast mode with manual configuration, unicast mode with signaled configuration, multicast mode, and 'mixed' mode (in which the Master and Slave operate in different modes), and mix these modes on the same test port and in the same domain;
- Emulate End-to-End (E2E) and Peer-to-Peer (P2P) delay mechanisms, and mix both these modes on the same test port and in the same domain;
- Emulate one-step and two-step Master and Slave Clocks on the same port and in the same domain.

Check PTP packet prioritization under traffic loads

N2X can emulate Slave and Master Clocks and generate user traffic on the same test ports with user-settable packet priorities (Type-of-Service/DiffServ Code Point bits), also known as QoS levels, for both the PTP and user packets. This allows you to saturate one or more interfaces to verify that:

- PTP messages are given priority over user packets;
- User packets are preferentially dropped when an egress port is oversubscribed;
- PTP packets do not suffer adverse packet delays or packet delay variation under congestion conditions.

In addition, you can test the priority of PTP multicast packets in the presence of high-priority user traffic (such as VoIP unicast streams, IPTV multicast streams and stateful TCP data streams).

IP Settings	
IPv4 address type	Multicast
IPv4 Priority	
<input type="radio"/> No code point	-
<input checked="" type="radio"/> Type of Service Code Point	
Precedence	Network Control
Delay	Low
Throughput	High
Reliability	Normal
Unused	0x0
<input type="radio"/> Differentiated Services Code Point	
<input type="radio"/> Default	-
<input type="radio"/> Class selector	-
<input type="radio"/> Assured forwarding	-
<input type="radio"/> Expedited forwarding	-
ECN	-
Calculated IPv4 priority (binary)	11111000
Calculated IPv4 priority (hex)	0xF8

Set PTP QoS levels to verify PTP packet prioritization under load

Simulate sophisticated PTP DDoS attacks

Generate large volumes of PTP messages to simulate sophisticated and brutal Denial-of-Service (DoS) or Distributed Denial-of-Service (DDoS) attacks on a Clock device or system, to verify resistance to potential threats:

- Using the N2X Master Clock emulation, emulate multiple rogue Masters (with correct stateful behavior or with incorrect behavior, such as missing Announce or Sync messages) in multiple clock domains across multiple interfaces, with different addresses and clock IDs.
- Using the N2X Slave Clock emulation, emulate multiple pools of rogue Slave Clocks on each interface with high rates of Delay-Request messages (above the negotiated Delay-Request Interval).
- Using the N2X PDU builder and field modifiers, create and send high rates of PTP PDUs with random or rapidly cycling field values (such as Announcement messages with varying Clock Quality) to simulate stateless DDoS attacks.

Perform Negative and Abnormal testing

Essential to interoperability testing is the establishment of DUT behavior in the event of an unexpected or malformed PDU, or behavior that does not conform to the IEEE standard.

Negative testing is built into the PTP emulation, enabling simulation of misbehaving peer devices and testing of the SUT under out-of-specification conditions. For example:

- Create emulated Master Clocks with undefined Clock Class values;
- Selectively disable emulated Master Clock messages, such as Announce, Sync and Follow-Up, to verify the robustness of Transparent Clock and Slave Clock state machines;
- Send Follow-Up messages with the Two-step mode flag set to “One-step”;
- Set unrealistically large delays between Sync and Follow-Up messages to stress Slave Clock timing recovery;
- Emulate PTP Clocks with QoS levels lower than that of user traffic;
- Send Delay-Request messages from an emulated Slave Clock faster than the Master allows.

In addition, N2X's flexible XML-based PDU builder allows you to easily create and transmit (via the GUI or API) non-conforming PTP PDUs. For example:

- Create malformed Announce or Sync messages;
- Inject PTP Sync messages at abnormally high message rates to stress a Transparent or Slave Clock;
- Inject PTP Delay-Request messages at abnormally high message rates to "build state" and try to overflow the resources of a Master, Boundary or Slave Clock.

You can also edit or extend the N2X XML files using a simple text editor to create non-standard PTP PDU definitions with additional TLVs. This can also be useful for tracing a PTP message through a system during troubleshooting.

Introduce control-plane loads such as STP and routing

N2X can emulate multiple layer-2 to layer-7 protocols at the same time as PTP, on the same test ports, to fully load the control-plane processing capabilities of the system-under-test. This ensures that your system will perform under the normal and extreme conditions found in real networks.

Here are just a few of the test scenarios possible:

- **Spanning Tree Blocking** – Emulate Spanning Tree Protocols (STP, RSTP, and/or MSTP) on N2X, and ensure that the SUT forwards PTP packets through blocked ports.
- **MPLS and Route Flapping** – Flap routing protocols (OSPF, RIP, IS-IS, BGP-4) and exercise signaling protocols (RSVP, LDP) to simulate network instabilities, to verify PTP packet forwarding and measure PTP performance under extreme control-plane loads.
- **Multi-protocol Load** – Stress the SUT with Ethernet OAM Connectivity Fault Management (E-OAM CFM), Link OAM, BFD, PBB, VPLS, and MEF UNI signalling traffic to ensure stability, characterize feature interaction with other protocols and uncover unwanted behaviors.
- **Service Disruption** – Test the impact of MPLS Fast Reroute, LACP failover, and route reconvergence on PTP operation and performance.
- **Multicast Stress** – Exercise IPv4 and IPv6 Multicast protocols such as PIM-SM, IGMP and MLD to stress and attempt to disrupt Multicast PTP packet forwarding.

Applicable Standards

- IEEE Std 1588-2008 (1588v2) IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems (published 24 July 2008)

Configuration and Ordering Details

Hardware

To use the N5568A IEEE 1588 Precision Time Protocol Emulation software, the following Agilent N2X hardware and software are required.

A N2X system is required with:

- System controller
- Chassis
- One or more Ethernet Test Cards

The N5568A software is supported on all N2X Ethernet test cards except the N2X XP or XP-2 test cards, which do not support protocol emulations.

Software

Required software packages:

- E7881B Packets and Protocols Application Software

Optional complementary software packages:

- N5556A Synchronous Ethernet ESMC Emulation Software
- N5580A Spanning Tree Protocol (STP, RSTP & MSTP) Emulation Software

Please contact your local Agilent representative to help configure and order an N2X test system.

Online Help

An extensive online help system provides complete descriptions and detailed usage instructions for every component of N2X. Dialog-level, context-sensitive help provides rapid access to the relevant sections of the online help.

Technical Specifications

Major Operational Modes

Encapsulations	UDP/IPv4,
PTP Packet Forwarding	Signaled Unicast, Manually configured Unicast, Multicast
Delay-Request Mechanisms	End-to-End, Peer-to-Peer
State-Machine Modes	One-step, Two-step

Key Configuration Parameters

Reported Clock Quality Parameters	Class, Accuracy, Offset scaled log variance, Priority 1, Priority 2, Alternate master flag, Steps removed, Time source
Timing Messages	Sync, Delay-Request, Delay-Response, Peer-Delay-Request, Peer-Delay-Response
Other Messages	Announce, Unicast negotiation, Management (via PDU builder)

Key Emulation Statistics

Message Counts	Received and Transmitted Messages (by type), Totals, Received Intervals Attributes
Key Measurement Types	Emulation State, Correction Factor Error, Sequence Errors, Best Master Clock (ID and timing), Slave OFM and MPD, Emulation States
Debug Mode for Troubleshooting	History of Sequence ID, T1, T2, T3, T4, Correction Factor and other details



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Revised: October 1, 2009

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Printed in USA, October 13, 2009
5990-4884EN

