



Throughput Comparison Between Agilent *Medalist* i3070 Series 5 and Predecessor i3070 In-Circuit Test Systems – A Production Floor Case Study

Case Study

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Abstract

Agilent's new *Medalist* i3070 Series 5 in-circuit test system is designed to enhance throughput. This case study evaluates the increase in speed of the Series 5 tester compared with its predecessor, the i3070 series. Results showed an overall improvement in test time by almost 30% for the Series 5 compared with the i3070.

Background

The Agilent *Medalist* i3070 Series 5 in-circuit test system is equipped with advanced double density pin cards (12 MPs) and the new analog stimulus and response unit (ASRU) "N" revision card. The ASRU-N includes a new digitized measurement circuit (DMC) and digital signal processing (DSP) algorithm. These new features speed up the analog testing while maintaining the original measurement operational amplifier (MOA) circuit for users who prefer more accurate measurements. In addition, the advanced double density pin cards will also improve digital test throughput.

Overall, customers will experience about 20% to 30% improvement in test times, which translates into higher production throughput and revenue.



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Evaluation objective and board information

The evaluation was conducted for a computer motherboard produced at a high volume production contract electronics manufacturer (CEM) site in Asia. The evaluation objective was to compare the difference between the customer’s existing *Medalist* i3070 and the new *Medalist* i3070 Series 5 in terms of:

- a) Test throughput
- b) First pass yield (FPY) and false reject rate (FRR)

Table 1 below shows a summary of the project information. This computer motherboard is chosen due to its large numbers of analog and digital components, which will provide substantial data for our analysis.

Table 1.

Board information	
Board type	Computer motherboard
Number of nodes	1259
Number of analog components	1670
Number of digital components	44

Conversion process

There are two methods to convert the unpowered analog tests. The purpose for both approaches is to add in the “as” option via an off-line computer without affecting the production system time. These two methods are:

- I. Manual editing using the graphical user interface
- II. Re-running of the interactive program generator (IPG)

In this evaluation, manual editing is chosen to mass edit the unpowered analog test source files.

For speed-up digital tests, change the ‘vector cycle’ and ‘receive delay’ statement to 80 n and 70 n respectively.

Upon completed the editing, first run and debugging are needed to make the analog and digital tests pass consistently with a known good board. All the advanced boundary scan tests and most of the digital tests are passed at the first run without further changes to the vector cycle. However, some digital tests need to be adjusted to their optimal vector cycles due to the characteristics of the digital components.

The efforts required to convert, debug and run test program in the speed-up modes are show in Table 2 below.

Table 2. Efforts required to convert test program

	Analog tests	Digital tests
Number of tests	672	51
Conversion time	0.75 hour (off-line)	0.50 hour (off-line)
Debug time	4.5 hours	1.00 hour

Evaluation process

Test throughput

Firstly, ten known good boards are chosen to run on the *Medalist* i3070. Test time is collected after tests are matured (after at least three cycles of execution). The same steps are repeated for the *Medalist* i3070 Series 5.

Table 3 shows the average test time results obtained. The test throughput improvement enabled by the Series 5 ICT system is evident, with board cycle time reduction by over six seconds, which is about 28% improvement. Do note that the tests have been optimized using the auto optimizer feature which is available in earlier software versions.

Table 3. Summary of test times

Component	i3070 time (sec)	Series 5 time (sec)	Improvement (sec)	Improvement (percentage)
Capacitor	2.692	2.056	0.636	30.93%
Inductor	0.133	0.081	0.052	64.20%
Resistor	5.665	4.311	1.354	31.41%
Total sub analog time	9.458	7.355	2.103	28.59%
Boundary scan powered shorts	2.547	1.183	1.364	115.30%
Boundary scan interconnect	0.920	0.244	0.676	277.05%
Boundary scan in-circuit	3.695	1.931	1.764	91.35%
Digital in-circuit	0.233	0.205	0.028	13.66%
Total board test time	29.12	22.755	6.365	27.97%

First pass yield and false fail rate

A total of 428 boards are used to benchmark the first pass yield (FPY) and false reject rate (FRR). Two true failure boards are intentionally added into the sample size. These boards are first tested on *Medalist* i3070, and the same sample boards are used on *Medalist* i3070 Series 5.

Results show that with the Series 5, system performance is maintained with a concurrent increase in test throughput, as can be clearly seen from the data in Table 4.

Table 4. Summary of first pass yield and false reject rate

System	Total	Passed	Failed	True failure	False failure	First pass yield (%)	False reject rate (%)
i3070	428	415	13	2	11	96.9%	2.5%
i3070 Series 5	428	414	14	2	12	96.7%	2.7%

Customer benefits

Table 5 shows potential achievable savings with the assumption of 20% throughput improvement, and the system performance maintained, based on the results shown above. Table 6 shows potential revenue generated (approximately USD \$900,000 per annum) with production volumes increased.

Table 5. Throughput increase benefits

	i3070	Series 5
Throughput increase	N/A	20%
Target volume per day	2000	2400
First pass yield	97%	97%
Actual board volume per day	1,940 pieces	2,328 pieces
Actual board volume per week (5 days)	9,700 pieces	11,640 pieces
Actual board volume per month (20 days)	38,800 pieces	46,560 pieces
	Quantity	
Net increase per day	388 pieces	
Net increase per week	1,940 pieces	
Net increase per month	7,760 pieces	

Table 6. Revenue increase benefits

Assumed product margin	US \$10	Time frame
Increase in margin from the increase in volume	US \$3,880	Day
	US \$19,400	Week
(Assume 5 work days per week)	US \$77,600	Month
(Assume 20 work days per month)	US \$931,200	Year

Conclusion

The evaluation results show that test times can be sped-up by six seconds without compromising the system performance. The throughput, first pass yield and false reject rate were evident with the increase in production volume. Based on data from this evaluation, the CEM initially upgraded seven i3070 systems to take advantage of the benefits enabled by throughput enhancements.

The customer subsequently upgraded another 15 systems after three months of successful runs on their newly upgraded systems to maximize their return on investment.



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Revised: July 8, 2010

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Printed in USA, August 11, 2010
5990-6378EN



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