Innovations in EDA: A Practical Approach to Verifying RFICs with Fast Mismatch Analysis

Eliminate Traditional Simulation Bottlenecks While Gaining New Insights

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Webcast: October 28, 2010



Agenda

- **Overview of RFIC Verification**
- The Problem of Mismatch
- Simulating Mismatch The Good, The Bad and The Ugly
- A Simplifying Assumption
- Introducing Fast Yield Contributor Analysis (FYC)
- **FYC Circuit Simulation Examples**
- LNA Supply Current Analysis (DC)
- VCO CR Analysis (CR)
- Receiver Gain Analysis (CR)

Review and Additional Resources



Overview of RFIC Verification

Why is Verification Critical for Advanced RFICs?

- Silicon is the technology of choice for both mainstream and emerging Wireless applications:
 - GSM, WCDMA, WIMAX, LTE, WiFi ...
 - Silicon mmWave (WirelessHD, WiGIG) and CMOS PAs & CMOS-SOI RF Switches
 - Most wireless design starts now in advanced CMOS technology nodes
 - Increased process variability, technologies not necessarily optimized for RF and mmWave
- Extremely complex and dense RF and mixed signal circuitry that interact
- Increased pressure to get wireless products to yield at volume





Overview of RFIC Verification

What is it?

• Simulating the performance of RF circuits using various sets of device parameters, operational parameters or sampling of statistical device models.

What are the different types of verification I can perform?

- Nominal: Most anticipated operating and process conditions
- Worse Case, Corners, ProcessVoltageTemperature (PVT)
- Monte-Carlo based PVT & Mismatch Analysis
- Operational Analysis





Overview of RFIC Verification Worse Case, Corners, PVT

Worse Case, Corners, PVT: Simulation with parameter sets based on the assumption that only few parameters effect performance:

- Oxide thickness, threshold voltage, sheet resistance, electron mobility etc
- Supply voltage, operating temperature, circuit configuration
- Names include Typical, Fast, Slow for various configurations of different devices (nmos/pmos: TT, FF, SS, FS, SF)

Why use it?

- Only a handful of simulations required
- Historically been the signoff run set especially where application/circuit oriented corners have been defined

Limitations:

- Application/circuit worse case/corner models may not be available for RF
- What does Fast or Slow mean with respect to RF metrics like NF or IIP3?
- Gives limited insight into where the actual problem is located in your design



Overview of RFIC Verification Monte-Carlo PVT, Mismatch Analyses

Monte-Carlo PVT & Mismatch: Simulations based on random or directed sampling of statistical device models built from analyzing how device characteristics vary from die to die, wafer to wafer, and lot to lot.



MC-Process vs MC-Mismatch

- MC-Process Models Global Variations
 - Large Scale Wafer to Wafer etc
- MC-Mismatch Models Local Variations
 - Small Scale Transistor to Transistor



Analyze Performance Variation and Correlation



Overview of RFIC Verification Monte-Carlo PVT, Mismatch Analyses Cont

Statistical Device Models are Available from All Silicon Foundries

Why Aren't Design Engineers Running MC-Process to Evaluate Performance Variation?

- Long simulation times: Larger, more complex RF designs with layout parasitics
- Prohibitively expensive to run the 1000s of required simulations
- Limitations of Standard Monte-Carlo Techniques:
 - Can tell you that you have a problem (excessive variation) BUT:
 - It CAN'T tell you what the source is or to what degree it impacts the results.
 - It CAN'T tell you how the various circuits and blocks interact to impact yield As a result, Most RFIC Designers only run Worst Case/Corners and Mismatch

While there are ways to reduce both the number and cost of MC-Process analysis, this Webcast will focus on improving techniques that RF Design Engineers actually use:

MC-Mismatch Analysis



The Problem of Mismatch Why is Mismatch So Important?

Modern electronic circuitry depend heavily on the concept of matched circuitry. There are many benefits to matching transistors in RFIC designs:

• Undesirable transistor characteristics can be eliminated

- At least to a first order

- Device voltages and/or currents can be duplicated elsewhere in the circuit
 - Many circuits use this technique
- Differential circuits can be created, improving signal-to-noise ratios
 - Critical as supply voltages increase
- Many other applications depend on matching



The Problem of Mismatch What Happens When Transistors are Mismatched?

Of course no two transistors are exactly the same. As device geometries decrease, these mismatches tend to account for a larger percent of the total device. This mismatch between devices has many undesirable effects:

- Circuitry may not be biased at the desired operating point
- Differential circuitry may produce undesirable DC offsets
- Spurious signals are produced which would not exist in a perfectlymatched design

The effects of these mismatches must be quantified prior to manufacturing in order to confirm operation to specifications.



Simulating Mismatch How is it Done?

Fortunately, most modern RFIC PDKs include models for mismatch effects:

- Spectre-formatted PDKs include mismatch effects for use within Monte Carlo analysis
- All transistors within a given hierarchical block are mismatched from each other





Simulating Mismatch So What is the Problem?

Having support in the PDK is one thing. Actually simulating mismatch is another thing entirely!

- Turning on mismatch in Monte Carlo analysis causes EACH transistor to have a different model parameter set
 - This can increase memory consumption by a factor of 10X or more
 - Simulation times can increase dramatically
- Because mismatch effects tend to be a random function, Monte Carlo analysis is required to fully characterize the circuit impact
 - 100s or 1000s of simulations may be required!

The impact is simulations which either require beyond 1000X nominal simulations or simply outgrow compute resources!



A Simplifying Assumption What Can Be Done to Speed Mismatch Simulations?

A popular simulation technique used to speed up slow simulations is to make a simplifying assumption.

- RFIC designers are already very familiar with this approach!
 - AC, SP and SSNA analysis use a small-signal assumption allowing the assumption that certain circuit characteristics are linear
- Fortunately, an assumption similar to the small-signal assumption can be applied to speed mismatch analysis!
 - Let's call it a SMALL-VARIATION assumption...

The rest of this presentation will explore the impacts of making this assumption during mismatch Monte Carlo analysis in terms of simulation time, compute resources and accuracy of results.



A Simplifying Assumption What is the small-variation assumption?

The small-variation assumption is that mismatch variations in YOUR manufacturing process are sufficiently small that there is a LINEAR relationship between all the varying device parameters and the figures-of-merit which they impact.

- There are many benefits which are gained by making this assumption.
- This assumption tends to be valid for mismatch variations.





A Simplifying Assumption How does the small-variation assumption help me?

There are two primary benefits that are realized through the application of the small-variation assumption:

- All mismatch Monte Carlo results can be derived by linear manipulations of a SINGLE nominal simulation.
 - You can think of it as a one-run Monte Carlo!
- The linear assumption allows the principle of superposition to be applied.
 - This allows the impact of EACH DEVICE's variations to be characterized independently!
 - A Mismatch Contribution Table can be produced!

The small-variation assumption can greatly speed simulation and/or provide new insight into circuit mismatch effects!



Introducing Fast Yield Contributor Analysis (FYC) Implementing the Small-Variation Assumption

- New Fast Yield Contributor (FYC) technology implements the small-variation assumption
- FYC permits fast mismatch analysis
 - Up to 100X speed improvement in harmonic-balance simulations
 - Little to no loss in accuracy
- Mismatch Contribution Tables (MCTs) can optionally be produced
 - Provide detailed breakout of the impact of the mismatch of each device in the design





Introducing Fast Yield Contributor Analysis (FYC) Availability of Fast Yield Contributor Analysis

New Fast Yield Contributor technology is currently available for the following simulators:

- Currently FYC is supported in the Monte Carlo task in DC, AC and harmonic balance
 - Both driven and autonomous (oscillator) circuits are supported in harmonic balance
 - Noise is not currently supported

✓ (////////////////////////////////////	Choosing Analyses Form - GoldenGate0
Analysis	Run List (CR)
L AC A SP	You are setting up analysis CR Enabled 🗹
H AC H SP H TR H CR H CR H CR H CR H CP H CR H CR	You are setting up analysis CR Enabled Enable Task Monte Carlo Options Yield Goals Parallelism Type Regular LHS HSS Boundary Rerun No. of Trials 1000 Start From Number Options Statistical Variation Seed random specified 30105 Max Wall Time (hr) Statistical Variation Type Process Mismatch Enabled for All Devices List Both
	Compute Correlations 🔲 Variable Correlation 🗌
	Save Trial Data 🔾 none 💿 failures 🔾 all To File mctrials.txt
	FYC 🗹 Compute Yield Contrib. Table 🗹 Threshold (%) 5
	OK Cancel Defaults Apply Help



Introducing Fast Yield Contributor Analysis (FYC) Using FYC Analysis

	Choosing Analyses Form - GoldenGate0	/////×
Analysis	Run List (CR)	
	You are setting up analysis CR	Enabled 🗹
	Enable Task Monte Carlo	
	Type Regular ULHS HSS Boundary Rerun No. of Trials 1000 Start From Number 1	
	Options	
	Statistical Variation Seed random specified 30105 Max Wall Time (hr) Statistical Variation Type Process Mismatch Enabled for All Devices List Both Compute Correlations Variable Correlation Save Trial Data none failures all To File mctrials.txt FYC Compute Yield Contrib. Table Threshold (%) 5	
	OK Cancel Defaults Ap	ply Help

FYC setup is nearly identical to setup of normal Monte Carlo Analysis

- Simply enable FYC from within the Monte Carlo Task
- Select whether or not the Mismatch Contribution Table is desired.
- FYC results are a SUPERSET of MC results
- All signals are available for all trials.
- Statistical information for performances are included
- Mismatch Contribution Table (MCT) is available if requested.



Introducing Fast Yield Contributor Analysis (FYC) MCT Results Tree



Mismatch Contribution Table results are selected from a results tree

- This tree contains every performance equation created for the simulation
- All levels of design hierarchy are provided underneath each performance
- Histograms and contribution information is available at ALL levels of hierarchy.



Agenda

Overview of RFIC Verification

The Problem of Mismatch

Simulating Mismatch – The Good, The Bad and The Ugly

A Simplifying Assumption

Introducing Fast Yield Contributor Analysis (FYC)

FYC Circuit Simulation Examples

- LNA Supply Current Analysis (DC)
- VCO CR Analysis (CR)
- Receiver Gain Analysis (CR)

Review and Additional Resources



LNA Example



- Description: LNA
- Process: 0.18 um CMOS
- Frequency: 2.4 GHz
- Active Device Count: 30
- Interesting Figures-of-Merit:
 - DC Current



LNA Example DC FYC Comparison

Normal Mismatch Monte Carlo

- Simulation Time: 4.14 sec
- Memory Consumption: 189 MB
- DC Current Statistical Results:
- Mean: 15.65 mA
- Std Dev: 0.4706 mA
- Minimum: 14.27 mA
- Maximum: 17.03 mA

FYC Mismatch Monte Carlo

- Simulation Time: 2.22 sec (1.9X) with MCT: 2.22 sec (1.9X)
- Memory Consumption: 189 MB

DC Current Statistical Results

- Mean: 15.64 mA
- Std Dev: 0.4708 mA
- Minimum: 14.24 mA
- Maximum: 17.00 mA



LNA Example DC Accuracy – Mismatch MC versus Mismatch FYC







LNA Example Mismatch Contribution Table (MCT) Results







LNA Example Mismatch Contribution Table (MCT) - Continued





LNA Example Mismatch Contribution Table (MCT) - Continued





VCO-Divider Example



- Description: VCO-Divide-by-2
- Process: 0.18 um CMOS
- Frequency: 5.4 GHz
- Active Device Count: 60
- Interesting Figure-of-Merit:
 - Oscillation Frequency



VCO-Divider Example CR FYC Comparison

Normal Mismatch Monte Carlo

- Simulation Time: 109 sec
- Memory Consumption: 188 MB

Oscillation Freq. Statistical Results:

- Mean: 5.40991 GHz
- Std Dev: 0.00019 GHz
- Minimum: 5.40936 GHz
- Maximum: 5.41043 GHz

FYC Mismatch Monte Carlo

- Simulation Time: 12.66 sec (8.6X) with MCT: 14 sec (7.8X)
- Memory Consumption: 188 MB

Oscillation Freq. Statistical Results:

- Mean: 5.40993 GHz
- Std Dev: 0.00019 GHz
- Minimum: 5.40937 GHz
- Maximum: 5.41048 GHz



VCO-Divider Example CR Accuracy – Mismatch MC versus Mismatch FYC







VCO-Divider Example Mismatch Contribution Table (MCT) Results





Receiver Example



- Description: Receiver
- Process: 0.18 um CMOS
- Frequency: 2.4 GHz
- Active Device Count: 946
- Interesting Figures-of-Merit:
 - Power Gain



Receiver Example CR FYC Comparison

Normal Mismatch Monte Carlo

- Simulation Time: 14,199 sec
- Memory Consumption: 443 MB
- Mean: 40.37 dB
- Std Dev: 0.04 dB
- Minimum: 40.28 dB
- Maximum: 40.50 dB

FYC Mismatch Monte Carlo

- Simulation Time: 421 sec (34X) with MCT: 568 sec (25X)
- Memory Consumption: 778 MB
- Mean: 40.38 dB
- Std Dev: 0.04 dB
- Minimum: 40.27 dB
- Maximum: 40.50 dB



Receiver Example CR Accuracy – Mismatch MC versus Mismatch FYC







Receiver Example Mismatch Contribution Table (MCT)





Receiver Example Mismatch Contribution Table (MCT) - Continued





Review and Additional Resources

Fast Yield Contributor analysis provides designers with muchneeded enhancements to enable extensive mismatch analysis of mixed-signal and RFIC designs.

- Based on a new small-variation assumption
- Provides significant speed improvement over traditional Monte Carlo
- Accuracy for mismatch analysis is very good
- Provides important details about contributions from mismatch within the circuit

For more information on Fast Yield Contributor analysis, please contact your EEsof Application Engineer.



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