Solutions for Undetected Shorts on IEEE 1149.1 Self-Monitoring Pins

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SOLUTIONS FOR UNDETECTED SHORTS ON IEEE 1149.1 SELF-MONITORING PINS

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Abstract *– This paper presents the problem of undetected shorts on IEEE 1149.1 compliant self-monitoring pins. Unidirectional and bidirectional self-monitoring pins may contain sufficient series termination resistance and low enough voltage swings such that shorts between two pins become resistively isolated from the receivers and therefore are undetected during wiring interconnect tests. Potential solutions to mitigate the problem are offered.*

Keywords: 1149.1, Wire Interconnect, JTAG, shorts, hysteresis, Board Test, Boundary Scan

I. INTRODUCTION

A self-monitoring pin is a type of boundary-scan driver pin which can capture the logic level that the output drive buffer is driving. Figure 11-32, 11-33, 11-37, 11-40 and Figure 11-41 of the IEEE 1149.1-2001 standard illustrate conceptual compliant designs supporting self-monitoring pins[1].

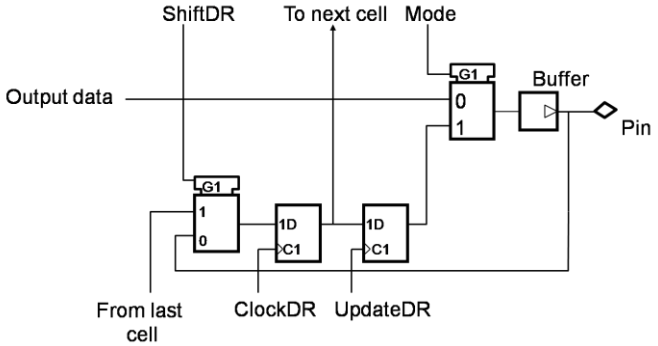

Figure 1. BC_10 type self-monitoring pin

A unidirectional two state output with self monitoring capability is shown in Figure 1. The logic value at the pin is captured prior to the SHIFTDR state and shifted out on TDO for analysis.

Pins with self-monitoring capability are preferred for board test as they improve fault diagnostics for 1149.1 driver to receiver interconnect tests. Figure 2 illustrates the self-monitoring pin A captures back a logic '1' when the net is open and pin B captures back a logic '0' when the net is shorted to ground. Without this self-monitoring capability, 1149.1 based tools will only see the constant logic '0' captured by the receivers on each net. Some 1149.1 software tools take advantage of the incorrect value seen by the driver to correctly diagnose the difference between a stuck-at fault on the net and an open on a net. This is an important distinction necessary to properly select between inexpensive or costly repair operations.

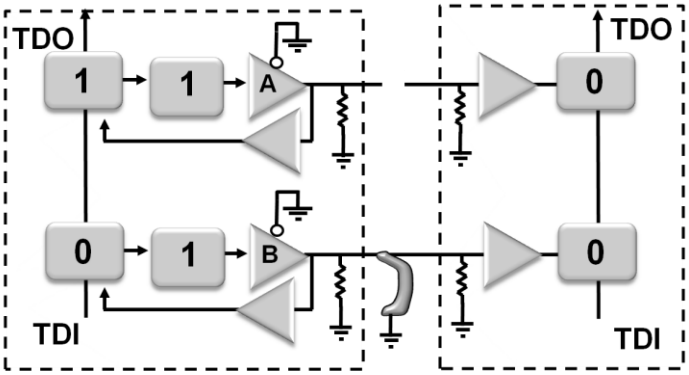

Figure 2. Difference of short-to-gnd and open

These types of self-monitoring pins are also capable of detecting shorts between nets that connect a Boundary-Scan device and a powered non-Boundary-Scan device or passive component such as a connector. Figure 3 shows a portion of a compliant IEEE 1149.1 device with three self-monitoring unidirectional outputs labeled A, B and C. Board level ATPG (Automatic Test Pattern Generation) tools would read the netlist and BSDL (Boundary-Scan Description Language) files for the ICs present to generate the test patterns. The board nets for A, B, and C would be each assigned a unique signature. During interconnect testing the ICs are loaded with the EXTEST instruction. When the test patterns are applied, the first bit of each net's unique signature is shifted in to the capture/shift flip-flop. In this case 1-0-1 is shifted in representing the LSB of the unique signatures for A, B and C. On the falling edge of TCK, while leaving the UPDATE-DR state, the values are moved to the update register and the logic value is driven by the output buffer. When the next bit of the unique signature, a 0-1-1 is to be shifted in, the tap controller must go through the CAPTURE-DR state.

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The capture/shift flip-flop will capture the logic value at the pin of each output A, B and C during the CAPTURE-DR state and and place the captured values on to TDO during the SHIFT-DR state. When there is no fault present, the logic value captured should be the logic value driven. In the case of Figure 3, where there is a short across the pins of B and C, the data captured back at C is a logic '0', when it should be a logic '1'. The figure represents that point in time, when the update flip flops are driving the 1-0-1 and the three capture flip-flops have captured a 1-0-0.

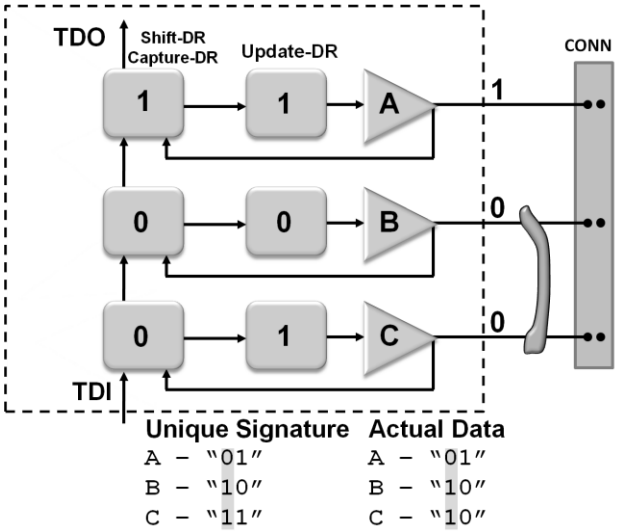


Figure 3. Self monitoring pins with short at connector

The test software will analyze the actual data returned and determine that B and C are shorted together as both received the same '10' signature value.

II. THE PROBLEM

The authors reported the problem of shorted unidirectional and bidirectional pins passing interconnect tests during an IEEE 1149.1 Working Group meeting. In one case, a WG member indicated that 1.8V and 1.5V self-monitoring unidirectional drivers on a device were passing 1149.1 based shorts tests. Tuthill observed bidirectional 2.5V CMOS drivers on a popular FPGA IC with passing shorts tests. Notes and potential solutions were shared between the authors which became the basis of this paper.

In both of the reported cases, the self-monitoring pins were able to detect shorts to ground and shorts to power. When the driver is driving a logic '1' and the pin is shorted to ground, the input captures a logic '0' and the fault is detected. When the driver is driving a logic '0' and the pin shorted to VCC (2.5V in the FPGA example) the input captures a logic '1' and the fault is detected.

An approximation of the design of two self-monitoring bidirectional pins is shown in Figure 4. Each pin includes a 33 ohm series termination resistor and non-zero internal buffer resistance. The output driver has an internal impedance which when combined with the series termination resistor provides roughly 50 ohm matching impedance to the printed circuit board. Figure 4 shows how the two pins when shorted together are 'resistively isolated' at the actual receiver inputs. The top output pin is driving 2.5V and the bottom driver is driving 0V. The voltage at the shorted pins is approximately 1V. Circuitry not shown turns on the p-channel FET in the upper pin 'on' and the n-channel FET in the lower pin 'on'. The bulk of the current flow is shown with the arrows. The voltage at the receiver inputs is shown. With the I/O reference voltage set to 2.5V, V_{IH} is 1.7V and the input on the top I/O sees a logic '1' due to the 2V present. V_{IL} is 0.7V in 2.5V CMOS. A logic '0' is seen by the bottom input due to the 0.5V present.

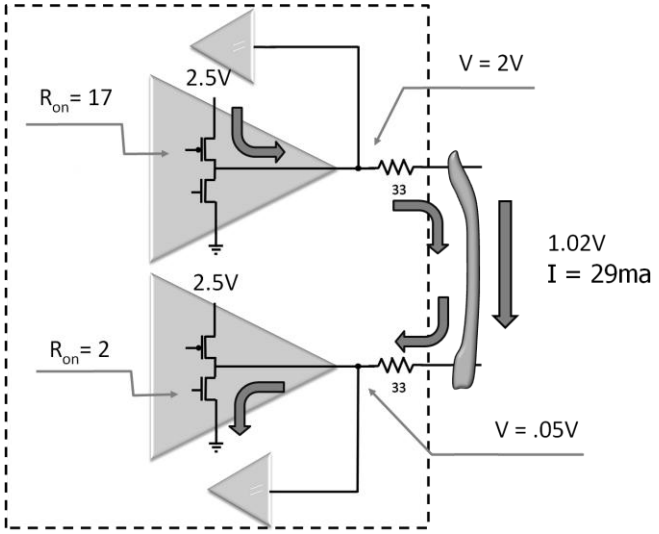


Figure 4. Two Self-Monitoring Drivers Shorted

Currently boundary scan cell designs BC_7, BC_8, BC_9 and BC_10 in the 1149.1-2001 standard are used to describe and implement the self-monitoring capability. The current standard doesn't support describing this 'partial test' behavior, with the ability to detect a short to a rail, ground or VCC, but not to detect a short to another pin of the same type. The problem leads ATPG tools to falsely identify shorts coverage which does not exist when self-monitoring cells are used in the BSDL file. PCB designers who rely on 1149.1 Design-for-Test tools make decisions during board layout based on the results of BSDL and netlist tool analysis. Incorrect reporting can lead to

downstream increased costs in test and test escapes. The problem is compounded when I/O levels may be set by an external voltage reference. In some cases the I/O will correctly be described via the BSDL file when set to 3.3V but will fail to detect shorts when set to 2.5V or 1.8V. The 1149.1-2001 standard does not currently support BSDL descriptions with parameters such as voltage levels.

III. SOLUTIONS

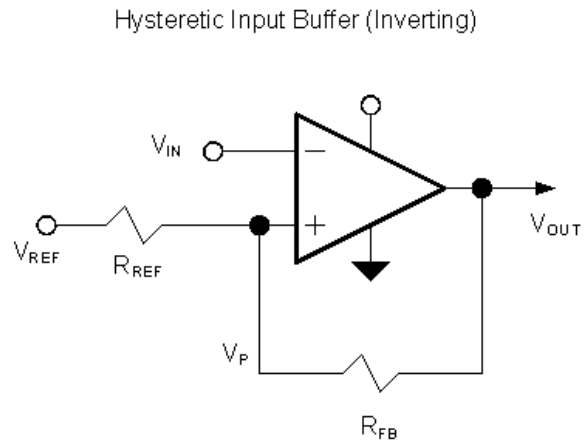
One solution could be to change the drive strength during EXEST such that more current can be sourced and a higher IR drop may be obtained. This may not be practical due to the size and complexity. It may also not be possible for designers using standard cell libraries who do not have this type of control over their I/O buffers.

A second solution could be to change the threshold on the input so that the shorted pin voltage is not in between logic '1' and '0'. This choice of threshold could be enabled by Boundary-Scan EXTEST mode and not used in normal mission mode. This also may be difficult for designers using standard cell libraries. It may not solve the problem as the voltage appearing to the input buffer may not be the same voltage as the shorted pin voltage as is the case in Figure 4

Two of the more promising solutions are provided in section IV and V.

IV. SOLUTION: HYSTERETIC INPUT

A third solution is to implement a hysteresis band at the receiver. This hysteresis could be enabled by Boundary-Scan EXTEST test mode and disabled when in normal system mode. This could be designed such that the midpoint voltage is within the hysteresis band and it takes a voltage closer to logic '1' or '0' to cause the receiver to perceive the opposite state from the previously perceived state. Figure 5 shows an example hysteretic input buffer. The V_{REF} is an input threshold voltage between a logic '0' and a logic '1'.



$$V_P = V_{REF} + (R_{REF}/(R_{REF} + R_{FB})) * (V_{OUT} - V_{REF})$$

Figure 5. Hysteretic Input buffer

For test purposes, this value may be 1.25V in our 2.5V example even though in mission mode the 2.5V CMOS standard defines logic high values as 1.7V and higher and logic low values as .7V and lower. The feedback loop R_{FB}/R_{REF} changes the effective reference voltage to Vp. The ratio of resistances and the gain of the buffer determine how much Vp changes when Vout toggles between the rails. There is no loading by this feedback path on V_{IN} itself. The example here assumes a R_{FB}/R_{REF} ratio of 2:1, a swing of 2.5v and a gain of 25.

The circuit was simulated and the output shown in Figure 6. When Vin is a logic '0', the threshold (Vp) is 1.75 volts, but when Vin moves above 1.7 volts, the threshold moves down to 0.7 volts. The threshold reverts to 1.75 when Vin again passes below 0.7 volts. This gives us a 1 volt hysteresis on the input. If two self-monitoring drivers produce a voltage anywhere between 0.7 and 1.75 when shorted, then this input buffer will produce a logic '0' or '1' depending on the last valid logic value it saw. Since a proper Boundary-Scan test will set both fighting drivers to 00, 01, 10, 11 at various points in the test, the two self monitors on the fighting drivers will "remember" the last value produced when the drivers were not fighting. Thus, one monitor will fail in each case. The ratio of resistors, gain, and value of V_{REF} can be engineered to appropriate values for self-monitoring pins.

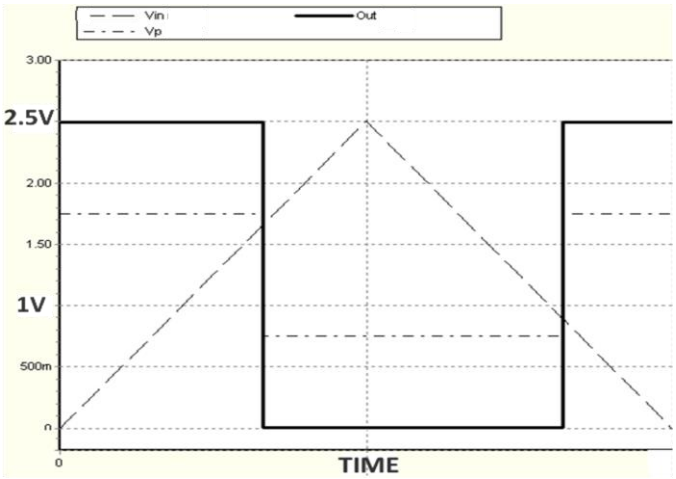


Figure 6. Plot of Hysteretic input voltages

The designer will want to know what "Vshort" is at the I/O pins, and take into account the IR drop back to the points where the self monitors are connected. The hysteresis cushion should be greater than twice this IR drop with V_{REF} set to Vshort. The output of the buffer would then be inverted before being fed to the input boundary-scan cell.

This solution works well but has a similar limitation as the prior two solutions and that is its availability to the designer using standard cell libraries. There may be an input buffer with hysteresis in the standard cell library but it may not be possible to set the hysteresis for the mission mode operation separate from the EXTEST operation. Setting the resistors for mission mode standards such as LVCMOS2.5 or LVCMOS1.8 may not be suitable for "Vshort". Traditional boundary-scan insertion tools such as Synopsys BSD Compiler may not know how to insert and connect the hysteretic input buffer. The other disadvantage is that detection requires the input to cross the threshold voltage to register the change. This may require a little different thinking during debug for test engineers familiar with working with the traditional static logic level observation of 1149.1.

V. SOLUTION: OUTPUTS-OFF MARCHING 0/1 TEST

Before describing the solution, the following background material will help in its understanding. The figures for the self-monitoring unidirectional outputs in the 1149.1-2001 standard lack important detail. Figure 1 shows essentially a wire connected at the pin brought back to the capture/shift flip-flop through a multiplexer. In a real IC design however, this is not possible. The only way to observe the logic value on a unidirectional output is through the use of a bidirectional buffer or asymmetrical I/O buffer. A standard cell I/O buffer is shown in Figure 7A. Typically a unidirectional self-monitoring pin using standard cell libraries would use a bidirectional buffer with the enable tied-off as in Figure 7B.

Asymmetrical outputs with self-monitoring capability are implemented in one of two ways in standard cell design. An open drain output can be created with the bidirectional I/O in (A) by connecting the output buffer to ground and bringing the data output to the enable as shown in (C).

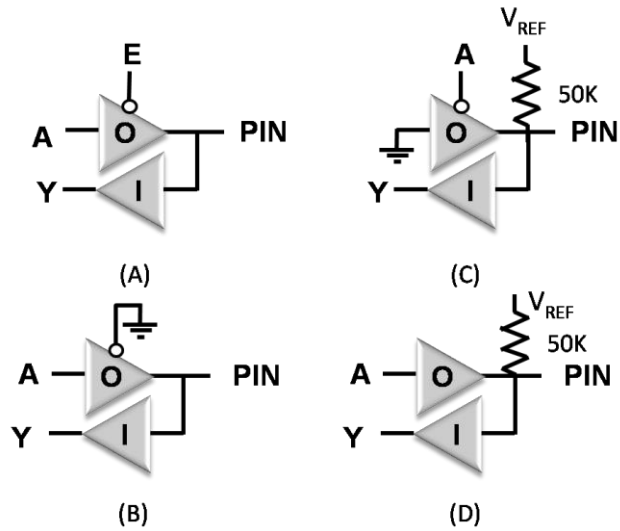


Figure 7. Standard cell I/O needed for self-monitoring capability

An open drain bidirectional I/O buffer may also be present in the library as shown in (D). This buffer could be used directly for an asymmetrical output with self monitoring capability. The point is that an output buffer by itself is never suitable for a self-monitoring pin as there is no way to observe the logic value at the pin.

A more accurate schematic for Figure 1 would include a tied-off bidirectional used as a unidirectional. Figure 8 shows the two state unidirectional output expanded to include a control cell to put the output in high impedance for test purposes. Nothing in the mission mode design changes in terms of performance, just the output can be put in a high impedance state during 1149.1 test. When the symmetrical output2 drivers can be made 3-state then the problem of the undetected shorts may be resolved through a unique pattern set targeted for bidirectionals and these 3-state drivers. If the output is an asymmetrical driver, such as an open drain output then this will also meet our needs for the pattern set however, we do not have evidence that a self-monitoring asymmetrical driver would ever have the potential of

having passing shorts since only one state is driven and the other state is essentially off.

In the first section of the paper we describe traditional shorts testing using unique net IDs as first described by Kautz, Goel and McMahon.[2,3] The patterns illustrated show fault detection using a small ID, however in practice true/complement type signatures are used to avoid aliasing as first described by Wagner[4].

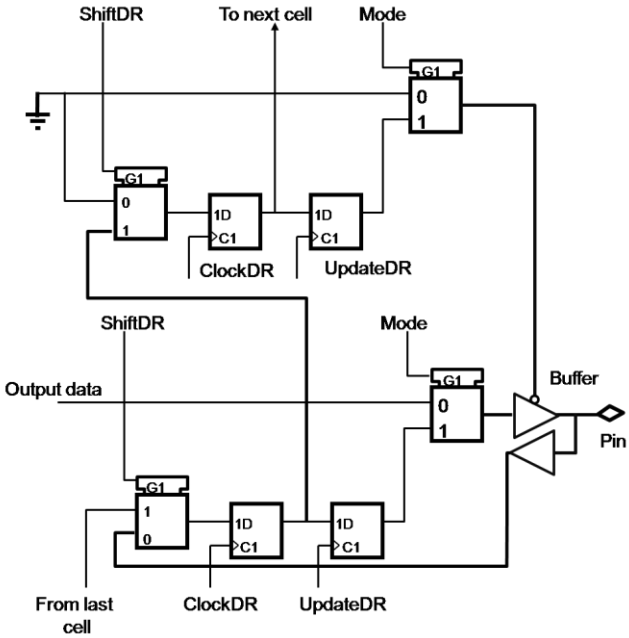


Figure 8. Self monitoring output with detail

Jarwala and Yau describe walking 1s and 0s pattern sets. However, in their descriptions the walking 1s/0s patterns are performed with at least one driver per net driving. They describe testing of 3-state I/O but only in the context of multi-driver tests for nets with multiple boundary scan drivers.[5]

None of the algorithmic approaches known detected the shorts. Clark-Tuthill developed the first outputs-off walking 1s/0s tests as a solution to the passing shorts on self-monitoring pins problem.. Figure 9 shows three self-monitoring outputs, A, B and C with the detail showing the proper I/O buffer needed for self-monitoring and a control cell for putting the output in high impedance. Critical to the solution is a weak bias to VCC or GND on each I/O, this capability is available in a standard I/O library. When the net is un-driven the received value must be constant '1' or a constant '0'.

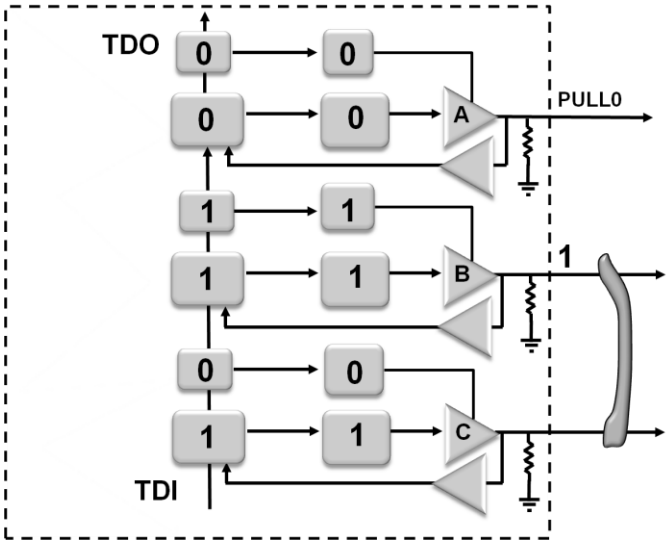


Figure 9. Output off walking ones test for shorts

The resistor shown is conceptual; any design which guarantees that the input is not floating will suffice. The FPGA device used in the measurements meets this criterion. A portion of the BSDL file of the FPGA shows the PULL0 construct and two cell bidirectional design.

```
"1459 (BC_2, *, controlr, 1)," &
"1460 (BC_2, IO_K34, output3, X, 1459, 1, PULL0)," &
"1461 (BC_2, IO_K34, input, X)," &
"1462 (BC_2, *, controlr, 1)," &
"1463 (BC_2, IO_L34, output3, X, 1462, 1, PULL0)," &
"1464 (BC_2, IO_L34, input, X)," &
```

In order to detect the shorts, traditional IEEE 1149.1 based tests are supplemented with high impedance and open drain walking 1s/0s tests for all PCB areas which are questionable that shorts will be detected during traditional Wagner type patterns. FPGA I/O set at 2.5V or lower is one of the areas of concern.

To test the nets, A, B and C are all put into input mode and '1' is driven on each output, one pin at a time.

Figure 9 is shown at the point in time where B is selected for driving a logic '1', the logic '1' is driven during UPDATE-DR and the tap controller has transitioned to the SHIFT-DR state where the boundary-scan cells have captured the logic value at the pin. With B and C shorted, C captures a logic '1' when it should be capturing a logic '0', allowing the short to be detected.

One advantage of this approach is that it is compatible with standard I/O libraries available to the designer. The second advantage is that the architecture may be automated as it works with traditional Boundary-Scan insertion tools. It works regardless of the I/O voltage and no special prediction of shorted pin voltages or on-

chip reference voltages needs to be determined at design time. It also may be more suitable for pins which have programmable I/O characteristics such as output impedance since the threshold voltage needed for the hysteretic input may change. This method works well for IC designers using standard cell libraries where the only way to create a self-monitoring output is with a bidirectional type buffer and pad. Since the bidir buffer is required for basic self-monitoring capability, there is no performance penalty over an output2 with self-monitoring capability. This may not be the case in full-custom designs as other options may be available to the designer who has full control over the design of the I/O buffer and has the resources to full characterize it for a particular technology node. In those cases, the hysteretic input may be the better solution.

One disadvantage is that the Clark-Tuthill approach requires more control cells. Shorts are not detected on three-state self-monitoring driver pins that are connected to a common control cell since they must all be high-impedance or driving. Another disadvantage is the size of the test patterns required compared to using the hysteretic input buffer with Wagner style true/complement type patterns. Wagner style vectors require just 2 * $Log_2(N+2)$ scan vectors to detect and diagnose faults where N is the number of nets to be tested. The outputs-off walking 1s/0s test requires 2*N+1 scan vectors if both PULL1 and PULL0 type pins are present in the design.

VI. DISCUSSION

The same principles for the hysteretic input and outputs-off marching 1s/0s can be applied to differential pins. Further work to refine the approaches for differentials needs to be done.

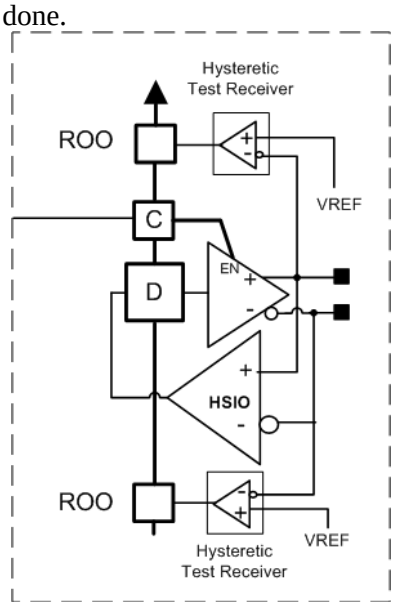


Figure 10. Bidir differential with hysteresis

The reader may be familiar already with the hysteretic inputs in the test receiver on each pin of IEEE 1149.6. Similar constructs could be used for a DC coupled 1149.1 based differential.

In Figure 10, hysteretic receivers on each differential leg, similar to 1149.6 are shown. These provide input into what 1149.1 specifies as a "redundant observe only cell" or ROO. This cell can be used by ATPG to observe each pin individually. Shorts can be detected between the pins and to adjacent differentials with similar voltage swings. The area and additional design considerations should be noted.

The Clark-Tuthill approach can also be applied to differentials. Figure 11 shows a bidirectional differential. The positive and negative pins are weakly biased when the device is in EXTEST in order to provide a valid input into the receiver and hence into the capture point of the 'D' boundary-scan cell.

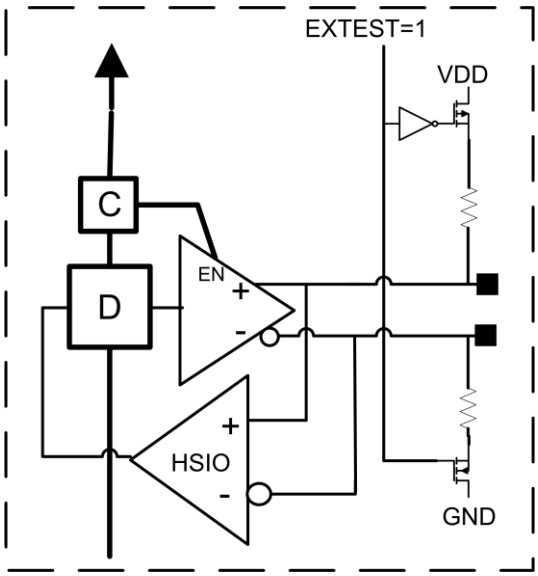


Figure 11. EXTEST biased input differential

LVDS receivers specify mission mode active or passive biasing so the receiver has a predictable value when the differential is not driven. This also may be leveraged for use during outputs-off marching 1s/0s.

This circuit assumes that the mission mode HSIO receiver is not turned off when the output driver is on via the control-cell. The receiver off function is typical when the designer wants to reduce power or simplify the signal integrity issues when the circuit is in output mode. In some cases, it may be necessary to include a smaller, simple DFT type comparator which takes the place of the HSIO comparator during EXTEST. Further work will need to be done to refine this circuit. If there are no redundant observe only cells on each leg (as shown) one boundary-scan cell cannot

resolve all the possible faults of two pins. During outputs-off marching 1s testing, a short is not detected as the constant logic '1' value received in the un-driven state masks the short from an adjacent positive leg which is driving. A short between the positive leg and another similar technology positive leg is detected when the marching logic '0' pattern is driven however.

A short between the two pins in Figure 11 is not detected. One way to detect the short between the two pins is with a window comparator on the differential receiver as shown in Figure 12. It's made up of two simple DFT comparators which look for a differential value greater than 65mv. The transmit side was not shown to simplify the understanding.

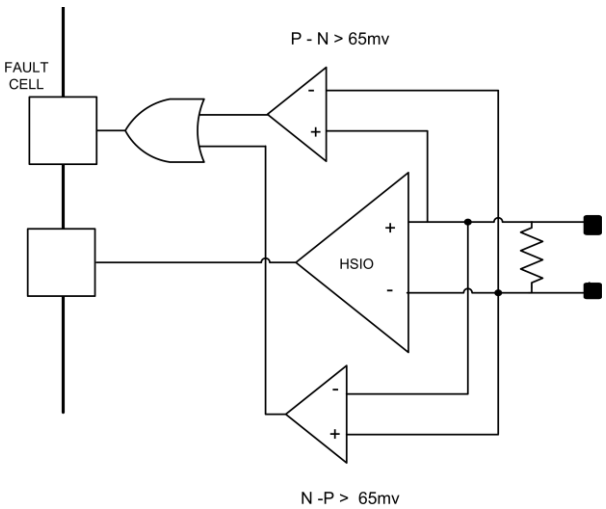


Figure 12. Window Comparator on input

A similar window comparator technique is used for detecting mission mode LVDS receiver problems. The comparators are used as an alternative to biasing the positive and negative legs which can distort the eye diagram and affect jitter. When small value voltages appear across the input to the comparators a logic '1' is received in the boundary-scan cell labeled "Fault Cell". While in concept this may work, the current IEEE 1149.1 standard does not support the logic gate or the 'fault cell' concept.

The Wagner algorithm is used commonly for boundary-scan test.[4] The patterns are small however there is a penalty for testing via 'driver fights'. Figure 13 shows the experimental results of a comparison of detected resistances using the Wagner approach and the Clark-Tuthill approach. A commodity device was used for the test and a variable resistance was placed across 3.3V LVCMOS based pins. The resistance was measured for several steps and the detection of a short was noted.

Wagner pin to pin Short VIO 3.3V			
Resistance of Short (Ohms)	Voltage @ Driver Lead (V)	Voltage @ Receiver Lead (V)	Short Detected
22	2.2	1.2	No
15.1	2.16	1.443	No
13.7	2.157	1.488	No
13.4	2.156	1.497	Yes
11	2.14	1.6	Yes

Clark-Tuthill pin to pin Short VIO 3.3V			
Resistance of Short (Ohms)	Voltage @ Driver Lead (V)	Voltage @ Receiver Lead (V)	Short Detected
88.6K	3.29	1.36	No
85K	3.29	1.46	Yes
81K	3.29	1.55	Yes
75K	3.29	1.67	Yes
67.8K	3.29	1.83	Yes
49.9K	3.29	2.28	Yes
25.2K	3.29	2.74	Yes

Figure 13 Interconnect Test Comparison

At 3.3V the largest resistive short detected was 13.4 ohms using the Wagner approach. In the Clark-Tuthill approach the largest resistive short detected was 85K ohms. These values will vary depending on the construction of the output driver itself. At lower voltages, 2.5V, only smaller resistive values than in the 3.3V table would be detected. This however can vary depending on the device I/O construction. The shrinking resistance values has implications on the ability of a Wagner algorithm only approach to detect resistive shorts during 1149.1 board test. While the Clark-Tuthill approach can detect large resistive shorts, it also has implications that an ATPG tool would need to consider all resistive paths in order to generate error-free patterns.

VII. CONCLUSIONS

This paper presents the problem of undetected shorts during IEEE 1149.1 based testing of self-monitoring pins. As the industry moves to I/O levels of 2.5V and lower, the voltage drop due to internal driver resistance becomes a larger percentage of the full swing voltage. This can lead to shorts being undetected on bidirectionals and self-monitoring I/O as the receivers are resistively isolated from the fault. Two major methods and two minor suggestions are offered to solve the problem; each has its own advantage and disadvantages. One thing is clear; IC vendors must fully

characterize their pins with 1149.1 testing in mind over the full voltage range, including shorting output pins. This must be done in order to create an accurate BSDL file and avoid describing self-monitoring pins which do not function correctly.

BSDL needs better constructs so self-monitoring pins which will not detect shorts can be identified. BSDL also needs better constructs to allow general purpose "outputs-off" walking 1s/0s type tests. In order to increase testability, it is recommended that symmetrical unidirectional drivers support a high impedance function with independent control-cell and a biased input. This can be done without affecting performance as the bidirectional buffer's enable just needs a control cell so it can be disabled during EXTEST testing. Symmetrical self-monitoring output2 pins should be avoided unless they are fully characterized over the entire mission mode voltage for all possible shorts, including detecting pin to pin shorts.

VIII. ACKNOWLEDGEMENTS

The authors would like to thank Brian Turmelle for his contribution in devising and conducting the shorted pin experiments.

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