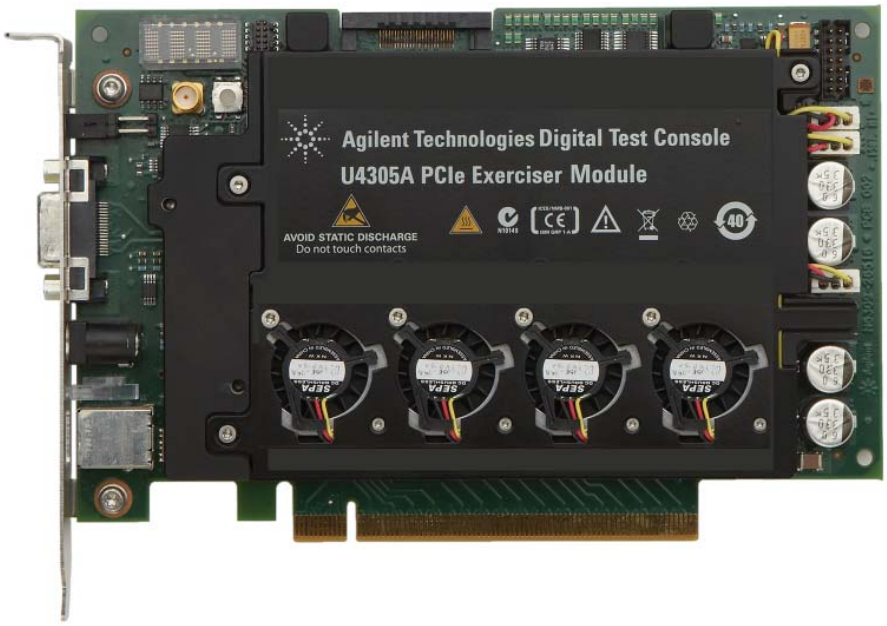
U4305A Protocol Exerciser for PCI Express® 3.0

Data Sheet



A Multi-Personality Instrument for PCIe, Multi-Root, and Single-Root I/O Virtualization

- Supports Gen1 (2.5 GT/s), Gen2 (5.0 GT/s), and Gen3 (8.0 GT/s) speeds
- X1, X4, X8, or X16 link widths
- Standard height, half-length card
- Perform through link PCIe® Link testing
- Verify Link Training and Status State Machine (LTSSM) state transitions and timeout implementations
- Emulate PCIe root complex or endpoint
- Emulation of non IOV PCIe, MR-IOV, or SR-IOV capable components
- Fully supported API to write custom test cases

Agilent Technologies

Overview

The Agilent U4305A Exerciser can be configured to provide sub-protocol layer test and debug for legacy and next generation PCIe devices. The U4305A Exerciser for PCIe is an advanced traffic generator that can be used to send and respond to TLP, DLLP, and physical layer packets to stimulate PCIe devices and systems. The Exerciser operates in one of three modes, PCIe, MR-IOV, or SR-IOV. The capabilities of these modes can be enhanced with the purchase of additional software licenses. Specific DUT test case requirements can be written by means of the included API. U4305A is a standard height, half-length PC form factor card as described in the PCI Express specification, and fits into every system including blade servers.

The PCI Express test and debug capabilities of the U4305A is broken down into the sub-protocol layers of the specification as shown in Figure 1. By emulating a PCIe component (with or without MRIOV capabilities), the Agilent U4305A Exerciser acts as an ideal link partner by sending appropriate I/O traffic to stimulate the device under test. The device under test can be exercised under test under various conditions and scenarios without influencing the performance parameters of the device under test. The Agilent U4305A Exerciser can send a block of TLP requests of 32 or 64 bit Memory, I/O, Configuration, or Message types as stimulus to the device under test. It can also be used to send completion packets in response to DUT's requests.

The U4305A PCIe 3.0 Exerciser provides the following:

- Supports Gen1 (2.5 GT/s), Gen2 (5.0 GT/s), and Gen3 (8.0 GT/s) speeds
- Supports LTSSM functions for up to x16 link widths
- Supports simultaneous use of LTSSM and Protocol Exerciser functions, without requiring any configuration
- Provides SR-IOV capabilities at Gen2 speeds
- Provides emulation of non IOV PCIe components, MR-IOV capable component, or SR-IOV capable components
- Emulation of MR-IOV capable components with five virtual hierarchies (with a separate completion queue for each hierarchy)
- Protocol Exerciser GUI and APIs provide a graphical control of the U4305A Exerciser card

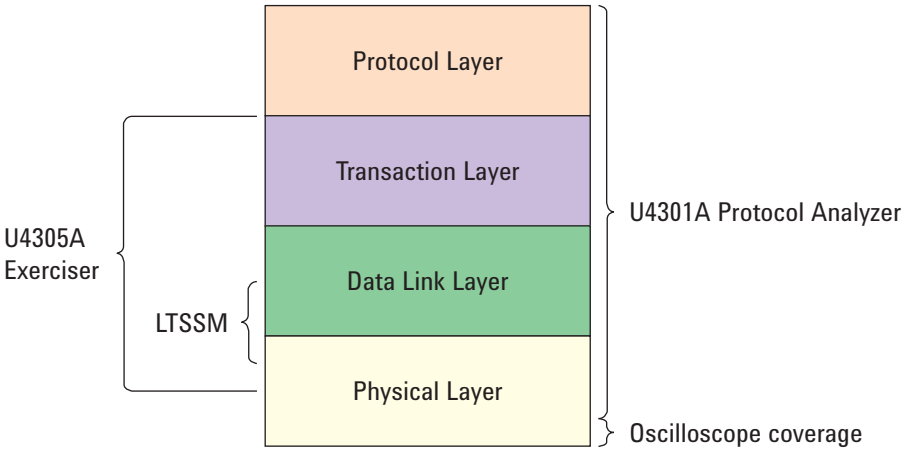


Figure 1. Application coverage of the Agilent U4305A PCIe 3.0 Exerciser module

Functions

As an endpoint

When emulating an endpoint, the Agilent U4305A Gen3 exerciser card is plugged into a PCIe slot on the motherboard, as a normal PCIe device. In this scenario, the exerciser card can be used to perform load and stress testing of the system under test.

As a root complex

When emulating a root complex, the Agilent U4305A Gen3 exerciser card communicates with the device under test through the Agilent N5316A backplane board. In this configuration, the exerciser communicates to the DUT through the bottom connectors. The DUT receives its power from the backplane.

Figure 2 shows example setups of a Protocol Exerciser card emulating an endpoint and a root complex.

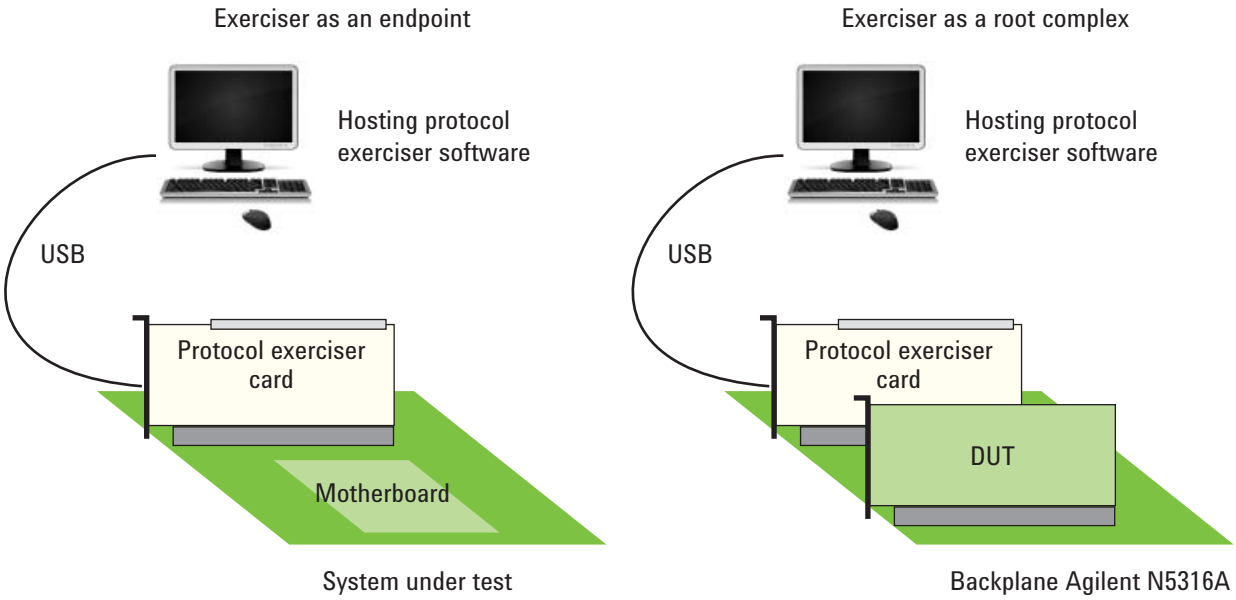


Figure 2. U4305A PCIe exerciser as endpoint and root complex applications

Functions (continued)

As an LTSSM tester

The Link Training and Status State Machine (LTSSM) is the sub-block that drives and controls the link initialization and training process for a PCIe device to enable the normal data exchange between PCIe nodes on the link. LTSSM operates at the physical layer and exchanges physical layer packets (Ordered sets such as TS1 and TS2) to initialize, train, and manage the link. LTSSM features are provided when option LT3 is purchased.

The Agilent U4305A Exerciser provides positive and negative test cases to exercise critical functions of either the end node (adapter card) or root complex (motherboard or blade). These test cases can force either DUT target devices into various LTSSM states, verify the state transitions, and timeout implementations, and report the test case results as either Passed or Failed.

LTSSM Physical Layer test features

- Supports 0.7 and 1.0 specifications through software selection
- Supports six way speed change from any of the three speeds to any of the three speeds
- When programmed as an Upstream Component (USC), supports going to Gen3 speed with all phases of equalization (0 through 3), only phase 1, or without equalization
- When programmed as a Downstream Component (DSC), it follows USC in equalization process
- Supports automatic or manual enabling/disabling of the lane reversal feature
- Supports independent lane polarity inversion setting for all the lanes
- Supports physical link widths X1, X4, X8, and X16. X2 is not supported. Link width is fixed and is specified when ordering.
- Supports option to enable/disable scramble modes for Gen1 and Gen2 speeds
- Supports all possible SKIP ordered sets (OS) at transmitter for all three speeds
- Can replace STP/END of a transmitted packet by programmable character at Gen1 and Gen2 speeds. Can corrupt FCRC of STP Token at Gen3 speed.
- Supports programmable Transceiver Settings covering a wide range of transmitted signal amplitude and emphasis levels
- Supports programmable Equalization settings sent in Transition Ordered Sets (TS OS) to request the DUT to transmit at various signal amplitude and emphasis levels

Data Link Layer test features

- Receive a packet as having an LCRC error and NAK in the packet to stimulate DUT response mechanism. Can repeat this for N (N is programmable) for a programmable sequence number causing DUT to replay multiple times and link retraining.
- Can offset Sequence number of transmitted packet for sequence number testing of the DUT
- Can send TLPs with LCRC and/or disparity errors
- Programmable replay timer value

Transaction Layer test features

- Can generate 32 bit or 64 bit memory transactions, Configuration Cycles, I/O Cycles, and message requests
- Generate correct or incorrect ECRC and check the same at the receiver
- Generate malformed TLP by making field inconsistent with actual payload length
- Generate poisoned TLP and nullified TLP
- Delay or discard erroneous completion notification to force completion notification
- Supports Data Compare to check integrity of the payload

Functions (continued)

Exerciser protocol checker

The U4305A PCIe Gen3 Exerciser provides an internal protocol check that reports various protocol errors that the DUT may have made and has been detected at the Exerciser's receiver. An external trigger can be generated on these events to enable trace tools to capture the details of the error condition.

Exerciser as a NON-IOV PCIe device

The Exerciser behaves as NON-IOV End Point (EP) or Root Complex (RC) when the protocol is set to PCIe. In this mode the U4305A Exerciser has three hardware channels and each channel is associated with a specific function (F0, F1, and F2). The traffic in each channel can be programmed independently either through the GUI or through the PCI port.

Two additional functions can be obtained with the purchase of the Option 024 software license.

Exerciser as a SR-IOV capable device

The exerciser behaves as a SR-IOV capable End Point (EP) or Root Complex (RC) when the protocol is set to SR-IOV. In this mode it is compliant with SR-IOV specification Rev. 1.1 (September 8, 2009).

In this configuration the exerciser supports the following:

- One Non-IOV function
- Two Physical Functions (PF)
- Two virtual channels (VC0 and VC(x))
- Two virtual functions (VF1 and VF2) per PF

PC Requirements

Two computers are required for the operation of the PCI express exerciser, a controller hosting the measurement application software, and a client hosting the device under test (SUT). The controller PC can connect up to a maximum of four Exerciser cards by means of USB ports.

Multiple clients can remotely connect to a single U4305A Exerciser session on the controller PC. Figure 3 shows an Exerciser session scenario in which Session A and Session B have been created on the controller PC with two U4305A Exerciser cards. Two clients are accessing Session A and one client is accessing Session B.

Controller and Client PC Requirements

- USB 2.0 interface for each Exerciser card
- Pentium processor 1 GHz or equivalent
- Windows® XP (with Service Pack 2) or Windows 7 (Enterprise or Professional 32-bit or 64-bit) operating system
- At least 256 MB RAM. For better performance, Agilent recommends the installation of at least 512 MB RAM.
- At least 500 MB free disk space on the C drive

Additionally, the client computer must have Microsoft .NET Framework 2.0 installed and it is provided on the installation CD.

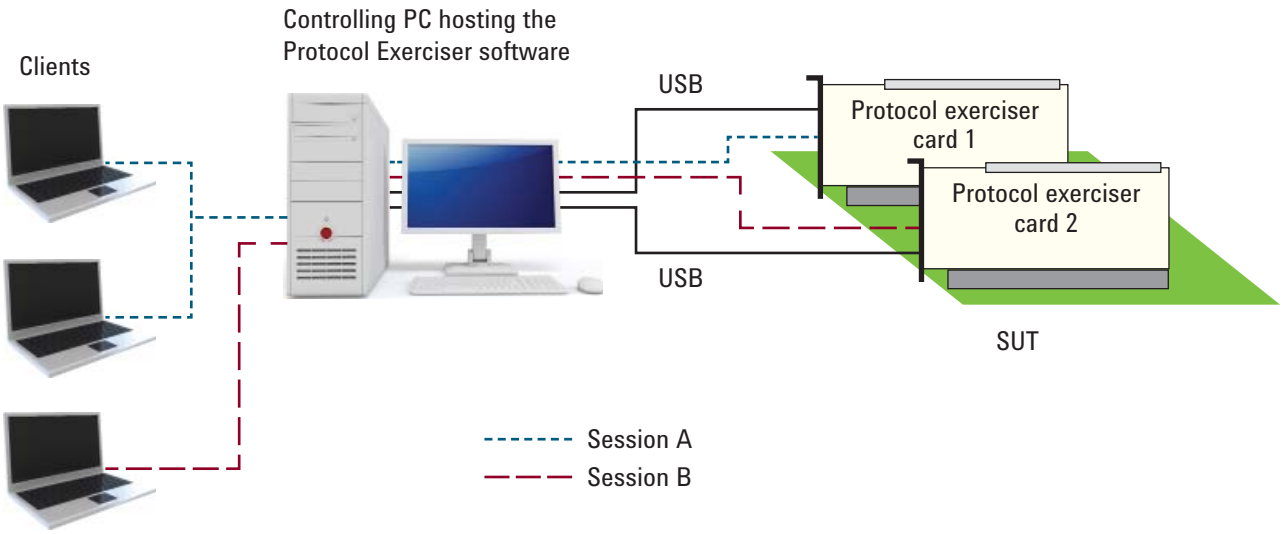


Figure 3.

Specifications and Characteristics

Physical characteristics

Size	Standard height half-length PCIe module 106.7 mm (4.2 inches) high and 167.65 mm (6.6 inches) long
Weight	408 gr (0.9 lb) Shipping weight: 2.36 Kg (5.2 lb)
Connectors	Power input, USB 2.0B, and two SMA(f) connectors for trigger in and out. Edge connector width is determined by the product configuration purchased. Note: The edge connector is not upgradable after purchase and Agilent does not recommend or support the use of lane adaptors as they have a negative impact on the unit's performance at high speeds.

Power requirements

Input	15 Vdc, 10 A maximum
Power dissipation	70 W maximum
Agilent part number 0950-4866 external power supply supplied with the Exerciser	
Input	100 to 240 V at 3.5 A maximum, 50 to 60 Hz

LTSSM supported states

The Agilent U4305A supports seven of the 11 LTSSM states. The supported states are:

- Detect
- Quiet
- Configuration
- L0
- Recovery
- L0s
- L1

U4305A trigger specifications

Trigger output	
Source impedance	50 ohms
Amplitude	2.4 V open circuited, 1.2 V into 50 ohms
Pulse width	120 ns
Trigger input	
Maximum input	2.0 V
Input impedance	Approximately 4 k ohms

Environmental specifications

This instrument is intended for indoor use in an installation category II, pollution degree 2 environment.

Temperature	Operating: 0 to +45 °C Storage: –40 to +70 °C
Humidity	15% to 95% operating, non-condensing
Altitude	2000 m (6,500 feet) maximum
Safety	IEC 61010-1:2001 / EN 61010-1:2001 Canada: CSA C22.2 No. 61010-1:2004 USA: UL 61010-1: 2004

Ordering Information

The relationship of the various software licenses available for the Agilent U4305A PCIe 3.0 Exerciser is prsented in the table below. The structure of these options is such that the options for MR-IOV, SR-IOV and ECRC are enhancements to the Exerciser license Option EX3.

	Options					
Features	EX3	LT3	MR2	23	24	22
Exerciser (EX3)	X					
LTSSM (LT3)		X				
MR-IOV Gen 2 (MR2)	EX3 Required		X		Optional	
SR-IOV Gen 2 (023)	EX3 Required			X	Optional	
Five functions (024)	EX3 Required		Optional	Optional	X	
ECRC (022)	EX3 Required					X

U4305A Exerciser card for PCIe 3.0, PCIe 2.0, and PCIe 1.0

A specific configuration is required to determine the lane width to be tested. Lane width is not upgradable after purchase. Agilent does not recommend or support the use of lane width adaptors as they greatly reduce the ability to reliably test systems operating at Gen2 or greater speeds.

Model number	Description
Exerciser card	
U4305A-E01	Exerciser link width X1
U4305A-E04	Exerciser link width X4
U4305A-E08	Exerciser link width X8
U4305A-E16	Exerciser link width X16
Software license	
U4305A-EX3	License for Exerciser
U4305A-LT3	License for LTSSM
U4305A-MR2	License for Gen 2 MR-IOV virtualization
U4305A-022	License for ECRC error checking in the received TLPs and ECRC error insertion
U4305A-023	License for Gen 2 SR-IOV emulation
U4305A-024	License for a total of five virtual hierarchies

Accessories	
N5316A	Agilent PCIe test backplane

Additional information is available in the Protocol Exerciser for PCI express User's Guide, part number N5308-91010 in the Agilent Web site, **www.agilent.com**.

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