

ICT Boundary Scan Development Steps

Test point access and good data make all the difference.

BOUNDARY SCAN IS a limited access solution created to recover the coverage when test access is lost on a PCB. Test development is one of the critical stages to determine the success of boundary scan implementation at in-circuit test. This month, we look at several boundary scan ICT test development steps.

PCB boundary scan test point access. A critical step in implementing boundary scan test successfully is to ensure that access to test points is available for nodes needed for the test. Analyzing probe access on boundary scan using available ICT tools allows the test engineer to review the test access on the PCB.

One challenge of IEEE Std. 1149.1 and IEEE Std. 1149.6 implementation on PCBs is the availability of a compliant BSDL that is physically verified from the silicon. A BSDL file provided by the ICT is the only link between the test development engineer and the silicon device that describes the correct boundary scan cell type, sequence and number of cells, manufacturing identity code, boundary scan register length and other related information (**FIGURE 1**).

FIGURE 2 illustrates the importance of a BSDL test. In this case, an interconnect test with an inaccurate BSDL file describing a device

will have a catastrophic effect on the boundary scan testing, and result in an inaccurate failure analysis. A missing internal cell in the BSDL will result in a wrong boundary register description, and every device in the chain between the wrongly described device and TDI would be offset by the inaccuracy. A missing control cell in a BSDL designed to disable a pin would fail with incorrect diagnoses.

Boundary scan test generation.

Once the boundary scan devices, BSDL and board topology are described to the ICT development software, boundary scan test generation is automatic. The information provided permits the system to identify boundary scan devices and test types to be generated. The boundary scan tests are also executed in a sequence that helps identify failures and ensure the power is off to prevent further damage to the PCB.

ICT development software can generate the following boundary scan test (**FIGURE 3**):

- **Boundary scan disable.** Disables output pins of all boundary scan devices in a boundary scan chain.
- **Interconnect test.** Generates

interconnect test for IEEE Std. 1149.1 and IEEE Std. 1149.6 cells. Interconnect test checks for shorts, but most opens will also be detected for connection in between boundary scan cells and devices.

- **Buswire test.** Generated on bussed boundary scan cell drivers in a boundary scan chain. During buswire test, it turns on boundary scan drivers one at a time to check for opens, as well as verify the operation of bidirectional pins to check the operation, first as drivers, then as receivers.
- **Powered shorts test.** Tests for solder shorts in between boundary scan nodes and pins that do not have test access and node/pins that have test access physically close to each other. Tests selected boundary scan driver cells; those not selected are tested only as receivers.
- **Connect test.** Checks for open pins on boundary scan cell drivers and receivers of devices that have test probes assigned. For larger devices that exceed the available number of test-head resources (for example, testing a 300-pin ASIC when only 200 resources are available), or to minimize ground bounce caused by too many simultaneous transitions, automatically split the connect test into two or more smaller tests.
- **Silicon nail test.** Uses Boundary Register cells to replace physical probes or nodes. The Boundary Register cells that act as drivers and receivers, as shown in the device between the boundary scan devices, are typically a non-boundary scan part or a small cluster.
- **Cover-Extend.** A hybrid between vectorless test and boundary scan. Uses a sensor plate to detect signals on each

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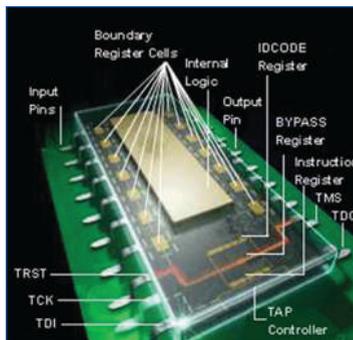


FIGURE 1. A boundary scan device.

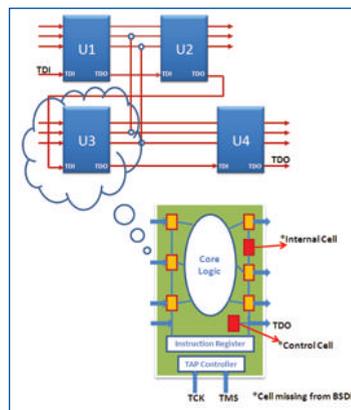


FIGURE 2. Inaccurate BSDL descriptions.

connector or non-boundary scan device pins connected to boundary scan cell drivers.

Developing ICT boundary scan tests. Here are best practices during boundary scan test development; all possible areas that could cause problems during testing are considered:

- Grounding is very important in any powered test in ICT. Make sure the board and test fixture have sufficient ground paths and returns for the types of devices to be tested. In particular, carefully consider boundary scan devices that will employ connect tests. If one of these devices has a large number of output pins that will be exercised during a connect test, grounding should be increased to prevent inadvertent state changes.
- ICT test development software typically should be able to minimize ground bounce by turning on ground bounce suppression during development. The boundary scan test generated by the software adds extra clock cycle to the test where state changes might cause a ground bounce.
- To ensure signal quality to the TAP (TDI, TMS, TCK and TDO), it should have the shortest twisted pair wire from probes to the test probe. This can be done by assigning a “CRITICAL” attribute to the TAP during development. The ICT test development software will assign the TAP first during probe placement to ensure the shortest wire in the fixture.
- TAP probe access should always be placed at the bottom of the PCB in order to have the shortest wire possible.
- Like any digital test, a boundary scan test should be treated the same. All surrounding digital devices and locks should be disabled to prevent interference to the boundary scan devices. The ICT test development software automatically generates a boundary scan test that will disable surrounding devices if you declare to the software how the device can be disabled. **CA**

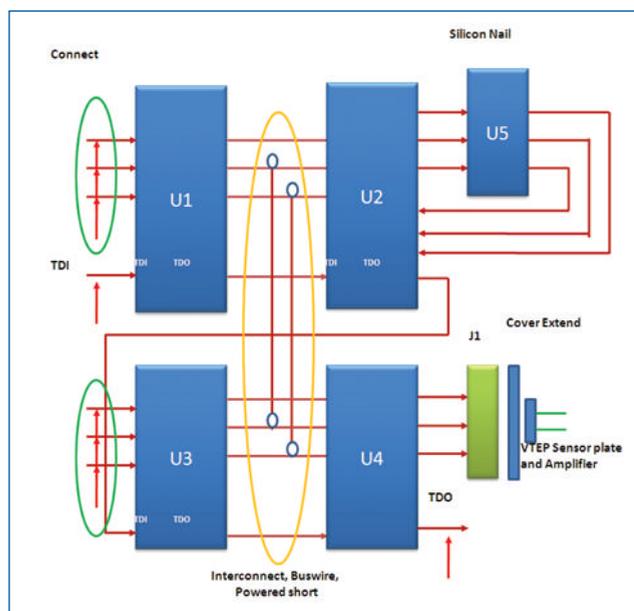


FIGURE 3. Circuit with Connect, Interconnect, Buswire, Powered short, Connect, Silicon nail and Cover Extend test.

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3. Agilent Medalist i3070 Boundary Scan training manual.
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ESDA, continued from p. 31

necessary. However, allowing operators to not wear wrist straps when seated, or allowing work surfaces with a higher resistance-to-ground than $1 \times 10^9 \Omega$, requires a tailoring statement. The tailoring statement must have technical justification and data to support the assertion that using the specification as-is is not necessary or deleterious to the product.

Additional thoughts. Products that fall into that “supersensitive” range may require efforts beyond the standard S20.20 program. For instance, for devices sensitive to charged device model damage, you may need to specify a minimum surface resistance value for work surfaces or anywhere else ESDS parts may touch, or you may need to limit metal-to-metal contact (say from tweezers or other tools).

You also may need to determine if more critical ionization is necessary to remove charge from product before it is handled or touched. Some companies are finding they must beef up the compliance verification program with more frequent or stringent testing. You also might benefit from beefing up training, highlighting critical items needed for the most sensitive products. Many companies dealing with ultrasensitive devices find that standard measurement tools are not enough. These companies find necessary the use of more robust process assessment tools, such as an electrostatic voltmeter and ESD event detectors. Some are using constant monitors for wrist strap, grounding and ionization verification to ensure these elements work continuously. Some companies have even implemented computer-based factory monitoring of these elements.

The “best” ESD control program is one that prevents any ESD damage to the components manufactured or handled, without overkill, resulting in expensive controls that may not be necessary. Certainly, an excellent place to start is to have a well documented and implemented S20.20 ESD control program. Additional controls may be necessary, depending on the sensitivity of the components handled and the manufacturing process complexity. **CA**

Ed.: For more on ESD programs, contact the ESD Association (esda.org).

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