

Agilent EEs of EDA

W1714 SystemVue AMI Modeling Kit

W1713 SystemVue SerDes Model Library

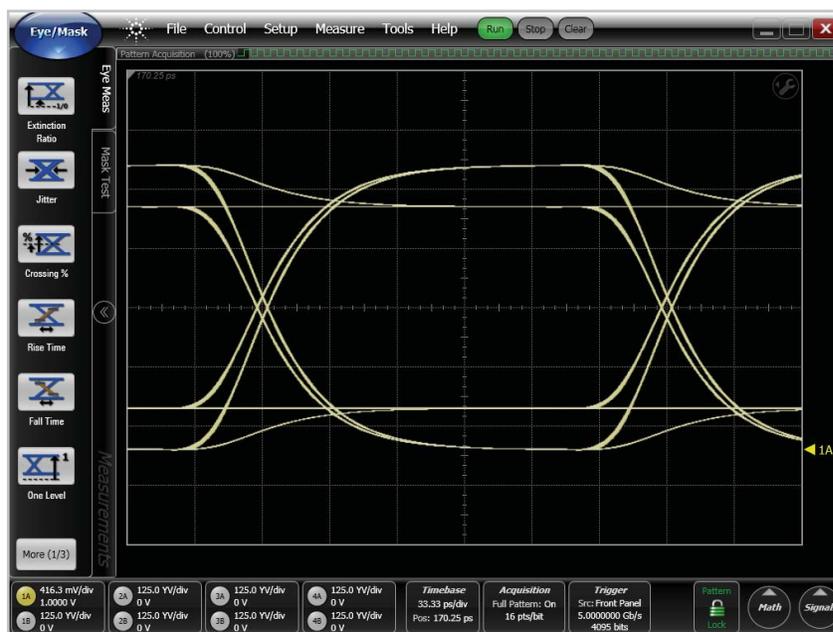
Data Sheet

Agilent's W1714 SystemVue AMI Modeling Kit consists of SerDes libraries for SystemVue plus automatic IBIS AMI model generation. The W1713 SystemVue SerDes Model Library is a subset of W1714 that omits its code generation feature. It is used for architecture optimization of a serializer/deserializer (SerDes) in cases where AMI generation is not required.

W1714 AMI Modeling Kit

"Do you really want to 'reverse engineer' the model out of the implementation? It often means sending all your IP out to a model building consultancy that also helps some of your competitors. With SystemVue, all your IP stays in-house."

The W1714 AMI Modeling Kit lets you optimize the signal processing blocks for your SerDes integrated circuit (IC) at the electronic system level (ESL). Once you've designed and optimized the algorithms, SystemVue automatically generates an IBIS AMI model that you can freely redistribute to your customers as an 'executable datasheet' to help them design your chip into their system.



This PCI Express transmitter model includes an IIR de-emphasis filter



Why IBIS AMI? Why now?

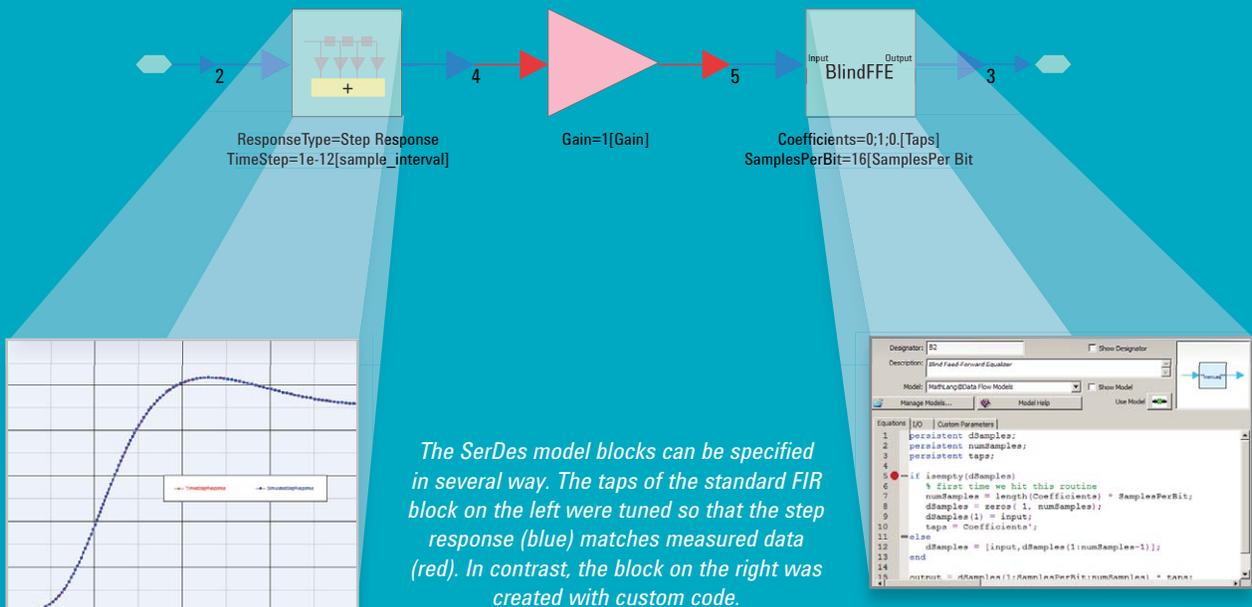
The motivating force behind the IBIS AMI modeling standard is the analog-to-digital transition in SerDes, which has had a big impact on model generation and simulation. Previously, SerDes were simple analog circuits with few—if any—register settings. IC vendors could provide SPICE netlist-based models of the small number of transistors in the circuit. For these relatively simple circuits, SPICE provided a throughput of perhaps a thousand bits per minute. This was acceptable because the OEM only had to do a small number of simulations. There were only a small number of points in the design space because there were only a few field-selectable register settings (e.g., gain or termination impedance value).

Although the circuits were small, the implementation details contained significant intellectual property (IP), which had to be protected with an encryption key specific to the EDA tool. Consequently, using a SPICE-like EDA tool was acceptable provided the IC vendor was prepared to create, verify and support multiple models—one for each EDA vendor’s encryption key.

Today, the situation has changed dramatically. Modern SerDes are mini communication systems with very complex digital signal processing and many field-selectable register settings, such as tap values, to optimize. Without IBIS AMI, the IC vendor would have to provide a model containing ten thousand transistors or more. It’s prohibitively expensive and unnecessarily wasteful in terms of compute time to model the behavior of multiply-accumulate logic by solving Kirchoff current laws. Instead, an EDA workstation can model that behavior natively and with 100% accuracy by using just one CPU instruction rather than the billions of cycles required to get the same answer via SPICE.

IBIS (Input-output Buffer Information Specification) is an industry standard, fast, behavioral “executable data sheet” of a chip I/O. AMI (Algorithmic Modeling Interface) is a feature that was introduced in IBIS version 5.0.

Unlike the traditional, analog part of the IBIS model (which is human- and computer-readable text-based specification of component values), the AMI portion is computer-readable machine-code executable that is dynamically linked into the EDA tool. Specifically, it’s a dynamic link library (DLL) on Windows® or a shared object on Linux. The machine code hides the IC vendors IP without the need for proprietary encryption. The code contains no implementation details: only a behavioral model of the digital signal processing used in the chip. The benefit to the IC vendor is that the model is ‘write once, run anywhere.’ The OEM gets a model that is very fast. This is because the AMI models are compatible with modern channel simulators like the one in Agilent’s Advanced Design System (ADS) software, which determine ultra-low BER contours in seconds using step responses and statistical techniques. With AMI models, it becomes practical for OEMs to run optimizing parameter sweeps on the end-to-end serial link to optimize the channel and tap values, as well as other field-selectable settings on each end of the SerDes links.



“Save time and reduce engineering costs by re-using the same Agilent toolset, from exploration to hardware implementation to live test.”

SystemVue reduces engineering effort and accelerates the maturity of SerDes designs for next-generation multigigabit transceivers (MGTs) in chip-to-chip serial links. It enables system architects, algorithm developers and hardware designers to investigate, implement and verify their SerDes signal processing blocks in the presence of interconnect impairment models similar to those encountered in the systems the SerDes will be designed into. The libraries give the user piece of mind that their product meets or exceeds real-world performance requirements from standards association for serial links like PCI Express and HDMI.

The W1714 AMI Modeling Kit provides measurement-hardened “golden reference” models that accelerate the SerDes design and verification process. The tool puts reliable Agilent measurement know-how at the front of the design process, where it improves the actual design, instead of only characterizing nonconformity after the fact. It can be used as a parameterized reference design to create test vectors for implemented blocks, or to fill in gaps to complete a fully-coded working chip-to-chip link, so that system-level performance can be continuously monitored.

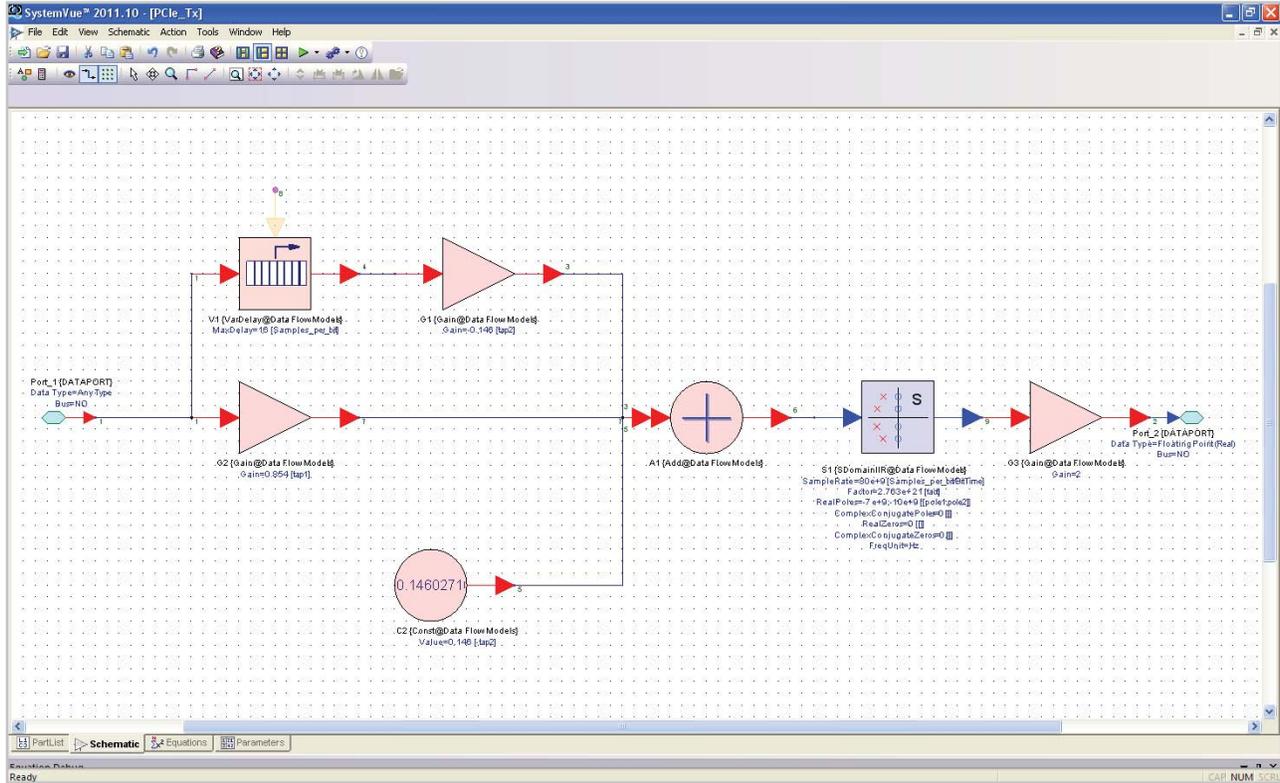
Why should I buy the W1714 AMI Modeling Kit?

- HDL simulators and SPICE aren't signal processing data flow tools. With SystemVue, you can rapidly optimize the signal processing with the right tool for the job.
- No need for slow and painful iteration at the implementation level. Implement the optimized architecture one time using the optimized SystemVue model as an executable specification.
- AMI is a natural by-product of the architectural model. It enables fast, accurate, automatic model generation with no risky disclosure of sensitive IP to a 'reverse engineering' model building consultancy. The IBIS AMI wrapper ensures standard compliance.
- No proprietary encryption. There is no need to verify and maintain multiple versions, one for each OEM's EDA tool. Instead, the W1714AMI Modeling Kit provides 'write once, run anywhere' functionality.
- Advanced functionality the goes beyond the present IBIS Ami standard to model repeaters and opto links.
- Generates all the files you need to ship your customer: *.ibs, *.ami, *.dll (for Windows executable), *.so (cross-compiled shared object for Linux). License includes royalty-free model redistribution rights.
- No need for the overhead of large, slow "run time" infrastructure files with your model. A simple .DLL is all that is needed for efficient simulation of your AMI interface.

The W1714 AMI Modeling Kit includes:

- BlindDFE Part
- BlindFFE Part
- CDR Part
- ClockTimes Part
- Coder64b66b Part
- Coder8b10b Part
- Decoder64b66b Part
- Decoder8b10b Part
- DFE Part
- FFE Part
- PhaseDetector Part
- PulseShaping Part
- SDomainIIR Part
- TimeResponseFIR Part
- VCO Part
- Standalone version of FlexDCA, the same eye pattern diagram software used in Agilent oscilloscopes.

W1713 SystemVue SerDes Model Library



A standalone license of FlexDCA – the same eye pattern diagram analysis tool used in Agilent oscilloscopes – comes with the product”

The W1713 SystemVue SerDes Model Library is a subset of W1714. It contains the same functional blocks as W1714 and is for architecture optimization of SerDes in the case where AMI generation is not required.

“If you don’t have a data flow model, you’re missing out on the chance to discover signal processing mitigations that overcome the severe impairments inherent in copper-on-FR4 interconnects.”

Non-portable proprietary extensions to generate mid-channel repeater and optical fiber communication link models

In addition to portable models, these products can also model mid-channel repeaters (both re-drivers that have no CDR, and re-timers that include a CDR) and optical fiber communication link models. Please note that unlike portable models (which run in any compliant simulator), models generated using proprietary repeater and opto extensions are non-portable and only run in SystemVue and ADS Channel Simulator. This is because IBIS doesn't presently support repeaters or opto links.

The repeater and opto link parts library includes:

- VCSEL driver
- VCSEL
- Multi-mode fiber
- PIN diode
- TIA

Requirements and Recommended Configuration

The W1713 SerDeS Model Library and W1714 AMI Modeling Kit require a core SystemVue platform (e.g., the W1461 SystemVue Communications Architect). In addition, W1714 requires the W1718 SystemVue C++ Code Generator.

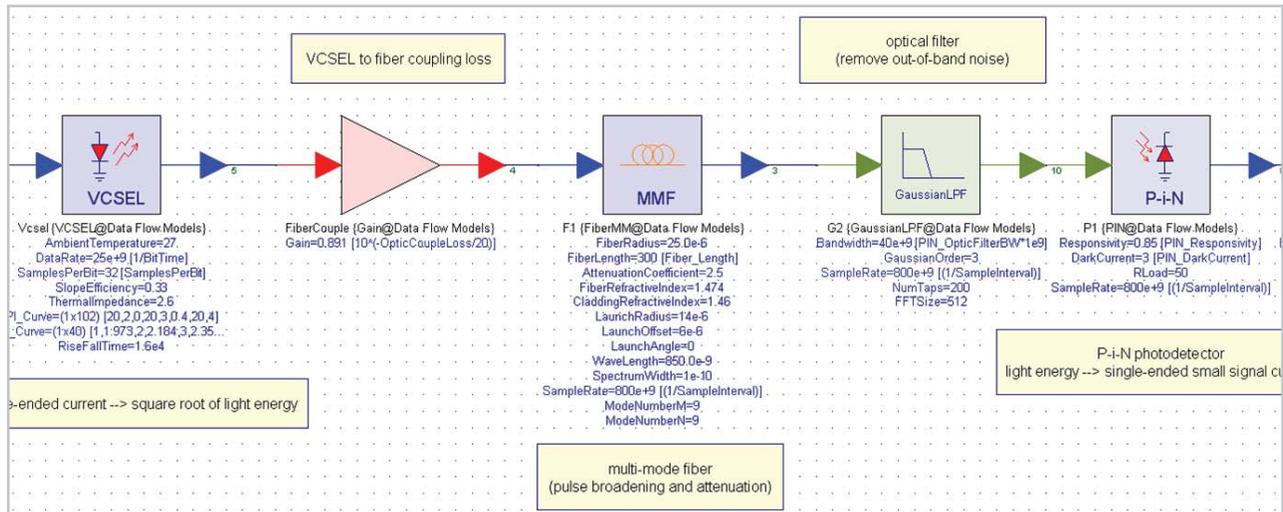
Application Examples included in W1714:

- Basic AMI model
- Parameterized response example
- PCI Express Gen2

How do I evaluate the W1713 SerDes Model Library and W1714 AMI Modeling Kit?

- View the video clips <http://signal-integrity.tm.agilent.com/2010/ibis-ami-faq/>
- Download the Technical Information Package from <http://www.agilent.com/find/eesof-ami-model-gen>
- Request an evaluation of SystemVue: <http://www.agilent.com/find/eesofsystemvue-evaluation>

"Implementation in your IC environment will proceed much more smoothly with the optimized SystemVue executable specification in hand."



Optical link model with vertical cavity surface emitting laser, multimode fiber, and photodiode.



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