Agenda

• DDR4 Technology Overview
• DDR4 Controller Phy and System Interconnect Validation and Compliance Test
• DDR4 Protocol Validation, BIOS and System Integration and Performance Optimization
• Design and Verification of DDR4 Physical Layer
• Wrap-up and Q&A Time
What is DDR4?

• Not just a DDR3 speed bump

• What you would expect:
  – Double the I/O rate to 3.2Gb/s
  – Reduced Vdd
  – Larger address space
  – More sophisticated training

• What you might not have anticipated:
  • Significant RAS and Mfg testability improvements
  • Rethinking of approach to AC Parametrics specification
  • Extensive protocol and signaling changes
  • Bank groups and “3DS” support from the start
DDR4 Pressed Hard Against the “Memory Wall”
Revolutionary Technologies Adopted in DDR4

“Memory Wall”

- **Signaling revolution**
  - Continuous forwarded clock
  - Extensive training on all signals
  - Controller based timing at DRAM
  - CRC with cancel on fail and retry
  - Move to serial/embedded clock

- **Interconnect revolution**
  - Direct die stacking
  - ~1000 signals die-die
  - Silicon Thru Vias

- **Computing revolution**
  - 1e2 to 1e7 processors
  - Mobile = desktop
  - Direct memory connect
  - I/O redefined?
  - “Functional” OS and Programming

Convergence?

- Speed x Interconnect Complexity
- Power x Cost Budget

- Graphics
- Computing
- Embedded / Mobile / Flash
Impact on Phy/Channel Design

- Microwave speeds on a very wide digital bus
- Hundreds (if not thousands) of design corners
  - Any one/combination could be the true “worst case” error generator
- New / Hybrid design techniques parallel AC Parametrics Test
- Crosstalk management more than twice as critical
- Maintaining power integrity is essential
- Phy / package / channel are truly a system
  - Accurate physical / design model correspondence essential
EDA Simulation for Enabling the Migration from DDR3 to DDR4
Outline

- Migrating the Channel from DDR3 to DDR4
- Pre-Layout “Getting to know the channel”
  - Serpentines vs. Switchback routing
- Post-Layout “Avoiding costly re-spins”
  - SI/PI Full-Path EM Simulations
- Measurement “How well does it work”
  - Fixture and Probe Loading
- Conclusion
## Migrating from DDR3 to DDR4

### The Basics

<table>
<thead>
<tr>
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<th>DDR3</th>
<th>DDR4</th>
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</thead>
<tbody>
<tr>
<td><strong>Signal Integrity</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Speed</td>
<td>2133 Mb/s</td>
<td>3200 Mb/s (goal)</td>
</tr>
<tr>
<td>3rd Harmonic</td>
<td>3.2 GHz</td>
<td>4.8 GHz</td>
</tr>
<tr>
<td>Unit Interval</td>
<td>938 pS</td>
<td>625 pS</td>
</tr>
<tr>
<td><strong>Power Integrity</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vdd</td>
<td>1.5 V</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Max Ripple</td>
<td>+/- 75 mV</td>
<td>+/- 60 mV</td>
</tr>
</tbody>
</table>

- Timing Window Reduced by 34%!

Requires 20% better Voltage Control
And a drop in PDN target Z
Why DDR4 Memory is a Challenge Compared to SERDES?

• Single Ended bi-directional DQ bus running at 3.2 GB/s on FR4 material with source synchronous clocking.

• Large Single Ended $di/dt$ creates X-talk and increases sensitivity to Return-Path Discontinuities

• No Equalization

• Limited pre-/de-emphasis techniques

• High Density Interface: Almost 150-signals routing

• SDRAM is a cheap Commodity device: Typical SDRAM eats 45% of the eye & Controller eats another 30%. ONLY 25% of the UI or $156\text{pS}$ for DDR4 is left for the FR4 channel.
Getting to Know the Channel
DDR4 PCB Layout Design Rules

Losses, Crosstalk, and EMI

- Routing Impedance
- Trace Width and Spacing
- Material stack-up
- BGA Trace Necking
- Via Transitions
- Reference Plane Transitions
- PDN Impedance
- Skew Routing Compensation

DDR DQ Byte Lane Model for Design Exploration

Model Variables Available for Tuning, Optimizing, and Design of Experiments
DDR Skew Compensation with Serpentine Routing

Source Synchronous Clocking of DQ Byte Lanes Requires Matched Channel Lengths
Electrical Length not Physical Length for DDR4

**PHYSICAL LENGTH MATCHING**
- Start: *Edges Aligned*
- End: *Edges are Skewed*

**ELECTRICAL LENGTH MATCHING**
- Edges Aligned, No Skew

23 mm Serpentine

23 mm Switch-Back

13 pS

Longer 23 mm Serpentine

2 mm Length Difference

Shorter 21 mm Switch-Back
Limited PCB Routing Space – Maximizing Density

Switchback routing results in less skew when utilizing Physical Lengths in a PCB CAD tool for length matching.

Serpentine with minimum layout width requires significantly more length for skew matching as compared to switchback routing.
DDR 4 Eye Mask Position and Margins

Eye mask is centered on DQS crossing and Vcent.

Any skew between DQS and the DQ will reduce margins.

Skew from Serpentine Routing with Physical Length Matching can result in 5% to 10% of the available DDR4 allocation for the channel timing budget.
Post-LAYOUT ADFI for Importing PCB Designs

1. Layer Selection Tools and Fabrication Details

2. Intelligent Net Selection
   Cookie Cutting

3. EM Simulation

4. EM S-Parameter Model
   Co-Simulation

5. DQ Signal Eye Diagrams

6. DDR Compliance Report
Post-Layout Full EM for Power Integrity

Samsung DDR3
PC3-UDIMM V102

© JEDEC, permission obtained to be used in EEs of training examples

POWER INTEGRITY SIMULATION

Impedance at Each IC, no Caps
How Well Does It Work.....
Measurement Probing Design Requires Simulation

- In-Situ probing at speed requires inserting a connection in the signal path.
- Simulation optimizes topology as well as optimum location for accurate probing.

Buried isolation resistor
Optimizing Probe Load and Bandwidth

Signal Loading  Conflicting Requirements  Bandwidth
Probe Load Impact on Signals

- Jitter/Noise added at DRAM
- Load Isolation / Probe BW
- Probe Bandwidth
- Instrument

Simplified schematic for each probed signal
Where to Go Next……..


- Integrated DesignGuides, Compliance DesignKits, and Examples:
  - IBIS AMI, DDR, PCIe, USB, HDMI, SAS2, UHS2

[agilent.com/find/signal-integrity](http://www.agilent.com/find/signal-integrity)
Impact on AC Parametrics Test

• Probing bandwidth

• New/Hybrid measurement techniques
  – High speed serial: Jitter and noise decomposition and extrapolation
  – Parallel memory timing: Protocol sensitive timing

• Four port de-embedding
  – Crosstalk
  – Virtual probing of controller and interconnect including packaging and die

• Importance of bus-wide SI insight
Making Your Most Accurate DDR4 Compliance Measurements

Ai-Lee Kuan
OPD Memory Product Manager
Agenda

• DDR4 Testing Strategy
  • Probing
  • Analysis Tool
  • Compliance Test
• Conclusion
DDR4 Testing Strategy

1. Choose the right probe and location to probe

2. Pick the oscilloscope with the most comprehensive analysis capability

3. Use the automated compliance app software to ensure compliance as per the JEDEC standard and repeatability
Probing
Steps to ensure probing success

1. Probe location
2. Simulation
3. De-embedding
Probe location

JEDEC specification is defined at the ball of the DRAM package.

Probing at transmission lines or surface mount components cause signal reflection and other SI issues.

Probing at the wrong location causes reflection, resulting in non-monotonic edges. This will cause error in your tests such as slew rate, setup and hold time measurements.
DDR4 BGA Interposer

DDR4 x4/x8 pin-out

Agilent

Note: All signals available at probe points except power, Vref, RFU

DDR4 DRAM

Riser

Elevates the interposer for smaller surface keep-out area

Scope pad points
Simulation

Why is simulation required?

- Check system operation with the added interposer loading
- Evaluate the bandwidth/frequency response of the measurement
- Determine what kind of de-embedding is (or may be) required

Smaller eye due to probe loading
De-embedding with InfiniiSim

Physical layout of a board

InfiniiSim General Purpose 9 Blocks Topology

GPU / Memory controller

DRAM probe

InfiniiMax probe head

Delay

Measurement

InfiniiMax General Purpose 9 Blocks Topology

Simulation

GPU / memory controller

BGA probe WCK s4p/ DQ s2p file

InfiniiMax probe head s1p file

Save configuration as transfer function file

Unloaded signals

GPU / Memory controller

DRAM probe

InfiniiMax probe head

Measurement

Unloaded signals
Benefits of de-embedding

Before de-embedding

Channel 1: Probing at VIA (under the DRAM)
Channel 2: Probing at scope pad point

After de-embedding

Channel 1: Probing at VIA (DQS strobe)
Channel 2: Probing at scope pad point

Channel 2 Frequency Response
Write Eye Diagram

Example with GDDR5 BGA interposer

**InfiniiSim ON**
- Rise time improved with de-embedding
- Eye diagram does not violate mask test

**InfiniiSim OFF**
- Slower rise time
- Eye diagram violates mask test
Write Eye diagram – Mask Unfold

InfiniiSim On:
Mask failure removed with InfiniiSim

InfiniiSim Off:
Mask failure caused by probing effect
DDR3 signals

1. DQS Read pre-amble
2. DQS Write pre-amble
3. DQ tri-state
Read/Write cycle

1. DDR4 read/write pre-amble pattern is similar to DDR3 write pre-amble pattern (one clock cycle).
2. No Hi-Z state on DQ (same as GDDR5 data). DQ is driven high all the time.
Separate read/write manually with InfiniiScan

Use InfiniiScan “Zone Qualify” to trigger on Read or Write burst. A zone is drawn on one of the distinctive waveform of the Read and Write bursts patterns.

There are 2 distinctive Read and Write burst patterns.
Separate read and write with MSO

• 4 analog channels – DQS, DQ
• 16 digital channels – CLK, RAS, CAS, WE, CS

MSO90000 X-Series Infinium Mixed Signal Oscilloscope

• Up to 33 GHz bandwidth
• Up to 20GSa/s sample rate
• 500Mpts memory depth

Mixed Signal Oscilloscope Ensures Read/Write Separation with command protocol
N6462A DDR4 Compliance Test Software

What are we testing?

- Clock Tests
- Electrical
- Timing
- Eye diagram

DDR4 Speed grades: 1600, 1866, 2133, 2400, 2666, 3200 MT/s (as per JESD79-4)
Electrical Tests

DQ Overshoot Amplitude

SRQseR
Timing Tests

- WRITE cycle tests
  - tWPST
  - tWPST

- Command Address Timing
  - tCKE

- READ cycle tests
  - Data Timing
    - tDQSQ
    - tQH
    - tLZDQ
    - tHZDQ
  - Data Strobe Timing
    - tRPST
    - tDQSCK
    - tDVAC(Clock)
    - tLZDQS
    - tHZDQS
    - tQSH
    - tQSL
    - tDVAC(Strobe)
**DDR3 Read/Write Eye diagram test**

Eye Diagram Test (not required per JEDEC spec)
- Allows measurement of Data eye height and eye width
- User can also define own mask as per device specification

Compliance app reports **Fail** status if eye diagram violates mask
The smallest margin to the mask of the 4 timing points is reported as tDIVW measurement result.
% Margin is then \( \frac{\text{Actual-Spec}}{\text{Spec}} \times 100\% \) or \( \frac{118.8\text{ps}-62.5\text{ps}}{62.5\text{ps}} \times 100\% = 90\% \)
Ringback could cause the measurement using the mask corners to be incorrect.

VdiVW – voltage must stay above/below VdiVW for TdiVW time.

Margin should really be the min voltage in the entire TdiVW range.
Test Result of TdiVW

Marker is placed on the worst case margin

4 corners actual values
Compliance app reports the following information:

1. Worst case value with screenshot.
2. Pass/fail status with margin
3. Multiple trial run results.
4. Statistical report of min, max and std dev.
HTML report is presented for reporting purposes. Provides details of test result with screenshot of worst case value.
Other Features for Margin Testing

Multi-burst and Multi Acquisition on Electrical and Timing tests:
- Characterize device for margin testing

Auto configuration for Voltage thresholds.
- Flexibility to test with non-standard operating voltages
Multi-Burst Measurement for Statistical Analysis

Multi-burst measurement allows measurement of multiple bursts in a single acquisition or multi-acquisition for statistical analysis – Min, Max, Mean, Stdev
Automated Threshold Settings for DDR4 Characterization

The intuitive GUI in the automated compliance app allows for measurement of non-standard DDR voltage levels. For example, 1.15V.
Conclusion

1. DDR4 speeds requires **new AC timing parameters** to be measured in a new way.

2. Speed to market depends on efficiency and reduced design cycles and cost. **Pick the tools** that would achieve this.

3. **Partner** with your tool vendor.
Impact on Protocol Test

• Probing density
• KoV approaching zero
• Extremely small data eye
  – Voltage AND time squeezed per spec
  – Degraded eye at DIMM connector
• Importance of training validation
• Analyzer setup must be highly automated
  – Per-DRAM configuration
  – More complex protocols and training
DDR4 Debug and Protocol Validation Challenges

Presented by:
Jennie Grosslight
Memory Product Manager
Agilent Technologies
Agenda:

- Overview of logic analysis for DDR4 Debug and Validation
- Examples:
  - Boot issues
    - Demo
  - System failures
  - System Validation and optimizing performance
- Summary
Benefits of Logic Analysis:

**Logic Analyzer Modes**

- **View when events happened.**
  Timing mode and Transitional Timing Modes
  Asynchronous to system under test.

- **Follow what happened**
  State Mode
  Synchronous to clock from system
  Enables most powerful SW tools

- **High resolution around trigger event.**
  Timing Zoom
  *Simultaneous with State or Timing modes*

- **Bus Level Signal Integrity Insight – Eye Scan**
  Qualitative comparison of eye diagrams relative to each other
Logic Analyzer solutions for DDR4

Connect

Interposers
BGA Probes
Mid-Bus Probing

Acquire

Captures highest data rates!
4 Gb/s
Capture smallest eyes.
100mV x 100ps at probe point.
Sequential Triggers up to 2.5GHz!

View & Analyze

DDR Decoders
DDR Protocol
Compliance
Performance Analysis
Trigger

Bus Level Signal
Integrity Insight
Data Valid Windows Shrinking

- Data Rates Increasing
- Voltage levels decreasing
- Different Signal integrity - different systems

Read DDR4 1600
Data valid windows scanned on U4154A logic analyzer with FS2501B DDR4 DIMM interposer on different DDR4 targets.

Read DDR4 1867
Read DDR4 2400

These DDR4 2400 and DDR4 1600 eyes were less than 200mV at the DDR4 interposer!
The logic analyzer must be able to capture signals smaller than 200mV x 200ps at the probe point.
Bus Level Signal Integrity Insight:
– Bridging a measurement gap

**Design**
EEsof EDA

**Signal Integrity**
Infinium 90000 Series Scope
InfiniiMax Probes

**Functional Analysis and Validation**
Plus Bus Level Signal Integrity Insight

- DDR4 Logic analysis
- U4154A Logic Analyzer Modules
- In M9502A Chassis
- With FS2501B DDR4 DIMM interposer

- Overlay Scans
- Burst Scans

5ps x 2mV Sample position resolution

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Agenda:

- Overview of logic analysis for DDR4 Debug and Validation
- Examples:
  - Boot issues
  - System failures
  - System Validation and optimizing performance
- Summary
Simplified Debug and Validation:

1. Get system to Boot!
2. Fix System Crashes or Failures
3. Validate and Optimize Performance
Test Tools and Techniques for Boot Challenges:

System boot Challenges:
* Doesn’t boot
* Intermittent boot
* Incorrect settings during boot (initialization)

Timing Modes: Standard and Transitional
* Time out triggers
* Timing Zoom – up to 256k deep
* View signal timing relationships

State Mode
* Decode Initialization
* Use store qualification to conserve LA memory
* Follow signal flow

Compare Window to debug intermittent boot

Eyescans of ADD/Control signals
* Quickly identify abnormalities
DDR4 Logic Analysis Demo

• High Level Waveform insight
• Initialization signal flow.
• Scroll through Eye Scans
• Expected DQS_W behavior
Example #1: DDR4 DQS Write – Training Issue!

Timing Zoom 256k high resolution trace. Shows DQS_Write training incorrect.
Test Tools and Techniques for System Failures:

System failures-
What Happened?
System crashes or non-crash system failures.

High Level Views of Traffic

State mode
* Easy setup with Setup Assistant
* Case Study: Follow signal flow with precise triggering and full decode.

Bus Level Signal Integrity Insight
Case Study: Following Signal Flow.

Description: System Writes DEADBEEF to restricted address when SW detects corrupt data from any address.

Engineers need to figure out: **What caused corruption?**

Logic Analysis trace shows **exact Write and Read traffic**, this allows the user to understand:

- Was WRITE or READ corrupt?
  - *Cuts problem in half*

- ‘What was system doing leading up to failure?’
  - Follow signal flow leading up to failure.
  - Understanding leads to root cause of issues.
CS: Capturing Trace from Exact Data Burst

Example:
This system writes DEADBEEF to restricted address when SW detects corrupt data.

Logic analyzer triggers on exact data burst.
CS: What Happened?

Trace shows all traffic leading up to notification of bad data.

Write burst of interest was -5187 samples before trigger.

• Pattern was NOT what should have been written.

Read burst of interest was -4077 samples before the trigger.

• Read is same pattern that was written into address space

• **Problem isolated to Writes!**
CS: Following the Signal Flow *Next steps…*

**Check Write Eye Scans**
- Does DQS to DQ relationship look correct?
  - DQS Write edge approx centered on DQ eye
  - System variable, know your system!
- If an issue is seen:
  - Observe high resolution timing traces Writes
  - Cross trigger scope from LA

**Next:** Run Protocol Validation tools. Errors can corrupt Writes to memory.
Test Tools and Techniques for System Validation and Optimizing Performance:

* Protocol compliance tools
* Post process
* Real time

System Validation and Performance Optimization

* Performance tool
Post Process vs. Real-Time Violation Detection

Biggest difference: Post process is limited to trace depth.

- Typically milliseconds to maximum of a few seconds

Real-Time: user selects coverage time

- seconds, minutes, hours ......

Typical coverage using post process methods

Anticipate __ Accelerate __ Achieve

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Post Process vs. Real-Time Violation Detection .....continued

Post Process Benefits

... Why use if Real-Time is available?

- Quick check of Logic Analyzer trace for possible violations
- Easy method to check a trace of a system crash
- Typically optional SW tool on logic analyzer

Example:
Time out trigger to capture trace of system crash

*DDR system stops writing to memory when system crashes*
Post Process vs. Real-Time Violation Detection .....continued

- Post Process results example
- Run on logic analyzer trace
Real-Time Compliance SW tool on Logic Analyzer

- Select technology
- Edit Parameters
- Load Data Rate tests
- Create custom tests
- Select time to run
Real-Time Compliance SW tools on Logic Analyzer

- Select Run options
- Run
- View Violation results

Traces of violations saved in directory of your choice.
Open Violation traces to view details
Real-Time Compliance SW tools on Logic Analyzer

Real-Time trace example:
Trigger on tRCD violation
Write too close to Activate
B4622B: Performance Analysis Tool

- Simple yet familiar format
- Overview showing quick DDR performance index
- Is my bus efficient?
  - Data Bus Utilization: 33.976 %
- Address access count in histogram view
- Read/Write efficiency check
Agenda:

• Challenges for DDR4 Debug and Validation
  • Overview of logic analysis
  • Case Studies and Examples
    • Boot issues
    • System failures
    • System Validation and optimizing performance

• Summary
Conquering Memory Debug & Validation Challenges

Accelerate Insight
* View when events occurred.
* Follow signal flow.
* Understand, “What happened?”

Bus Level Signal Integrity Insight

Probing
DDR4 DIMM, SODIMM, BGA interposers, and mid-bus
# Key Differences between DDR4 and DDR3 for Functional Debug and Validation

<table>
<thead>
<tr>
<th>Key Technology Differences</th>
<th>Impact on Debug and Validation</th>
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</thead>
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<tr>
<td>Different pinouts: BGA, DIMM, and SODIMM</td>
<td>New probing required</td>
</tr>
<tr>
<td>Higher data rates</td>
<td>Smaller data valid windows, <em>Especially from midbus probing or DIMM/SODIMM interposers to logic analysis.</em></td>
</tr>
<tr>
<td>Lower signal voltages</td>
<td></td>
</tr>
<tr>
<td>New Command/Address latency (CAL)</td>
<td>Different Decode and Compliance Tools</td>
</tr>
<tr>
<td>Switched memory bank option for servers, New Signals:</td>
<td></td>
</tr>
<tr>
<td>ACT</td>
<td></td>
</tr>
<tr>
<td>BG</td>
<td></td>
</tr>
<tr>
<td>Threshold for Read eyes is higher than threshold of Write eyes.</td>
<td>Test equipment must accommodate different thresholds.</td>
</tr>
<tr>
<td>DDR4 termination DQ stay high unless driven low. (pseudo-open drain (POD) drivers with Vdd terminations.)</td>
<td>State mode tuning techniques change from DDR3.</td>
</tr>
</tbody>
</table>

*Anticipate Accelerate Achieve*

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New DDR4 Interposers

Introduced  April 10th, 2012

- Requires two U4154A modules with option -02G
- Timing and State analysis
- DDR Eyescans
- Includes FuturePlus protocol decoder to show executed bus transactions

FS2501B: DDR4 2400 DIMM interposer

FS2502B: DDR4 1867 SODIMM interposer
1 Protocol Violation checks
   • Post process testing
   • Same framework as Scope Compliance tool.

2 Performance Analysis
   • Provides bus statistic information.
   • Provides histogram view on number of access at a specific memory address

3 DDR2/3 Trigger setup
   • Enable automation of creating trigger on physical address

4 NEW! Real time Protocol Compliance tool with custom violation option!
State Mode: Initialization Capture and Decode

Filter NOP Trigger. Stores valid commands and Data bursts. Doesn’t store NOP/Deselect
Wrap-up

• DDR4 brings revolutionary (for memory) approaches to evolutionary DRAM generation

• Significant impact on specification, design, physical and protocol measurement

• Power, speed and density improvements appeal to embedded, desktop and server computing

• May enjoy a longer than “normal” lifetime as a primary memory technology

• DDR4 expertise likely to have good ROI despite signaling and protocol complexity
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(BP-3-1-13)

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Published in USA, March 19, 2013
5991-2149EN