



**Agilent Technologies**

# Gain Compression Simulation

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# Chapter 1: Gain Compression Simulation

To calculate the X dB gain compression point of an amplifier or mixer, use the XDB simulation component, from the Simulation-XDB palette. The simulator sweeps the input power upward from a small value, and when the required amount of gain compression is seen at the output, the analysis is complete. A common calculation is the 1-dB gain-compression point; this is the default.

Refer to the following topics for details of gain compression simulation:

- [“Performing a Gain Compression Simulation” on page 1-2](#) describes the minimum setup requirements for a gain-compression simulation.
- [“Example \(ADS only\)” on page 1-3](#) is a detailed setup for calculating gain compression, using a power amplifier as the example.
- [“Gain Compression Concept” on page 1-8](#) is a brief explanation of the gain compression calculation, plus information on how it compares to a harmonic balance simulation.
- [“XDB Simulation Parameters” on page 1-9](#) provides details on the tabs and fields in the XDB simulation controller.

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**Note** You must have the Gain Compression license to run the simulator. You can build the examples in this chapter without the license, but you will not be able to simulate them.

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## Performing a Gain Compression Simulation

Start by creating your design, then add current probes and identify the nodes from which you want to collect data

For a successful analysis:

- Use port-type sources at the inputs, such as the P\_1Tone under *Sources-Freq Domain*.
- Terminate outputs with port-impedance terminations. You can find this type of port under *Simulation-S\_Param*. Verify the impedance value.
- The *Num* values in the port-impedance terminations are used to specify input and output ports.
- Add the Gain Compression control element to the schematic. Fill in the fields under the Freq and XdB tabs:
  - For Freq, set the fundamental frequency and order
  - For X db, specify the input and output ports, the frequency at each port, power variation for each port, and maximum input power.
- For a faster simulation of large circuits, use the Krylov option. Refer to the topic “Selecting a Solver” in the chapter “Harmonic Balance Basics” in the *Harmonic Balance Simulation* documentation for instructions on how to use this option.
- You can use previous simulation solutions to speed up the simulation process. For more information, refer to the topic “Reusing Simulation Solutions” in the chapter “Harmonic Balance Basics” in the *Harmonic Balance Simulation* documentation.

For details about each field, click *Help* from the dialog box.

## Example (ADS only)

Figure 1-1 illustrates the setup for a basic gain compression simulation of a power amplifier circuit.

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**Note** This design, *XDB1.dsn*, is in the *examples* directory under *Tutorial/SimModels\_prj*. The simulation results are in *XDB1.dds*.

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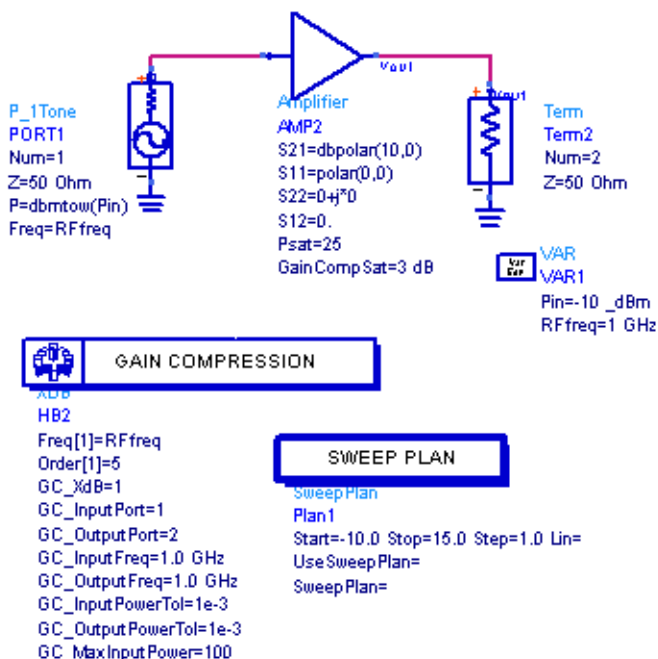


Figure 1-1. Gain-compression simulation example

To perform a gain-compression simulation:

1. From the **Sources-Freq Domain** palette, select a port-type source such as a *P\_1Tone* or *P\_nTone*. Place the source at the input of the component or circuit under test, then define input power and edit other parameters as required.
2. From the **Simulation-S\_Param** palette, select a **Term** component and place it at the output of the component or circuit under test. Edit the impedance if necessary.

3. Ensure that the input port source is identified as Num=1, and the output port termination as Num=2. Also ensure that you have labeled the inputs and outputs of nodes at which you want data to be reported.
4. From the **Simulation-XDB** palette list, select an **XDB** simulation component, and place it on the schematic, then edit it.
5. Select the **Freq** tab, and edit frequencies, orders, and fundamentals as required.

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**Hint** In a one-tone simulation such as this one, *MaxOrder* is irrelevant.

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- Ensure that values are established for all of the frequencies of interest (for example, RF, LO, and IF frequencies) in the design under test. (Where mixers are employed, set the LO frequency to Freq[1]; it is easier to achieve convergence if the frequency of the signal with the largest amplitude is assigned to Freq[1].) To add or delete frequencies, select them in the *Select* field, then click *Add* or *Cut*. Display them on the schematic to facilitate editing.
6. Select the **X dB** tab and set the following:
    - In the *Gain compression* field, either accept the default or enter a new gain-compression value. The default is 1 dB.
    - Under *Port numbers*, ensure that appropriate values are entered for the input port source (generally Num=1) and the output termination (generally Num=2).
    - Under *Port frequencies*, set appropriate values for the input and output frequencies. In a circuit employing a mixer, the input frequency would be that of the RF input, the output frequency that of the IF output.
    - Under *Power tolerances*, set appropriate values for acceptable variations in power at the input and output ports. In the *Max. Input Power* field, set the maximum input power over which the simulator is allowed to search.

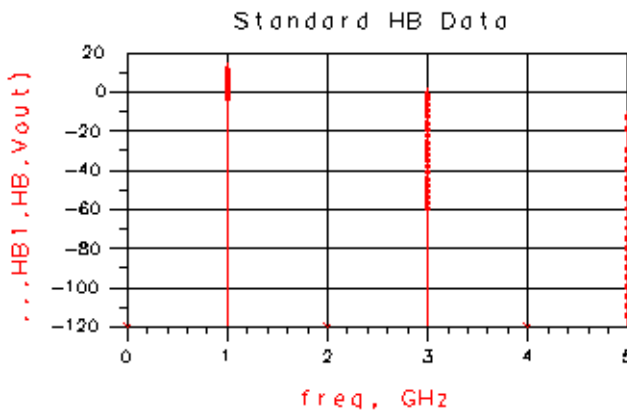
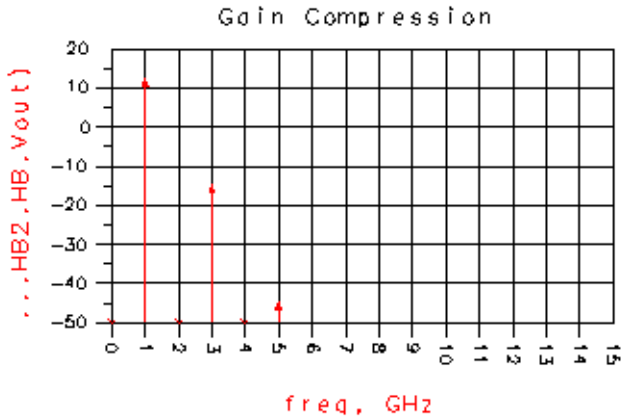
7. To reduce memory requirements significantly where many frequencies and orders are involved, select the **Solver** tab, then select **Krylov Solver**.

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**Note** We do not recommend using the Krylov option on small problems. For details, refer to the topic “Selecting a Solver” in the chapter “Harmonic Balance Basics” in the *Harmonic Balance Simulation* documentation.

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8. **Simulate.** Gain compression data items may be identified with an HB prefix. The following is a Rectangular plot of the results of the simulation. At the top are the gain compression results, with the standard harmonic balance results at the bottom for comparison.

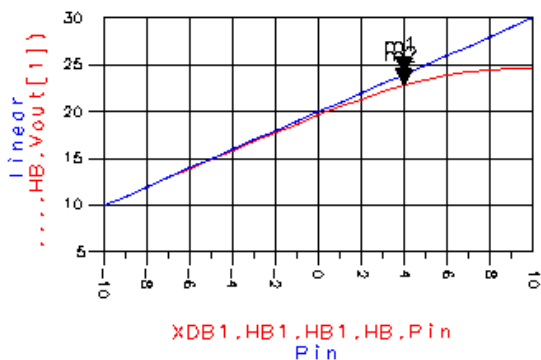


The following graphs and their associated equations illustrate how to extract more meaningful results from the simulation. The equation *Gain* finds gain by subtracting the input power  $P_{in}$  from the output voltage of the fundamental [Vout[1]]. The equation *linear* adds input power to gain to produce the linear plot in the graph. To find the input power that leads to a compression point of approximately 1 dB, place a marker on each trace and move them so that their difference is as close to 1 dB as the simulation results allow. The simple equation *compression* subtracts the values of the markers, and a List plot of that equation shows the input power that yields a gain compression of approximately 1 dB.

$$\text{Eqn } \text{linear} = \text{Gain}[1] + \text{XDB1.HB1.HB1.HB.Pin}$$

$$\text{Eqn } \text{Gain} = \text{dBm}(\text{XDB1.HB1.HB1.HB.Vout}[1]) - \text{XDB1.HB1.HB1.HB.Pin}$$

$m_1$ $\text{Pin} = 4.000000$ $\text{linear} = 23.951017$	$m_2$ $\text{XDB1.HB1.HB1.HB.Pin} = 4.000000$ $\text{dBm}(\text{XDB1.HB1.HB1.HB.Vout}[1]) = 22.815169$
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$$\text{Eqn } \text{compression} = m_1 - m_2$$

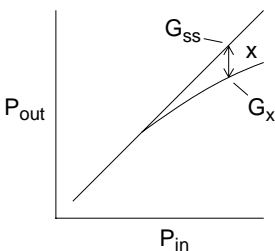
Pin	compression
4.000	1.136

## Gain Compression Concept

Gain compression is the difference, in dB, between a point on an idealized linear (small-signal) power-gain slope and a corresponding point on the actual power curve. That is, for a gain compression of  $x$  dB,

$$-x = 10 \log_{10} (G_x / G_{SS})$$

where  $G_x$  is the point on the idealized linear gain slope that is  $x$  dB directly below the point  $G_{SS}$  on the small-signal power curve, as illustrated below.



The simulator stops its analysis when it reaches that point. The default setting is 1 dB.

The XDB simulator uses a harmonic balance algorithm, and as such shares many of the parameters and options that the Harmonic Balance simulator provides. However, this simulation requires that the input and output of the component or circuit whose gain compression is being simulated be defined by an appropriate source and termination.

# XDB Simulation Parameters

The Gain-Compression (Xdb) Simulation controller enables you to define these aspects of the simulation:

- **Freq**—Frequencies of fundamentals and status level for summary information.
- **XdB**— Gain compression, port numbers and frequencies, and port tolerances
- **Params**—Parameters related to device operating-point levels, FFT oversampling and convergence, initial guess, writing final solution to a specified file, budget simulation, and harmonic balance assisted harmonic balance.
- **Solver**—Set up convergence mode, matrix solver, and memory management.
- **Output**—Selectively save simulation data to a dataset. For details, refer to the topic “Selectively Saving and Controlling Simulation Data” in the chapter “Simulation Basics” in the *Using Circuit Simulators* documentation.
- **Display**—Control the visibility of simulation parameters on the Schematic. For details, refer to the topic “Displaying Simulation Parameters on the Schematic” in the chapter “Simulation Basics” in the *Using Circuit Simulators* documentation.

## Freq

Following are descriptions of the fields to set up frequency for this component. In the following table, names used in netlists and ADS schematics appear under *Parameter Name*.

**Table 1-1. XDB Simulation Freq Options**

Setup Dialog Name	Parameter Name	Description
Fundamental Frequencies		
Edit		Edit the Frequency and Order fields, then use the buttons to Add the frequency to the list displayed under Select.
Frequency	Freq[n]	The frequency of the fundamental(s). Change by typing over the entry in the field. Select the units (None, Hz, kHz, MHz, GHz) from the drop-down list.
Order	Order[n]	The maximum order (harmonic number) of the fundamental(s) that will be considered. Change by typing over the entry in the field.
Select		Contains the list of fundamental frequencies. Use the Edit field to add fundamental frequencies to this window.  Add -- Allows you to add an item. Cut -- Allows you to delete an item. Paste -- Allows you to take an item that has been cut and place it in a different order.
Maximum mixing order	MaxOrder	The maximum order of the intermodulation terms in the simulation. The combined order is the sum of the individual frequency orders that are added or subtracted to make up the frequency list. For example, assume there are two fundamentals and Order (see below) is 3.  If Maximum order is 0 or 1, no mixing products are simulated. The frequency list consists of the fundamental and the first, second, and third harmonics of each source.  If Maximum order is 2, the sum and difference frequencies are added to the list.  If Maximum order is 3, the second harmonic of one source can mix with the fundamental of the others, and so on.
Levels—Enables you to set the level of detail in the simulation status report.		
Status level	StatusLevel	Prints information about the simulation in the Status/Summary part of the Message Window. A value of 0 causes no or minimal information to be reported, depending on the simulation engine. Higher values print more detail.  The type of information printed may include the sum of the current errors at each circuit node, whether convergence is achieved, resource usage, and where the dataset is saved. The amount and type of information depends on the status level value and the type of simulation.

# XdB

Following are the fields used to define XDB simulation. In the following table, names used in netlists and ADS schematics appear under *Parameter Name*.

Table 1-2. XDB Simulation X dB Options

Setup Dialog Name	Parameter Name	Description
Gain compression	GC_XdB	Enter the gain compression, the default is 1 dB.
Port numbers		
Input	GC_InputPort	The number of the input port.
Output	GC_OutputPort	The number of the output port.
Port frequencies—Ports must be placed and defined. Set the port number of the input source to 1, and the port number of the output Term (termination) component to 2, then set frequencies.		
Input	GC_InputFreq	The frequency of the input port.
Output	GC_OutputFreq	The frequency of the output port.
Power tolerances		
Input	GC_InputPowerTol	The variation in power, measured as a change in dB (delta dB), allowed at the input port.
Output	GC_OutputPowerTol	The variation in power, measured as a change in dB (delta dB), allowed at the input port.
Max. Input Power	GC_MaxInputPower	The maximum input power (in dBm) allowed before the simulator aborts. This setting is used to prevent the simulator from continuing to search if it is having difficulty finding a solution.

## Defining Simulation Parameters

Defining the simulation parameters consists of four basic parts:

- Enabling the budget simulation.
- Specifying the desired level of detail in the simulation status summary
- Specifying the amount of device operating-point information to save

In the following table, names used in netlists and ADS schematics appear under *Parameter Name*.

**Table 1-3. XDB Simulation Parameter Options**

Setup Dialog Name	Parameter Name	Description
Device operating point level	DevOpPtLevel	Enables you to save all the device operating-point information to the dataset. In ADS, if this simulation performs more than one XDB analysis (from multiple XDB controllers), the device operating point data for all XDB analyses will be saved, not just the last one. Default setting is None.
None	None	No information is saved.
Brief	Brief	Saves device currents, power, and some linearized device parameters.
Detailed	Detailed	Saves the operating point values which include the device's currents, power, voltages, and linearized device parameters.
FFT		
Fundamental Oversample	FundOversample	Sets the FFT oversampling ratio. Higher levels increase the accuracy of the solution by reducing the FFT aliasing error and improving convergence. Memory and speed are affected less when the direct harmonic balance method is used than when the Krylov option is used.
More...	Oversample[n]	Displays a small dialog box. To increase simulation accuracy, enter in the field an integer representing a ratio by which the simulator will oversample each fundamental.

Table 1-3. XDB Simulation Parameter Options (continued)

Setup Dialog Name	Parameter Name	Description
Initial Guess		
Use Initial Guess	UseInFile	<p>Check this box to enter a file name for a solution to be used as initial guesses. This file is typically generated from a previous simulation by enabling <i>Write Final Solution</i>. If no initial guess file name is supplied, a default name (using DC solution) is generated internally, using the design name and appending the suffix <i>.hbs</i>. A suffix is neither required nor added to any user-supplied file name. For example, if you have saved the Harmonic Balance solution from a previous simulation, you can later do a nonlinear noise simulation and use this saved solution as the initial guess, removing the time required to recompute the nonlinear Harmonic Balance solution. Or you could quickly get to the initial Harmonic Balance solution, then sweep a parameter to see the changes. In this latter case, you will probably either want to disable the <i>Write Final Solution</i> option or use a different file name for the final solution to avoid overwriting the initial guess solution. (See <a href="#">“Write Final Solution” on page 1-13.</a>)</p> <p>The Annotate value specified in the DC Solutions tab in the Options block is also used to control the amount of annotation generated when there are topology changes detected during the reading of the initial guess file. Since HB simulations also utilize the DC solution, to get optimum speed-up, both the DC solution and the HB solution should be saved and re-used as initial guesses. See <i>DC Simulation</i>.</p> <p>The initial guess file does not need to contain all the HB frequencies. For example, one could do a one-tone simulation with just a very nonlinear LO, save that solution away and then use it as an initial guess in a two tone simulation. The exact frequencies do not have to match between the present analysis and the initial guess solution. However, the fundamental indexes should match. For example, a solution saved from a two tone analysis with Freq[1] = 1GHz and Freq[2] = 1kHz would not be a good match for a simulation with Freq[1] = 1kHz and Freq[2] = 1 GHz.</p> <p>If the simulator cannot converge with the supplied initial guess, it then attempts a global node-setting by connecting every node through a small resistor to an equivalent source. It then attempts to sweep this resistor value to a very large value and eventually tries to remove it.</p>
File	InFile	Specify a filename to save results.
Regenerate Initial Guess for ParamSweep (Restart)		
Final Solution		
Write Final Solution	UseOutFile	<p>Check this box to save your final HB solution to the output file. If a filename is not supplied, a file name is internally generate using the design name, followed by an <i>.hbs</i> suffix. If a file name is supplied, the suffix is neither appended nor required. If this box is checked, then the last HB solution is put out to the specified file. If this is the same file as that used for the Initial Guess, this file is updated with the latest solution.</p> <p>Transient simulations can also be programmed to generate a harmonic balance solution that can then be used as an initial guess for an HB simulation. Refer to <i>Harmonic Balance Simulation</i>.</p>
File	OutFile	Specify a filename to save results.

Table 1-3. XDB Simulation Parameter Options (continued)

Setup Dialog Name	Parameter Name	Description
Budget		
Perform Budget simulation	OutputBudgetIV	Enables Budget simulation, which reports current and voltage data at the pins of devices following a simulation. Current into the <i>n</i> th terminal of a device is identified as ... <i>device_name.tn.i</i> . Voltage at the <i>n</i> th terminal of a device is identified as ... <i>device_name.tn.v</i> .
Harmonic Balance Assisted Harmonic Balance	HBAHB_Enable	Set the HBAHB mode to <i>Auto</i> , <i>On</i> , or <i>Off</i> . Default is <i>Auto</i> and is recommended.

## Solver

Refer to the topic “Selecting a Harmonic Balance Technique” in the chapter “Harmonic Balance Basics” in the *Harmonic Balance Simulation* documentation.

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