



Agilent Technologies

Advanced Design System 2005A
Release Notes

April 2006

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ADS 2005A Release Notes

This document describes known defects in Advanced Design System 2005A and, wherever possible, provides a workaround. It also identifies errors and omissions in the documentation. The following table shows the version history for this document.

| Version | Date | Revised/New | Issue Title |
|-----------------|----------------|-------------|--|
| Initial Release | August 2005 | | |
| Update 1 | September 2005 | Revised | "Matlab Cosimulation in compiled mode with Matlab Compiler 4.0 is not supported" |
| | | New | "Verilog-A compiled files are version specific" |
| | | New | "DataAccessComponent uses different dialog boxes for DSP and A/RF schematics" |
| | | New | "Mixed unit types may be created following Yield Optimization" |
| | | New | "Multithread simulation on PC only works for DSP designs" |
| | | New | "WLAN_802_11b_TX WTB signal to ESG cannot be demodulated properly using the current default setting" |
| | | New | "Installation manual incorrectly lists 64-bit operating system support for ADS 2005A" |
| Update 2 | October 2005 | Revised | "Hyperlinks to PDF files do not work on Windows machines using Internet Explorer 6x" |
| Update 3 | April 2006 | Revised | "SIV and MDS migration not available in ADS2005A" |

For more information concerning known issues in Advanced Design System 2005A, or to report a new issue, refer to the Agilent EEsof Knowledge Center.

Installation

Installation manual incorrectly lists 64-bit operating system support for ADS 2005A

The UNIX and Linux Installation manual incorrectly lists 64-bit operating system support for ADS 2005A. ADS is not supported on 64-bit machines, nor is it supported on 64-bit machines running in 32-bit compatibility mode. Only 64-bit Momentum simulations are supported in 2005A.

For a current listing of supported operating systems for 2005A, refer to Chapter 1 in the [UNIX and Linux Installation](#) manual.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

<http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=211657>

Value of HOME variable in Environment Variables must match value in registry

To run properly, on the Windows platform, the HOME variable set in the environment must match the value stored in:

```
HKEY_LOCAL_MACHINE\Software\Agilent\ADS\2.9\eeenv\HOME
```

This registry value is normally set during the installation process.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

<http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Licensing.412>

Canceling the Uninstall Program on Windows Systems

The uninstall program on Windows may be very slow. If you cancel the uninstall program, you may encounter problems reinstalling ADS.

Workaround:

For ADS 2003C and earlier versions:

1. Delete the ADS installation folder. For example, select *C:\ADS2003C* using Windows Explorer then press the **shift** and **delete** keys. Select *yes* to confirm deletion of read-only and program files.

2. After the installation folder is deleted, select *Start > Programs > Advanced Design System (version) > Uninstall ADS*.

For ADS 2004A and newer versions:

1. Delete the ADS installation folder. For example, select *C:\ADS2004A* using Windows Explorer then press the **shift** and **delete** keys.
2. Reboot the PC.
3. Run ADS Uninstall using one of the following methods:
 - If you have access to the ADS CD ROMs, insert the PC Setup Program Disk1 into the disk drive. This should auto-launch the ADS installer. Select Remove to start the unistall process.
 - If you DO NOT have access to the ADS CD ROMs, select **Start > Run**, type the following command, then press **OK**:

```
C:\PROGRA~1\COMMON~1\INSTAL~1\Driver\9\INTEL3~1\IDriver.exe /M{A9ABAC9B-45C9-4026-81EC-1C3F0F72BFFF}
```

Note The space must be preserved in the proceeding typed command.

Solaris 8/9 require shared library patch for C++

The installation documentation's system requirements state that Solaris 8 systems without the C/C++ compiler require the shared library patch for C++. This patch is also required for Solaris 9. The following list identifies the patches for each system:

Solaris 8

108434-17 32-bit Shared library patch for C++

108435-17 64-bit Shared library patch for C++

Solaris 9

111711-11 32-bit Shared library patch for C++

111712-11 64-bit Shared library patch for C++

Patches are available at:

<http://sunsolve.sun.com/pub-cgi/show.pl?target=patchpage>

Select the patch report for your Solaris OS, or search for the specific patch number. Exact patch numbers may change as Sun issues new patches. You may need to look for the patch name instead.

Mouse cursor flickers on Linux

On Linux, if the windows manager option is set to: *Point in Window to make Active*, and several modal dialogs are open, it is possible that the mouse cursor will flicker.

Workaround: Set the windows manager option, *Click in Window to make Active* and unset *Point in Window to make Active*. The key here is whether to *click* or *point*. Some shells refer to this process as '*Focus follows mouse*' or '*Click to focus*'.

The location of the window manager options and descriptions may vary depending on the shell being used. Look for the area where windows style preferences or behavior can be set.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Layered_API.1442

Design Environment

Design file corrupted on saving

If you run out of disk space while saving a design on UNIX, the design file may get corrupted. The corrupted file may cause ADS to fail when you open the design.

Workaround: To avoid this problem, check your available disk space make sure you have enough before running ADS.

Unarchiving .zap files on UNIX with insufficient disk space

ADS may hang if you attempt to unarchive an archived (.zap) project on UNIX and do not have sufficient disk space. This problem has been observed on HP-UX 10.20 but may also occur on other operating systems.

Workaround: Ensure that you have sufficient disk space before unarchiving a large project (a large amount of RAM is also required). If necessary, try renaming the .zap file with a .z extension and use the *unzip* utility to decompress the project file.

Information on library_group is lost when design is copied

If you copy a design for which you have defined a library (the Library Name field in *File > Design Parameters*), the library information will be lost.

Workaround: Open the copied design, choose *File > Design Parameters*, and enter the desired library name in the Library Name field. Alternatively, you can manually edit the AEL file to add the desired library name.

Opening multiple designs on Windows

On the Windows platform, ADS will run out of memory if you open multiple design windows.

Workaround: Whenever possible, open or create designs within the same window. You can set opening and creating designs in an existing window as your default option by deselecting the *New/Open Design in New Window* option in the Main Preference dialog box (*Main window > Options > Preferences*).

Non-orthogonal rotations can put pins off grid

If the rotation increment is not a multiple of 90 degrees, it is possible to get symbol pins off the grid. This typically happens when the rotation angle is set to 45 degrees. When objects are rotated 45 degrees and then rotated again for another 45 degrees, the resulting instances may have their pins slightly off the grid.

Workaround: It is strongly recommended that users should check the *Options > Preferences Entry/Edit Rotation Angle* and set it to 90 degrees.

Backward compatibility for designs

Starting with ADS 2003C, you can open Analog/RF designs from subsequent versions of ADS. However, you will not be able to open Signal Processing designs from subsequent versions.

When opening an Analog/RF design from a subsequent version of ADS:

- The system displays a warning dialog box with a list of instances that were modified including a list of which parameters were updated.
- If the design from the subsequent version of ADS contains instances of components that did not exist in the current version of ADS, the system will be unable to find the component definitions for those components. You must delete these instances or replace them with alternative components.

Data Display

Problem with debug mode on the PC

Using the HPEESOF_DEBUG_MODE on the PC may cause the Data Display server to hang. This mode is invoked by the command *hpads_verbose*.

Workaround: If possible, do not use the debug mode on the PC.

Dataset Aliases should only be used to reference static data

You should only use Dataset Aliases to view data that is static and not changing during the Data Display session. If you use a Dataset Alias to reference trace or equation data, this data will not automatically update after the simulation completes.

Workaround: To force data referenced by a Dataset Alias to update, you must close and reopen Data Display window.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

<http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=AEL.775>

Electronic Notebook

Adding Data Display pages to an existing Electronic Notebook

If you attempt to add a Data Display page (using *Add Page* and the *New Notebook Page* dialog box) to an existing notebook, and that page is actually a combination of two or more data display files (such as you might create using the Smart Simulation Wizard), the Electronic Notebook may crash.

Workaround: Delete the existing */notebook* directory in the project of interest and generate the notebook again.

Physical Design

Push/Pop performance problem after importing dxf file

After importing a hierarchical layout (i.e., DXF, GDSII, etc.), if you push into a sub circuit and then pop out of it, there may be a long delay (several minutes) before the

pop out operation is completed. The same delay can exist when invoking the command *Edit > Component > Update Component Definitions*.

Workaround: After importing the layout, go to the Main window and select *File > Save All*.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Physical_Des.3471

Disabling Layout Connectivity Features

It is possible to disable layout connectivity features when there are performance and memory consumption problems with large designs such as reticles or imported designs. To disable layout connectivity features you must manually edit *de_sim.cfg* by adding the following line:

```
LAYOUT_PIN_CONNECTIVITY_ONLY=TRUE
```

For more information refer to “Checking Connectivity Information” in Chapter 11 of the *Schematic Capture and Layout* manual.

Analog/RF Simulation

Verilog-A compiled files are version specific

The Verilog-A compiled files (CML files) are compiled when you run the first simulation, or when you run a subsequent simulation containing a modification of an associated Verilog-A source file.

CML files are version specific. In ADS 2005A version 1.20 is used. To avoid compatibility problems between different versions, these CML files are placed in the 1.20 folder of the cache directory.

For 2004A simulations the CML files are still located in the 1.12 folder of the cache directory. If you use 2004A, the appropriate version of the files will be picked up.

DC simulation enhancements for 2005A

The robustness and speed of the default DC analysis algorithm has been significantly improved in 2005A. All DC analyses with factory-default settings are expected to converge to the correct solution with near-optimal speed. Therefore, by default, the

user-defined values of the advanced DC simulation parameters saved in previous releases are disabled and factory-defined default values are used. For more information, refer to the [DC Simulation](#) manual.

HB simulation enhancements for 2005A

2005A features improved robustness and near optimal speed of the HB analysis and its variants at factory default settings. The HB analyses at default settings achieve convergence rate above 90% and speed comparable to user-defined 4A settings.

In order to utilize these HB enhancements, please follow these guidelines:

1. New designs: Specify only the frequency and order in HB (For HB variants such as sweeps, HB noise, etc, some additional basic setup will be needed such as sweep range, noise frequencies, etc).
2. Existing design from previous release: Throw away the existing HB controller/analysis, and start fresh, specifying only the frequency and order (plus any HB variant basic setup).
3. If for some reason you wish to retain the simulation settings exactly as they were in a previous release, keep the existing HB controller/analysis and consult the HB simulation manual for a list of backwards compatibility exceptions. You will have to manually set these settings to their previous release values.

Oscillator phase noise ‘pnm_x’ improved and ‘pnf_m’ removed

Oscillator phase noise simulation now only computes *pnm_x*. The *pnm_x* flattening problems present at small offset frequencies have been fixed and *pnm_x* now provides a good phase noise result for all offset frequencies. The *pnf_m* result is no longer computed and existing data display setups from versions prior to ADS 2004A that plot *pnf_m* will show up as *<invalid>*.

PackFFT parameter in HB simulation

The parameter *PackFFT* controls the frequency map packing for multitone Harmonic Balance. By default, when it is not explicitly set to ‘yes’ or ‘no’, the simulator enables it (i.e., ‘yes’). Setting *PackFFT* to ‘yes’ may improve the simulation speed and reduce memory consumption by using a smaller number of time samples (smaller FFTs), but at the potential loss of dynamic range and accuracy due to the aliased harmonics of the first fundamental now possibly landing on various mixing tones. For mixers and other applications with a single large dominant (LO) tone, that frequency should be assigned to the first fundamental and *PackFFT* should be set to ‘no’ so that any

aliased harmonics of this large signal will just land on its own harmonics and not on mixing terms. If you are simulating mixer intermodulation or third-order intercept, it is recommended that this parameter be set to 'no' to achieve the most accurate results. In ADS, the parameter *PackFFT* is found on the *Display* tab of the HB and CE controllers. To set this parameter in ADS, check it on the Display tab and then set it to 'yes' or 'no' directly on the schematic. In RFDE, *PackFFT* is found in the Options dialog for the HB and Env analyses.

Simulating MGA_72543_SParam.dsn produces wrong results

The simulation results produced by

/examples/PtolemyDocExamples/Timed_RF_Subsystems_prj/networksMGA_72543_SParam.dsn are incorrect.

If you run this simulation, a simulation error message like the following will be generated:

```
Warning detected by HPEESOFPSIM during netlist parsing. SwitchV
X6.X1.X1.SWITCHV1 is shorted.
```

An updated design is available from the Agilent Knowledge Center at:

<http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=172707>

Behavioral Models

New version of VCA models: VCA_Setup and VCA_Data

The data-based amplifier modeling pair known as *VCA_Setup* and *VCA_Data* have been enhanced to include additional output-side-driven S-parameter information, (i.e., S22 and S12). This enhancement requires the extraction of a fresh VCA dataset using the new Setup component for compatibility with the new version of the VCA_Data amplifier model. A VCA dataset extracted by an earlier version of VCA_Setup will not work with the new VCA_Data model. If it is used, an error message will be generated and you will be asked to re-extract the behavioral profile using the latest version of VCA_Setup.

Performing MonteCarlo based P2D or S2D extraction

MonteCarlo analysis can now be performed in conjunction with P2D (or S2D) file extraction by setting up a MonteCarlo controller referenced *Xy.HB1* to the AmplifierP2D_Setup (or AmplifierS2D_Setup) controller with ID *Xy* on the same schematic. The variables of interest should be labelled for statistical analysis in standard fashion. The various trials of MC analysis are reported as *VAR mcTrial=X* statements to the P2D (or S2D) file. One point of caution is that if *StartTrial* is greater than zero then the data file will contain a *mcTrial=0* data segment followed by all the data segments pertaining to *mcTrial=StartTrial* through *mcTrial=Y* where $Y = \min\{\text{NumIters}, \text{StopTrial}\}$. This extra data point should not have an adverse effect on P2D (or S2D) behavioral model performance.

Use 'Simulate > Stop and Release Simulator...' in the schematic window to abort a simulation

If you stop a simulation from the Simulation Status window and then try to start another simulation, you may receive an error message stating: “*Foreground simulation already running*”.

This occurs because the inter-process communication messages (between the schematic editor and the simulation status window) to stop a simulation are not processed in the right order due to timing issues.

Workaround: Use the *Simulate > Stop and Release Simulator...* menu pick in the Schematic window to reset the simulator and allow further simulations to proceed.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

<http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Simulation.10460>

Nonlinear Devices

Do not use Mixer2 or MixerIMT2 with Budget Analysis

Budget simulation in Harmonic Balance has no knowledge that a frequency conversion takes place in the SDD-based Mixer2 and MixerIMT2 components. This leads to a frequency conflict and no plan is generated.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

<http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Simulation.7403>

Transformer and TransformerG obsoleted

The *Transformer* and *TransformerG* components have been obsoleted but are still available for backwards compatibility. To use the features available in these components, substitute the *TF* component for *Transformer* and *TransformerG*.

MixerIMT2 may not generate correct IMD levels

The MixerIMT2 documentation (in *Components > Circuit Components > System Models > System Data Models*), describes the MixerIMT2 component. It includes a description that explains how the values in the table are used to determine the levels

of the IMD when the RF and LO signals are different from the reference levels defined on the IMT table. Please be aware that the simulated signal levels of the IMD tones from the MixerIMT2 component may not follow this description when the RF signal levels are different from the reference given in the IMT table.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

<http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Simulation.8408>

<http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Simulation.8423>

<http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Simulation.8424>

Preventing simulation errors in foundry design kits used in circuit design

If a foundry design kit is used in a circuit design, it is recommended that the *ModelInclude/TechInclude/DesignKitInclude* component is placed at the top level (i.e., same level as the *TestLab/Sequencer*), and not placed in sub-circuits or individual test benches in order to prevent simulation errors.

AgilentHBT model DC operating point values are only approximate

The DC operating point values reported for four of the parameters of the AgilentHBT model, *Dthx*, *Dthi*, *Gmdc_ext* and *Gmdc_int*, are only approximate, analytical calculations based on the DC solution, and as such they may be inexact or inaccurate. It should be noted that these parameters in no way affect the validity of the model simulations. They are only meant to provide supplemental information.

RF System Budget Analysis

Sweep status not reported at every sweep point

If the Budget analysis controller is used with a *ParamSweep* or other parent controller, the current sweep status is not reported at every sweep point. Although, some ADS controllers like Harmonic Balance do report a status message (e.g., HB HB1[2/7]). The Budget controller does not send a status message during simulation. Also, when a warning or error is reported, the exact sweep point at which the event occurred is not reported.

Budget controller UI measurements tab Add > Apply > Delete empties list

On Unix and Linux platforms, performing the following steps on the Budget controller UI's measurements tab clears the list of selected measurements on the dialog box:

1. Select a measurement from the list on the left.
2. Click **Add**
3. Click **Apply**
4. Click **Delete**

This empties the entire list of selected measurements on the right, instead of the highlighted measurement on the list (the last one added).

Workaround: Click *cancel* and *undo* the last change on the schematic.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

<http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Simulation.10366>

Verilog-A

ADS status window appears frozen during Verilog-A compilation

The ADS status window appears frozen during Verilog-A compilation. This is a known behavior that does not have a workaround. Do not stop the simulation when you see this behavior. The Verilog-A compilation will finish and the status window will be updated at that point.

Compilation of large files on HP-UX

Compilation of large files (several thousand lines) on HP-UX is problematic with the supplied gcc compiler. The workaround is to use the cc compiler that is part of the aCC tool suite. In order to do so, you must have the cc compiler available on HP-UX. Appendix B of the “*Using Verilog-A in ADS/RFDE*” manual outlines how to switch from the gcc to the cc compiler. Note that the cc compiler that ships as part of the operating system will not work.

Lack of CML cache locking mechanisms

When Verilog-A modules are compiled to Compiled Model Library (CML) files, a CML cache directory is used. CML cache locking mechanisms have not been implemented in this release. This means that it is possible to encounter file sharing issues if multiple simulations using the same CML cache are run on the same platform at the same time.

Workaround: To avoid this problem, simulate on two different platforms, simulate sequentially instead of in parallel, or use separate caches for each simulation.

Transient simulation speed

The performance of Verilog-A based models relative to corresponding C based models is analysis dependent. For large Verilog-A files, Transient simulations are generally within a 2X window while the other analyses (DC, AC, Harmonic Balance, Circuit Envelope) are generally within a 1.5X window. This is significantly faster than traditional interpreted approaches.

Compile time

The Verilog-A compile time can vary dramatically depending on the size of the Verilog-A file, the platform, and the processor. For small files on fast machines, it takes a matter of seconds. For huge files on slow machines, it can take minutes or up to an hour. Note that for simulations taking only a few seconds, the compile time can far exceed the simulation time. On state-of-the-art hardware, compile time is not a roadblock for most customers.

Remote simulation requires an environment variable to be set

When working in a UNIX environment, you must set the environment variable

```
AGILENT_VERILOGA_COMPILER=hostname:agilent-vacomp
```

prior to running the ADS remote simulation daemon (hpremote). The same name can be used as is specified in the '*Remote Host Selection*' text box on the 'Single' tab of the 'Simulation Setup' dialog box.

The 'sim_veriloga' license can be pulled when it is not used

The license associated with compilation and loading of Verilog-A modules is '*sim_veriloga*'. Simulations without Verilog-A content do not pull the '*sim_veriloga*' license. The exception is when a Verilog-A file with a module which overrides a

built-in component is placed in the Verilog-A search path. In this case, the *'sim_veriloga'* license will get pulled, regardless of whether the component is used in the simulation or not.

ADS Ptolemy Simulation

Multithread simulation on PC only works for DSP designs

Multi-Thread simulation (MT) can speed up ADS simulation. However, there is a limitation on the PC. On a PC this only works for DSP designs. For Cosim designs there is no speed improvement and the simulation may fail.

Workaround: Use MT on Linux for Cosim to speed up the simulation.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Signal_Proc.3868

DataAccessComponent uses different dialog boxes for DSP and A/RF schematics

The DataAccessComponent uses different edit component parameter dialog boxes for DSP and A/RF schematics. The DSP schematic uses a standard ADS dialog box, however, the A/RF schematic uses an improved dialog box created exclusively for the DataAccessComponent. Consequently, if you place the DataAccessComponent on the DSP schematic first, and then place it on the A/RF schematic the standard dialog box will be used rather than updated one.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Signal_Proc.3872

Connectivity error when DSP subnetwork uses an iterated port

Ptolemy subnetworks do not support iterated ports. If a DSP subnetwork uses an iterated port, a connectivity error will be generated.

Workaround: Connect a *Bus* component (from the Numeric Control palette) to the port and specify the bus width for the *BusWidth* parameter. This creates a single multiport in the subnetwork.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Signal_Proc.2587

Red ‘anytype’ pins do not work properly with timed signals

Components with ‘anytype’ input pins will not propagate *timed* signals properly. These ‘anytype’ components should only be used with numeric signals (*int*, *float*, *fixed-point*, *complex*, and *matrix*). This restriction applies to the components in the Numeric Control library, such as the Commutator component.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Signal_Proc.2274

Misleading error message appears if DF controller is missing

When starting a Ptolemy simulation, the following, misleading, error message may appear:

```
Error detected by HPEESOFSIM during netlist parsing
  Undefined parameter "DefaultROut" used by ".X "
```

This message indicates that the design is missing a DF controller.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Signal_Proc.3016

Limitation on naming user-defined models

User-defined Ptolemy models cannot have the same name as standard ADS Ptolemy models. Creating a user-defined Ptolemy model with the same name as a standard ADS Ptolemy model may cause the simulator to crash when that model is used.

VSA_89600_Sink models cause Tk plots to hang

If you are using VSA_89600_Sink models in a simulation with Tcl/Tk models and you minimize a Tcl/Tk dialog box or window you will be unable to reopen that dialog box or window. The result is, you must exit the VSA 89600 software, which in turn causes ADS to hang, forcing you exit ADS.

Workaround: Pause the measurement using the pause icon on the VSA 89600 UI toolbar and then maximize the Tcl/Tk dialog box or window.

VeeLink component can cause internal error in VEE

Using the Ptolemy Vee Link component on a workstation that has a numeric character as the first letter of the host name causes an internal error in Vee. For example, if the PC you are using to run a simulation has a host name of *99Agent*, the simulation status window will record an error with the text *Internal error*, specifying the VeeLink component as the error source.

Workaround: Change the host name to have an alpha character first (i.e., *Agent99*) or use the IP Address in the HostName field when configuring the VeeLink component.

ESG/PSG Automatic Level Control(ALC) could fail for bursted signals

The *CM_ESG_E4438C_Sink* and *CM_PSG_E8267C_Sink* components optionally download an ADS generated signal to the instrument at the end of the simulation. When certain bursted waveforms are played on the ESG ARB, the ALC circuitry in the instrument fails to track the power level of the signal, and the output is corrupted. In such situations, you should see “UNLEVEL” displayed on the ESG front panel.

Workaround: Turning off ALC from the ESG front panel should help you get the expected ESG RF output.

CM_SStudioFileRead component doc refers to LocalFileName parameter of CM ESG/PSG sink components

A file compatible with the *CM_SStudioFileRead* can be created using the *CM_ESG_E4438C_Sink* or *CM_PSG_E8267C_Sink* components' *DownloadMode* parameter, not the *LocalFileName* parameter as reported in the documentation for the *CM_SStudioFileRead* component.

AEL warning messages when opening ADS 2002 designs containing MatlabLibLink in compiler mode can result in ADS hanging on Unix platforms

This problem is caused by any assignment statement in the user function that ends without using a semicolon(;).

For example, “a = 3” instead of “a = 3;”

Workaround: Use “ ; ” to end statements. This problem does not occur in script mode and does not occur on Win32 platforms.

MatlabLibLink in compiled mode does not respond on Windows

If the *mcc.log* file shows a prompt asking you to specify a compiler, open up a command prompt on windows and type:

```
mbuild -setup
```

You can choose *Icc*, which comes with the Matlab installation, or any other supported compiler such as VC++.

Also, be sure that the *mbuild.bat* file has the line:

```
set MATLAB=some_path
```

This line must point to your Matlab installation.

Matlab Cosimulation in compiled mode with Matlab Compiler 4.0 is not supported

Matlab Compiler 4.0 in the Matlab 14.0 release is not supported in ADS for compiled mode cosimulation. The *MatlabLibLink* component does not compile the script files. Compilation only works with Matlab Compiler 3.0.

Matlab Cosimulation with script mode is supported with Matlab 14.0.

Components with stringarray state parameters add one extra value

TkButtons, *TkShowBooleans* and *PatGen_16522A_Sink* have parameters that automatically add an extra value by inserting the stringarray state and their default value. These parameters are for labeling purposes but can cause simulation to fail if the number of labels is different than the number expected.

Workaround: Assume one extra label is always added and adjust the number of labels accordingly.

Type DataType moved to ADSPtometry namespace

The type *DataType* has moved from the global namespace to the *ADSPtometry* namespace. This was done to avoid conflicts with definitions in the *Windows.h* header. A variable of type *DataType* now must be declared as:

```
ADSPtometry::DataType myVar;
```

instead of

```
DataType myVar;
```

When assigning values to an *ADSPtolemy::DataType* variable or comparing its value against the predefined data types (INT, FLOAT, COMPLEX, FIX) the namespace specifier *ADSPtolemy::* must be used.

For example:

```
if ( myVar == ADSPtolemy::INT ) {
...
}
```

An alternative to using the *ADSPtolemy::namespace* specifier is to add the line using namespace ADSPtolemy; before declaring and using *ADSPtolemy::DataType* variables.

For example, in the go method you can have:

```
using namespace ADSPtolemy;
DataType myType;
myType = input.resolvedType(); // input is the name of the input port
if ( myType == INT ) {
...
}
else if ( myType == FLOAT ) {
...
}
else {
...
}
```

TimedSink does not record swept characterization frequency correctly

This problem occurs in simulations where a signal's characterization frequency is dependent on a swept variable. If such a signal is saved to the dataset using a TimedSink component, the sink will not record the varying characterization frequency (saved as attribute *f_c*) correctly. The characterization frequency that is recorded will be the same for all sweep points and will be equal to the signal's characterization frequency at the first sweep point.

Incorrect parameter settings of VSA_89600_Source may crash a simulation

If the parameters of *VSA_89600_Source* are incorrectly set, for example, a frequency trace (typically *VSATrace=A*) that is set for a timed output (*OutputType=Timed*), the VSA instance will disconnect itself and the simulation will become very slow or crash.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Instrument_Links.402

Scheduler problem with designs containing highly multirate data

If a simulation does not reach the status “Scheduler finished scheduling” in a reasonable amount of time, it means that the design contains complex multirate data.

Workaround: Break the design in two. Simulate the first design and dump the output to a file. Use the second design to read the data from the file and simulate it. You can use sequencer to chain the two designs back into one simulation.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Signal_Proc.3088

Component ‘ReadFilePreProc’ does not work with remote simulation

Component *ReadFilePreProc* can only be used with local simulations.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Signal_Proc.3637

HDL Cosimulation

Recommended HDL Simulator Tools

Mentor Graphics, ModelSim:

* Version 5.7g on HP-UX, Sun, Linux and PC platforms

Cadence, Verilog-XL:

- * Logic Design and Verification LDV 5.1 [05.10-p004] on HP-UX, Sun and Linux platforms
- * LDV 3.3 [3.30.p001] on PC platforms

Cadence, NCSim (NC-Verilog):

- * LDV 5.1 [05.10-p004] on HP-UX, Sun and Linux platforms
- * LDV 5.0 [05.00-s009] on PC platforms (HdlSimulatorGUI=ON mode does not work)
- * LDV 4.0 [04.00.p006] on PC platforms (HDL HdlSimulatorGUI=ON or OFF mode works properly)

HDL Cosimulation in UI mode does not work correctly when used with sweep or optimization

If the parameter “HdlSimulatorGUI” is set to “On” during a parametric sweep or when optimizing designs that contain the components *HdlCosim*, *NCCosim* or *VxlCosim*, HDL Cosimulation will error out after the first simulation point.

Workaround: Set the parameter “HdlSimulatorGUI” to “Off” during sweep or optimization.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Signal_Proc.3813

HDL Cosimulation with multi-threaded scheduler may hang-up

Windows 2000/XP dual processor machines and Solaris machines using any HDL Cosimulation component, along with the multi-threaded scheduler option set on the DF controller, causes the Cosimulation to randomly hang.

Workaround: The solution is to not use multi-threaded simulation on those operating systems for designs that hang-up the simulation. If the Cosimulation does hang, identify the started processes and manually kill them.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Signal_Proc.3863

ISS Cosimulation

DSP target limitations on setup

A DSP target should be specified using the *TI CCStudio Setup* tool. Only one DSP target can be specified, and it is limited to the TMS320C6x/TMS320C54x simulators. (Hardware boards such as DSK or EVM cannot be used as the DSP target.)

- If you specify more than one target, the Parallel Debug Manager will open during cosimulation and the cosimulation will fail.
- If you do not specify a DSP target during setup, a dialog box will pop up during cosimulation and prompt you to select a target DSP board or simulator. You will then have to select a configuration and double-click the *TI CCStudio* icon or restart *TI CCStudio*.

Examples

IS95A_ChnCodec_prj number of frames tested too small

In the example *IS95A_ChnCodec_prj*, the number of frames tested in the designs is too small to produce an accurate BER/FER for a high SNR.

Workaround: Use a larger number of frames to obtain good BER curves.

CDMA2K_RC_TD_prj examples inconsistent with CDMA 2000 standard

In some examples of forward link in *CDMA2K_RC_TD_prj*, the scrambling mode by long PN code and the data mapping for OTD mode are not consistent with the CDMA 2000 standard. You can still use these examples as references because this inconsistency has little influence on system performance.

PerchCH_prj data slot settings

In the *PerchCH_prj* example, the *.dsn* file has a setting for 1000 slots of data, but the associated dataset (*.dds*) file was obtained using a setting of 100 slots. Using larger slot numbers provides more accurate results, but leads to significantly longer simulation times.

Example Search is case insensitive

Example search is not case sensitive. For example, searching for the word “*Amplifier*” will yield the same results as searching for the word “*amplifier*”.

Momentum

Solving in RF mode then plotting S-parameters using the Visualization tool

If you try to plot S-parameters using the Visualization option, for a project that was last solved in RF mode, Visualization may crash. This is true when the S-parameters are in either the CITIfile format or the AFS (Adaptive Frequency Sweep) format. The problem is caused by the fact that the visualization option is expecting certain types of data (GAMMA and Z0) that MomentumRF does not generate.

Workaround: Display the S-parameters obtained from MomentumRF using the ADS Data Display.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Mom_UI_ADS.1033

Visualization current density off by a factor of 2

The actual current density in a plot is 2 times greater than the value reported by Momentum Visualization.

Stopping Momentum simulation process

The Momentum simulation process might not automatically stop after selecting *Simulation/Synthesis > Stop Simulation...* in the simulation status window.

Workaround: Manually terminate the Momentum simulation process from command line.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Mom_UI_ADS.1010

Visualizing surface currents of existing projects

The *Momentum* manual does not describe how to visualize the surface currents of existing projects with Momentum Visualization.

The surface currents of projects solved with Momentum under ADS 1.0 or ADS 1.1 can be visualized using Momentum Visualization. The surface currents shown are the superposition of weighted port solutions. The definition of a port solution was altered in ADS 1.3/1.5. In ADS 1.1 and earlier, a port solution was defined as follows:

A voltage source is attached to the port under consideration and all other ports are left open. Consequently, displaying individual port solutions will show standing wave patterns. For the port solution definition in ADS 1.3/1.5, refer to the chapter, “Displaying Surface Currents”, in the Momentum manual. Port solutions from ADS 1.1 and earlier can be transferred to the ADS 1.3 definition.

Contact Agilent technical support if you have trouble transferring port solutions.

Visualizing surface currents using discrete arrow plots

The *Momentum* documentation does not mention that arrow plots enable you to visualize the surface currents using a vector representation.

On a dense, uniform grid, a vector represents the sampled surface current. Normally, the grid density should be appropriate. If not, the discrete arrow plot provides another way to look at the surface currents. In a method of moments solution, your circuit is subdivided into a number of cells.

The surface current on each cell is expanded in a set of basis functions (Momentum uses rooftop basis functions). On a cell, there is a basis function associated with each edge. The total current on a cell is the linear superposition of all basis functions with their appropriate amplitude. In the discrete arrow plot, a vector is shown in the middle of all cell edges representing the basis function amplitude.

Setting absolute limits for layout parameters

You cannot set an absolute upper or lower limit for layout parameters that are defined for Momentum Layout Components. You should check to see whether or not a specific value is physically meaningful.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Mom_UI_ADS.1149

Simulating structures with a port on box and layer with thick metal expansion on

The simulation results of structures in a box, where the location of the port is on the box perimeter and on a metal layer where thick metal expansion is on, will be wrong as this port is shorted.

Workaround: Don't use thick metal expansion for the metal layer containing the port.

Problems occur when removing a nominal/perturbed parameter in a Momentum Layout Component

The first time a *nominal/perturbed* parameter of a Momentum layout component is deleted using **cut > ok**, it may not be completely removed. An error message reading, "*Design can not be read into this window*" typically pops up, however, the parameter can still be partially present.

After deleting a nominal/perturbed parameter, you should verify that it has actually been removed from the parameter list of a Momentum layout component.

Workaround: If the parameter is still present, re-do the delete operation before the next **Create/Update** of the layout component. This will completely remove the parameter.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Mom_UI_ADS.1499

Know problems when using Momentum in Digital Signal Processing Only mode

When ADS is setup in *Digital Signal Processing Only* mode, the creation of Momentum layout components and the usage of these components in the schematic environment will generate errors.

Workaround: Change the ADS setup to '*Analog/RF Only*', or '*Both, With Default: Analog/RF Design*'

Z0 and GAMMA values appear incorrectly in dataset

When selecting the *Momentum > Substrate > Create/Modify, Substrate Layers* tab, if Permittivity (Er) is set to Re, Conductivity, GAMMA will not appear in the dataset and the Z0 values will be set to the default of 50 ohms. This occurs because the port

solver was switched off to improve Momentum simulation speed.

To switch the port solver back on, the configuration variable located in, *HOME/hpeesof/config/momentum.cfg* must be set as follows:

```
MOM3D_USE_PORTSOLVER=2
```

This forces the port solver to run, and the Z0 and GAMMA entries will appear correctly in the dataset.

Momentum remote PVM cluster info added to console window

The Simulation System Startup dialog does not always allow you time to enable the *Show Cluster Configuration when Started* checkbox when using the PVM based remote simulation system. To remedy this, the cluster information is now displayed in the eesof Momentum Remote Simulation Console window. To update the information, select the Refresh button.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Mom_UI_ADS.1595

Advanced mesh settings in Advanced Model Composer need to use configuration variable

The AMC user interface does not allow you to take advantage of the advanced mesh options in Momentum such as horizontal side currents, transmission line mesh, layer specific mesh and primitive mesh.

A config variable needs to be defined in order to use the “layout settings” (meshing, ...) while building AMC models:

```
Set "PMLG_USE_LAYOUTSETTINGS=TRUE"
in "$HOME/hpeesof/config/pmlg.cfg"
```

Note AMC's Layout Component database is not protected against inconsistencies that one can introduce during generation if non-UI controlled parameters are changed during the creation process.

Tuning

Tuning Initialization Can Take Some Time

When launching Tuning, the initialization can take anywhere from a few seconds to a minute or more depending on the size of the design hierarchy. Currently, there is no work-around.

Include Opt Params does not include parameters with a space between opt and {

The *Include Opt Params* feature in *Tuning* does not include parameters that have a space between the `opt` and the “{” in their syntax.

Workaround: To ensure that these parameters are included, edit the parameter and remove the space.

Wireless Design Libraries

The DTV Design Library has been updated

The DTV Design Library has updated three areas in 2005A, ISDB-T usability, DVB-H and DVB-T channel estimation

1. Improve the usability of ISDB-T system

The new features are:

- provide top-level ISDB-T signal sources and receivers of one layer, two layers and three layers system.
- provide top-level partial receiver of ISDB-T to support narrowband ISDB-T system.
- develop ISDB-T demo systems, these demo systems include BER, MER, spectrum and constellation measurements and etc. These demo systems are as follows:

DTV_ISDB_Demo_OneLay.dsn

DTV_ISDB_Demo_ThreeLay.dsn

DTV_ISDB_Demo_TwoLay.dsn

DTV_ISDB_Demo_Partial.dsn

2. Develop DVB-H system

The new features are:

- provide top-level DVB-H signal sources and receivers of non-hierarchical and hierarchical structures
- develop DVB-H demo systems, these demo systems include BER, MER, spectrum and constellation measurements and etc. These demo systems are as follows:

DTV_DVBH_Demo_Hierarchical.dsn

DTV_DVBH_Demo_Non_Hierarchical.dsn

3. Improve channel estimation for DVB-T

The algorithm of two-dimension channel estimation and interpolation algorithm was updated (in *DTV_DVB2DChEstimator*). The BER performance of DVB-T system was improved. All the simulation results of DVB-T test benches were updated.

3GPP W-CDMA Design Library

The 3GPP product contains content for the 3GPP FDD mode and HSDPA over FDD mode. This product only supports 3GPP HSDPA Uplink. It does not include any 3GPP TDD mode capability. A separate Product with a separate license is released to support 3GPP TDD LCR(1.28 Mcps Option).

This release has the following new features:

- Generate uplink HSDPA channel along with the necessary W-CDMA control channels and/or data channels.
- Full receiver test capability. Analysis the BER in AWGN and fading channel for ACK/NACK signal and RMSE for CQI value.
- New top level signal sources and measurement models for 3GPP FDD mode.

Update to 3GPPFDD_HS_DPCCH_Decoder and 3GPPFDD_HS_DPCCH_Encoder subnetworks documentation

The HS_DPCCH physical channel mapping function must map input bits b_k directly to the physical channel so that bits are transmitted over the air in *ascending* order

with respect to k . In this subnetwork, bits are transmitted over the air in *descending* order with respect to k (where b_k and k are described in section 4.7 of 3GPP Technical Specification TS 25.212 V5.60 “Multiplexing and channel coding (FDD)” Release 5).

Workaround: For the 3GPPFDD_HS_DPCCH_Decoder, add a Reverse component (ADS Numeric Control library) between 3GPPFDD_HS_DPCCH_DeMux and the 3GPPFDD_HS_CQI_Decoder. Set the N parameter of the Reverse component to 20.

For the 3GPPFDD_HS_DPCCH_Encoder add a Reverse component (ADS Numeric Control library) between 3GPPFDD_HS_CQI_Encoder and the 3GPPFDD_HS_DPCCH_DeMux. Set the N parameter of the Reverse component to 20.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=CSDC_3GPP.728

UWB Design Library enhancements for 2005A

- A change the receiver structure to accommodate three sub-bands frequency hopping signal;
- Developed the fading channel model and test the PER under fading environment
- Added CSI to improve the decoding performance
- Updated the time synchronization algorithm to improve the robustness
- Added a frequency error parameter to the frequency hopping source
- Added one-pin EVM

Problem with long channel delay in UWB Design Library

The PER performance is poor in fading channels CM3 and CM4. The receiver needs to be improved.

Instrument Server

Instrument connectivity using the Instrument Server supported on PC only

Though the *Connection Manager* is recommended for ADS instrument connectivity, ADS continues to support legacy instrument interfaces like the instrument server and older instrument components but only on PC platforms.

The instrument server and older instrument components rely on the older SICL IO library for instrument connectivity. Because of this, instrument connectivity through the instrument server and older instrument components is supported on PC platforms only. The Instrument Server only exists on Windows platforms. However, data file translation capabilities are available in a new application, the Data File Tool.

Problem with datasets using .ds extension

The instrument server does not overwrite existing dataset data blocks, thus a unique blockname is required for every read of an instrument or file. You will receive an error message reporting the need for a unique blockname; however, on Win2000, ADS may hang if you close the Instrument Server immediately after receiving this error message.

Improper reading of units in Time Domain measurements

The instrument server currently does not support time domain measurements from a network analyzer. If you attempt to enter these measurements, the stop/start units will be returned as Hz, when they should be in seconds.

Connection Manager

Connection Manager 8510 measurement may not work with E2050 LAN/GPIB gateway

When 8510 measurements are connected to the instrument through an E2050 LAN/HPIB gateway, the Connection Manager Client will display an error dialog stating that the 8510 measurement did not collect enough data to fill the trace data array.

Workaround: The only known workaround is to use a different interface to communicate with the 8510. The E5810 LAN/HPIB gateway is known to work. An updated version of the IO Libraries will be released as soon as possible.

Color images printed in black and white

Xprinter cannot print color graphics saved as EPS, PCL4, or PCL5 files. Try printing directly to the LaserJet 5M printer or assign the 5M to FILE instead of printer.

Printed and screen colors differ

The HP Color LaserJet printer has problems printing color hardcopy from UNIX installations using Xprinter if the PCL Cartridge driver is selected. The colors in the hardcopy produced using this driver do not match those displayed on the monitor.

Workaround: Use the Color LaserJet PS driver when generating color hardcopy or print in monochrome.

“Print to File” does not work properly when the destination directory is read-only

“Print to File” does not work properly when the destination directory is set to read-only. In this case, a file is not generated and no error or warning message is displayed.

Workaround: Make sure the destination directory is not read only.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

<http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Hardcopy.446>

When adding new PPD files for unsupported printers, you must remove any spaces at end of the ModelName field

Some vendors provide PPD files whose *ModelName* field contains spaces after the model name, but before the ending quotation mark. This will cause the 3rd party printing system used in ADS to crash.

Workaround: Before adding new PPD files, check for these spaces and remove them.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

<http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Hardcopy.443>

The Print Setup Dialog may cause a crash on RedHat Enterprise v3 machines under certain circumstances

Bringing up the Print Setup dialog on RedHat Enterprise v3 machines may cause the application to crash under certain circumstances. This has only been observed once, but the root cause for this failure has not yet been identified.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

<http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Hardcopy.442>

DesignGuides

Mixed unit types may be created following Yield Optimization

When using the *Filter DesignGuide* or *Impedance Matching Tool* to perform Yield Optimization, a parameter may be updated following the optimization with mixed unit types, (e.g., the nominal value is in pF but the optimization range values are in fF). This will cause a warning message to be issued and the schematic window to show the network.

Workaround: To correct this, edit the component making the units consistent and re-save the design. The DesignGuide can now be used with the corrected network.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

<http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=DesignGuides.860>

Context-sensitive help not enabled for all DesignGuide commands

If you are using the cascading menu configuration on the PC and attempt to access the context-sensitive help (*Help > What's This?*) for a command, you may not get the requested information. Context-sensitive help is not enabled for a number of DesignGuide commands. Please refer directly to the documentation for the DesignGuide for the desired information.

Missing help for DesignGuide subnetworks

Many DesignGuide schematics contain subnetworks. If the subnetwork has no modifiable parameters, no online help is available for it.

DeveloperStudio issues

- The Palette Editor does not update the display of an edited bitmap until you log out and restart ADS (UNIX only)
- There is a refresh problem in the Content Browser. If you map content to a subnetwork collector, it only displays the first nine characters in the subnetwork name. If you collapse the subnetwork collector, and re-open it, then the full name is displayed.
- SUN OS—If you are editing the Palette Name in the Palette Editor, and you press the down arrow on the keyboard, it produces an error.
- Report Summary for Palette (and others) has a sizing problem; it is not able to show all of the information without cutting off some text.

DeveloperStudio limitations not documented

- The bitmap viewer in the dialog *Insert Palette Item* is not as wide as the window will permit. It wraps the bitmaps to a second row.
- The preview feature of the Bitmap Editor only works on the PC.
- The Palette Editor *Insert Palette Item/Change Caption* feature is only available on the PC.
- The Content Editor does not allow file browsing, so the source ADS projects must reside at the top level of \$HOME, and the starting HTML files must reside at the top level of *studio_files/<project_name>/doc*.
- UNIX—The background colors for the window pick up the user settings and do not use the ADS window colors. This sometimes makes the user interface difficult to view. The default background colors work best.
- After using the Menu Editor to make a change in the name of a menu, there is a delay in the time it takes menus to respond after being selected.

RF System DesignGuide WCDMA Forward Link design simulates incorrectly on Linux

The WCDMA Forward Link test bench in the RF System DesignGuide does not simulate correctly on the Linux platform.

Workaround: Correct results may be obtained using other supported platforms.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

<http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Simulation.10078>

IBIS simulation in ADS2005A supports V-T tables

IBIS simulation in ADS2005A supports V-T tables and is significantly different from the ADS2004A version. To make use of V-T table data, you must re-import IBIS models using ADS2005A and replace all IBIS components on the schematic page if created using ASD2004A version.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

<http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=DesignGuides.829>

IBIS simulation convergence

If DC simulation does not converge or if it takes a long time for an IBIS simulation, place the *Transient Simulation Option* component on your schematic page. Set DC Mode to **Options > Convergence > Advanced Setting Button**, set *Advanced DC Convergence Setting Mode* to *Hybrid Solver*. Stop and rerun the simulation.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

<http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Simulation.11142>

Analog/RF WCDMA sources do not have calibrated output power

In the RF System DesignGuide, the WCDMA signal sources located under *Additional Analog/RF Sources > WCDMA* have a *Pavs* parameter that is used to set the average output power. However, the actual average output power will vary depending upon the channel configuration that is used.

Workaround: To calibrate the source, use the *Power Calcs.* page on the corresponding data display and adjust *Pavs* until *Pout_dBm* indicates the desired output power.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

<http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=DesignGuides.844>

RFIP Encoder

The IP Encoder in ADS2004A doesn't copy datafiles into designkit

This issue has been resolved in ADS2005A. All datafiles referenced in the design are copied into the “data” directory of the design kit.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=IP_Encoder.192

The ads_encoder license doesn't release after use

This issue has been resolved in ADS2005A. The *ads_encoder* license now gets released properly after use. This is true even if the “Encode Design” dialog box is canceled.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=IP_Encoder.191

Documentation Search

Partial word queries

Using a partial word for a query entry could prevent the search engine from finding any matches. For example, when you perform a query, use a complete term such as *hpeesofsim* because no matches will be found for *eesofsim*.

Boolean operators are not allowed in searches for exact phrases

When searching for an exact phrase, Boolean operators (AND, NOT, OR) are not allowed in the query. For example, the exact phrase “design and display” is not allowed, and the following message will appear:

“Bad query. Not expected in phrase: and.”

Workaround: Try to reformulate your query using an alternate syntax such as:

design NEAR display

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Learning_Prd.4407

Running a second search in the Documentation window causes an error

When you run a search using the entry box available in the Documentation window, a Search window appears with the results. On UNIX, if you run a second search in the Documentation window (not in the Search window), a JavaScript error appears: “Search applet undefined”.

Workarounds:

- When the Search window is open, run any additional searches from the Search window.
- If you prefer running additional searches from the Documentation window, close the Search window first, or click Reload in the Documentation window's toolbar, then run the search.

Documentation Search errors may occur on WinXP SP2 systems with local ADS installations

In certain cases, documentation search errors may occur on Windows XP SP2 systems if you are logged in as a local user without administrator privileges.

Workarounds:

- Use a different web browser such as Netscape or Mozilla Firefox.
- Have administrator privileges enabled for you.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Learning_Prd.4523

Documentation/Online Help

Hyperlinks to PDF files do not work on Windows machines using Internet Explorer 6x

In Microsoft Windows machines running Internet Explorer 6.x, there may be no response when a hyperlink to a PDF file is clicked.

Workarounds:

This is a problem with the security settings in Internet Explorer 6x. The workaround is as follows:

1. Open IE 6.x.
2. Choose **Tools > Internet Options**.
3. Click the **Security** tab.
4. Click the **Local Intranet** icon.
5. Click the **Sites** button.
6. Click the **Advanced** button.
7. Enter "*http://eesof.tm.agilent.com*" in the "*Add this Web site to the Zone*" field.
8. Click the **Add** button.
9. Accept the changes to the preceding dialogs by selecting **OK** for each.

Alternately you may:

- Right-click the PDF hyperlink, then choose "*Save Target As*".
- Use a different web browser such as Netscape or Mozilla Firefox.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Learning_Prd.4529

Hyperlink to Examples does not work on Windows XP SP2 using Internet Explorer

In Microsoft Windows XP SP2 running Internet Explorer 6.x, there is no response when clicking the hyperlink to the *Examples* documentation.

Workarounds:

- Access the ADS 2005A Examples Documentation from the Agilent EEsof Product Documentation Web site at:

<http://www.agilent.com/find/eesof-docs/>

- Use a different web browser such as Netscape or Mozilla Firefox.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Learning_Prd.4531

Others

Spectre netlist translator does not handle the spice netlist syntax

Spectre translator cannot handle the spectre simulatable netlist, which contains the spice syntax.

Workaround:

There are two options:

1. Translate spice netlist files using the spice/hspice translator and then modify the netlist as required. This is preferred.
2. Manually convert the spice syntax to spectre syntax and then use spectre translator.

Note that the spice/hspice translator handles a pure spice/hspice syntax and spectre translator handles a pure spectre syntax. For more details, refer to Chapter 3 in the *Netlist Translator for SPICE and Spectre* manual.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Spectre_Tran.239

USB hardware key not recognized in PCs using newer Intel chipsets

Some USB hardware keys are not recognized with systems using one of Intel's newer chipsets.

Workaround: To remedy this you need to download the latest FLEXid drivers from:

<http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=191479>

SIV and MDS migration not available in ADS2005A

Both SIV and MDS migration have been removed as features in the ADS2005A release.

Workaround: For SIV migration you can use ADS2004A for the migration, save the design/project and then open it using ADS2005A.

WLAN_802_11b_TX WTB signal to ESG cannot be demodulated properly using the current default setting

For RFDE Examples/WLAN/WLAN_WTB_Test, using WLAN_802_11b_TX WTB under the default setting the signal downloaded to ESGc cannot be demodulated properly. This is because the default value of the parameter ESG_SampleClkRate is incorrect. This value needs to be set to 66 MHz instead of 80 MHz.

Workaround: To resolve this problem either change the ESG_SampleClkRate from 80 MHz to 66 MHz in the *wtb* design, or change the ARB Sample Clock from 80 MHz to 66 MHz for the ESGc ARB setup.

More information about this issue may be found by referring to the Agilent EEsof Knowledge Center at:

http://edasupportweb.soco.agilent.com/cgi-bin/show.pl?id=Signal_Proc.3874

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