



Agilent Technologies

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HDL Blocks

Advanced Design System 2008

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395 Page Mill Road, Palo Alto, CA 94304 U.S.A.

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HdICosim



Description: General HDLCOSIM star to cosimulate with any VHDL/Verilog entity using ModelTech EE simulator

Library: HDL Blocks

Class: SDFHdICosim

Parameters

Name	Description	Default	Unit	Type	Range
HdlSrcFile	HDL Source file followed by the dependency files (space separated) to be built, or ADS project compile_verilog or compile_vhdl files, and if empty read compile_verilog (compile*.bat files read on WIN32)			filename	
Inputs	Names of the input HDL ports to communicate with			string array	
InputPhases	Delay to be used for updating inputs within			int array	

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	each IterationTime step				
InputPrecisions	Precision of the inputs in the sequence they appear in the HDL definition			string array	
Outputs	Names of the output HDL ports to communicate with			string array	
OutputPrecisions	Precision of the outputs in the sequence they appear in the HDL definition			string array	
HdlModelName	VHDL entity[.architecture]+configuration] or Verilog module name to cosimulate with			string	
HdlLibrary	HDL libraries (space separated) that user model depends on (to map them explicitly use name=path syntax), if set to none then all the code will be compiled in work library, and to avoid recompiling use "work" (remember that code must be compiled atleast once before cosimulation)			filename	
HdlSimulatorGUI	HDL simulator Graphical User Interface Mode: Off, On	Off		enum	

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CmdArgs	HDL Simulator command invocation arguments, if any			filename	
IterationTime	Time to run the HDL block before collecting the outputs	100		int	
TimeUnit	Time resolution limit to be passed to HDL simulator: fs, ps, ns, us, ms, sec	ns		enum	

Pin Inputs

Pin	Name	Description	Signal Type
1	Clock	Inputs to write data to 'Clock' port specified for Inputs parameter (if unconnected and 'Clock' is specified for Inputs parameter, then a default signal will be sent)	fix
2	Set	Inputs to write data to 'Set' port specified for Inputs parameter (if unconnected and 'Set' is specified for Inputs parameter, then a default signal will be sent)	fix
3	hdlCosimMultiInput	Inputs to write data to HDL ports specified for Inputs parameter	multiple fix

Pin Outputs

Pin	Name	Description	Signal Type
4	hdlCosimMultiOutput	Outputs to read data from HDL ports specified for Outputs parameter	multiple fix

Notes/Equations

1. For detailed descriptions of these parameters, refer to [HDL Cosimulation Components and Their Parameters](#).

NCCosim



Description: General HDLCOSIM star to cosimulate with any Verilog module using NCVerilog simulator

Library: HDL Blocks

Class: SDFNCCosim

Parameters

Name	Description	Default	Unit	Type	Range
HdlSrcFile	HDL Source file followed by the dependency files (space separated) to be built, or ADS project compile_verilog or compile_vhdl files, and if empty read compile_verilog (compile*.bat files read on WIN32)			filename	
Inputs	Names of the input HDL ports to communicate with			string array	
InputPhases	Delay to be used for updating inputs within each IterationTime step			int array	

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InputPrecisions	Precision of the inputs in the sequence they appear in the HDL definition			string array	
Outputs	Names of the output HDL ports to communicate with			string array	
OutputPrecisions	Precision of the outputs in the sequence they appear in the HDL definition			string array	
HdlModelName	VHDL entity[.architecture] or Verilog module name to cosimulate with			string	
HdlSimulatorGUI	HDL simulator Graphical User Interface Mode: Off, On	Off		enum	
CmdArgs	HDL Simulator command invocation arguments, if any			filename	
IterationTime	Time to run the HDL block before collecting the outputs	100		int	
TimeUnit	Time resolution limit to be passed to HDL simulator: fs, ps, ns, us, ms, sec	ns		enum	

Pin Inputs

Pin	Name	Description	Signal Type
1	Clock	Inputs to write data to 'Clock' port specified for Inputs parameter (if unconnected and 'Clock' is	fix

		specified for Inputs parameter, then a default signal will be sent)	
2	Set	Inputs to write data to 'Set' port specified for Inputs parameter (if unconnected and 'Set' is specified for Inputs parameter, then a default signal will be sent)	fix
3	hdlCosimMultiInput	Inputs to write data to HDL ports specified for Inputs parameter	multiple fix

Pin Outputs

Pin	Name	Description	Signal Type
4	hdlCosimMultiOutput	Outputs to read data from HDL ports specified for Outputs parameter	multiple fix

Notes/Equations

1. For detailed descriptions of these parameters, refer to [HDL Cosimulation Components and Their Parameters](#).

VxICosim



Description: General HDLCOSIM star to cosimulate with any Verilog module using VerilogXL simulator
 Library: HDL Blocks
 Class: SDFVxICosim

Parameters

Name	Description	Default	Unit	Type	Range
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HdlSrcFile	HDL Source file followed by the dependency files (space separated) to be built, or ADS project compile_verilog or compile_vhdl files, and if empty read compile_verilog (compile*.bat files read on WIN32)			filename	
Inputs	Names of the input HDL ports to communicate with			string array	
InputPhases	Delay to be used for updating inputs within each IterationTime step			int array	
InputPrecisions	Precision of the inputs in the sequence they appear in the HDL definition			string array	
Outputs	Names of the output HDL ports to communicate with			string array	
OutputPrecisions	Precision of the outputs in the sequence they appear in the HDL definition			string array	
HdlModelName	VHDL entity[.architecture;]+configuration] or Verilog module name to cosimulate with			string	
HdlSimulatorGUI	HDL simulator	Off		enum	

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	Graphical User Interface Mode: Off, On				
CmdArgs	HDL Simulator command invocation arguments, if any			filename	
IterationTime	Time to run the HDL block before collecting the outputs	100		int	
TimeUnit	Time resolution limit to be passed to HDL simulator: fs, ps, ns, us, ms, sec	ns		enum	

Pin Inputs

Pin	Name	Description	Signal Type
1	Clock	Inputs to write data to 'Clock' port specified for Inputs parameter (if unconnected and 'Clock' is specified for Inputs parameter, then a default signal will be sent)	fix
2	Set	Inputs to write data to 'Set' port specified for Inputs parameter (if unconnected and 'Set' is specified for Inputs parameter, then a default signal will be sent)	fix
3	hdlCosimMultiInput	Inputs to write data to HDL ports specified for Inputs parameter	multiple fix

Pin Outputs

Pin	Name	Description	Signal Type
4	hdlCosimMultiOutput	Outputs to read data from HDL ports specified for Outputs parameter	multiple fix

Notes/Equations

1. For detailed descriptions of these parameters, refer to [HDL Cosimulation Components and Their Parameters](#).